Engineering 1620 – Spring 2020

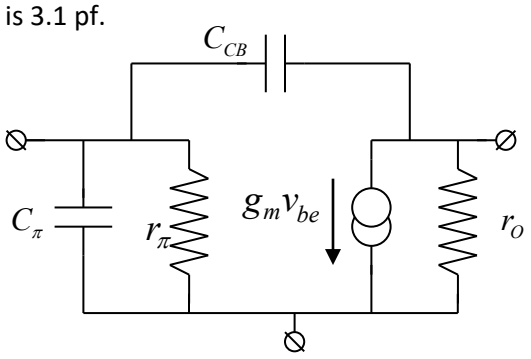
Homework Set 4 Answers

1) Here is the basic hybrid-pi model of a BJT transistor. It is probably too simplistic as it ignores parasitic resistances in series with each terminal of the device, the inductance of the package connections, and additional capacitance from the package to ground in the board on which the transistor gets mounted. My purpose in setting the problem was just to remind you of where the principal effects come from and give you a sense of the numbers.

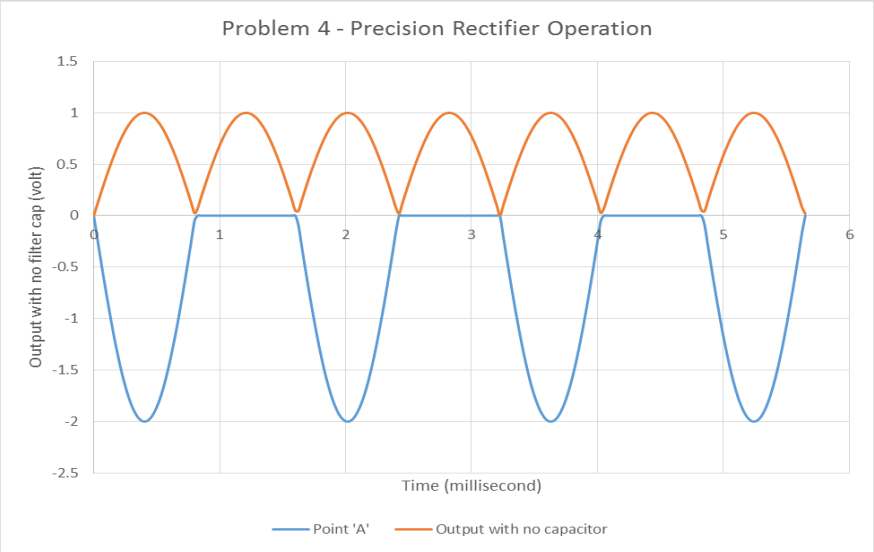
Filling in values for the BFP640 from its data sheet in no particular order: From figure 12 at V_{CB} = 2.5 – V_{BE} = 1.9 volts, C_{CB} = 0.093 pf (estimate); from figure 3 at 20 mA and V_{CE} = 2.5 volts, the output resistance r_0 is >> 2 K so can be treated as infinite for high frequency calculations; from the usual formula for transconductance, $g_m = \frac{qI_{CQ}}{kT} = \frac{0.02}{0.0256} = 0.78$ sie; from figure 4 at 20 mA, h_{FE} = 200; from the usual formula for $r_\pi = \frac{(1+h_{FE})kT}{qI_E} = 269$ ohms; and finally from figure 8, F_T = 39 GHz from which we can calculate C_π:

$$f_T = \frac{1}{2\pi r_e (C_\pi + C_{CB})} \text{ or } C_\pi = \frac{1}{2\pi r_e f_T} - C_{CB}.$$

On substitution: C_π is 3.1 pf.



2) Here are parts 2.1 and 2.3 in an Excel graph:

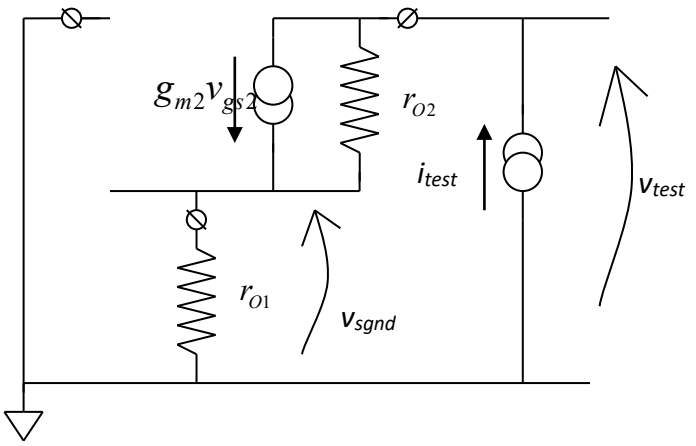


2.2) D2 prevents the opamp from going into output stage saturation when the input signal is negative and thus reduces the response time of the circuit when the signal becomes positive again. It limits the negative output swing to a single diode forward voltage drop.

2.4) The average value of a rectified sinusoid is $V_{AVG} = \frac{2V_{peak}}{\pi} = 0.637 \text{ volts}$. The filter time constant leads to a cutoff frequency of the filter at $f_C = \frac{1}{2\pi 1 \cdot 10^{+5} 1.6 \cdot 10^{-7}} = 10 \text{ Hz}.$ The lowest frequency in the output is 1240 Hz so the ripple is roughly .637/124 = 5.1 mV.

3.1) While this might be used as a current mirror, it probably should be called a current source because the input side of the mirror has a fixed current rather than a time dependent signal. M3 and M1 are the matched pair that have the same VGS and nearly the same VDS that forces the current in M3 to be mirrored in M1. M2 increases the output impedance by cascoding the output drain current of M1. M3 provides the fixed gate voltage to the cascoding transistor but its primary purpose is to equalize the drain voltages of M1 and M3 to improve the current match.

3.2) The output resistance of the circuit is the ratio of a change in output voltage to a consequent change in the output current. To calculate it, one needs the small signal equivalent circuit of the output side of the mirror. At low frequencies when the gate-drain capacitance of M2 can be neglected, the gate voltages of M1 and M2 are constant and hence at small signal ground. Because the small signal model has the gate of M1 grounded, the dependent current source in M1 is zero current; only the output resistance of M1 from channel length modulation is needed in the circuit model. Also add a test current, i_{test}, to drive the output of the model. The final model is simply



The current through r_{O1} is i_{test} so $v_{gs2} = -i_{test} r_{O1}$. The KCL equation at the drain is

$$i_{test} = -g_{m2} r_{O1} i_{test} + \frac{v_{test} - i_{test} r_{O1}}{r_{O2}}$$

Multiply through by r_{O2} and collect terms to get $z_{out} = \left(1 + g_{m2} r_{O1}\right) r_{O2} + r_{O1}$. The term $g_{m2} r_{O1}$ reflects the effect of source (or emitter degeneration) on output impedance and is one of the standard results a designer has to keep in mind all the time.

3.3) The input path has two gate-drain connected transistors in series and the resistance of each is the inverse of its transconductance. The total resistance is thus $r_{in} = \frac{2}{g_m}$. (The numeric value is 1.6e4 ohms.)

3.4) All four transistors have the same current, ID = 20 uamp. The transconductance is $g_m \approx \frac{2I_D}{V_{ov}} = 1.2 \cdot 10^{-4}$ sie. Since lambda is small and VDS is low (on M1 it is about 1 volt) we can write $r_O \approx \frac{1}{\lambda I_D} = 2 \cdot 10^6$ and then the output resistance is $242 r_O = 4.84 \cdot 10^8$ ohms.

3.5) The key observation here is that this circuit also acts like a current mirror. The gate-drain capacitance of M2 extends from the output to the input node. The input resistance is relatively low so any test voltage applied to the output terminal would largely appear across C_{GD} and the current through that would be copied through the mirror thus doubling the effect of C_{GD}. The total apparent capacitance would be $C_{OUT} = 2C_{GD} + C_{GSS}$

4) The starting point is to write out the gain of the amplifier. It has a single dominant pole at $f_d = \frac{f_{GBW}}{A_{OL}}$ where f_{GBW} is the gain-bandwidth product and A_{OL} is the low frequency open-loop gain. With this:

$$A(s) = \frac{A_{OL}}{1 + j\frac{f}{f_d}} \text{ and } 1 + A(s) = A_{OL}\frac{1 + j\frac{f}{f_{GBW}}}{1 + j\frac{f}{f_d}}$$

where this assumes that $A_{OL} >> 1$. In this problem $A_{OL} = 4 \cdot 10^5$ ohms and $f_d = \frac{2.4 \cdot 10^7}{4 \cdot 10^5} = 60$ Hz.

4.1) By Miller's theorem, the input should appear to have an impedance equivalent to C_{INT} scaled by the factor $1 + A(s)$. From the impedance of a capacitor this is

$$z = \frac{1}{j2\pi f A_{OL} C_{INT}}\left[\frac{1 + j\frac{f}{f_d}}{1 + j\frac{f}{f_{GBW}}}\right]$$

4.2) At 1 Hz, the phase angle of the pole-zero ratio in the brackets is negligible (or to be more exact 0.94 degrees). So the impedance has a – 89.1 degree phase, and is essentially a 60 ufd capacitor with reactance of 2.75 K ohms.

4.3) At 1 KHz, the phase angle in the bracket is $\tan^{-1}\left(\frac{1000}{60}\right) = 86.6$ degrees. (The denominator still has negligible imaginary part.) This moves the phase of the impedance to 3.4 degrees making it essentially a resistor. The magnitude is $|z| \approx \frac{1}{2\pi f_d A_{OL} C_{INT}} = 332$ ohms, essentially a 332 ohm resistor.

4.4) The reactance of the 15 pf capacitance of the amplifier input impedance is 9.8 megohms so that is negligible in comparison to the 332 ohm resistor.

4.5) At 1 MHz, the phase angle of the numerator of z is 90 degrees since the imaginary part of the numerator is 16,000 times bigger than the real part. The denominator contributes a phase of -2.4 degrees so the impedance is still essentially a resistor. The magnitude is still 332 ohms.

In the frequency range from somewhat above the dominant pole frequency until nearly the unity gain frequency, the input impedance stays constant and resistive. The decrease in reactance of C_{INT} is offset because the amplification from the opamp is decreasing above the dominant pole frequency. The two effects have inverse dependence on frequency and so cancel. Similarly C_{INT} and the amplifier have offsetting phase shifts of nearly 90 degrees that net to near zero degrees.

5.) The problem requires writing the two KCL node equations and using the equality of the base currents in Q1 and Q2. The output current is beta times the base current of Q3. The full set of equations in some detail is:

$$
\begin{aligned}
i_{in} &= i_{b3} + i_{c1} \\
i_{c1} &= \beta i_{b1} \\
i_{out} &= \beta i_{b3} \\
i_{b1} &= i_{b2} \\
(\beta+1) i_{b3} &= (\beta+1) i_{b2} + i_{b1}
\end{aligned}
$$

The solution for the difference between the input and output currents is that the input current exceeds the output by $i_{in} - i_{out} = \dfrac{2i_{in}}{\beta^2 + 2\beta + 2} \approx \dfrac{2i_{in}}{\beta^2}$.

6.1) Let the closed loop gain of the amplifier be $G \equiv 1 + \dfrac{R2}{R1}$. Let the voltage relative to ground at the node where C2 joins the two resistors, R, be v_1. Then the output voltage in terms of the voltage at v_1 is by inspection:

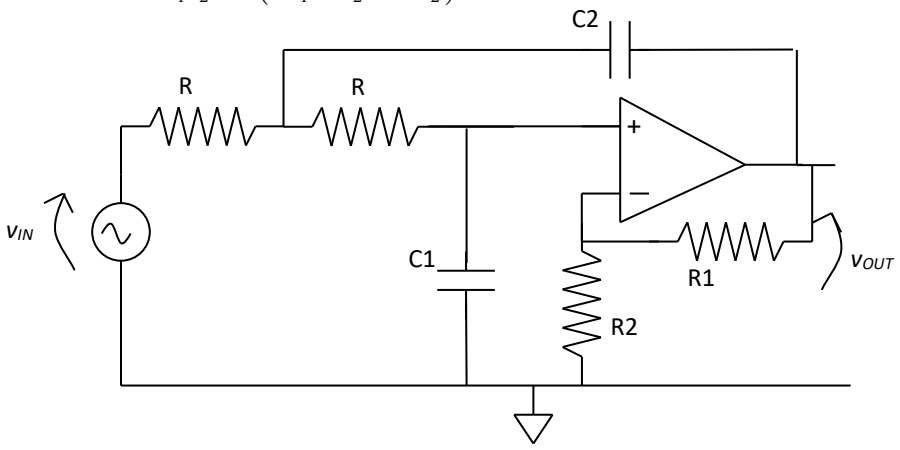
$$v_{OUT} = \frac{G}{1+s\tau_1} v_1 \text{ or } v_1 = \frac{1+s\tau_1}{G} v_{OUT}$$

where $\tau_1 = RC_1$. The KCL current nodal equation at v_1 is:

$$0 = v_1 \left[\frac{1}{R} + \frac{sC_1}{1+s\tau_1} + sC_2 \right] - \frac{v_{IN}}{R} - sC_2 v_{OUT}$$

$$Gv_{IN} = \left[1 + s\tau_1 + s\tau_1 + s\tau_2 \left(1 + + s\tau_1 \right) - Gs\tau_2 \right] v_{OUT}$$

and $H(s) = \dfrac{G}{s^2\tau_1\tau_2 + s(2\tau_1 + \tau_2 - G\tau_2) + 1}$ *qed.*



6.2) The easy part first: select an arbitrary value for R2, say 10 K, then R1 = 4 K. If R = 1 megohm, then the numerical values of the two time constants are simply the values of the capacitors expressed in microfarads. The second order Butterworth polynomial is $s^2 + \sqrt{2}s + 1$ so by comparison we have:

$$C_1 C_2 = 1 \text{ and } \sqrt{2} = 2C_1 + C_2 - 1.4C_2$$

Multiplying the second equation by C_2 and eliminating C_1 leaves $0.4C_2^2 + \sqrt{2}C_2 - 2 = 0$, the solution of which is C_2 = 1.083 ufd. C_1 = 0.924 ufd.

6.3) For operation with a bandwidth of 3.1 KHz, we need to divide the capacitors by $2\pi \cdot 3.1 \cdot 10^3 = 1.948 \cdot 10^4$ but scaling the resistor value from 1 megohm to 100 K increases the capacitors by a factor of 10. The net effect is that $C_2 = \frac{1.08}{1.948 \cdot 10^3} = 555$ pf and C_1 = 474 pf.