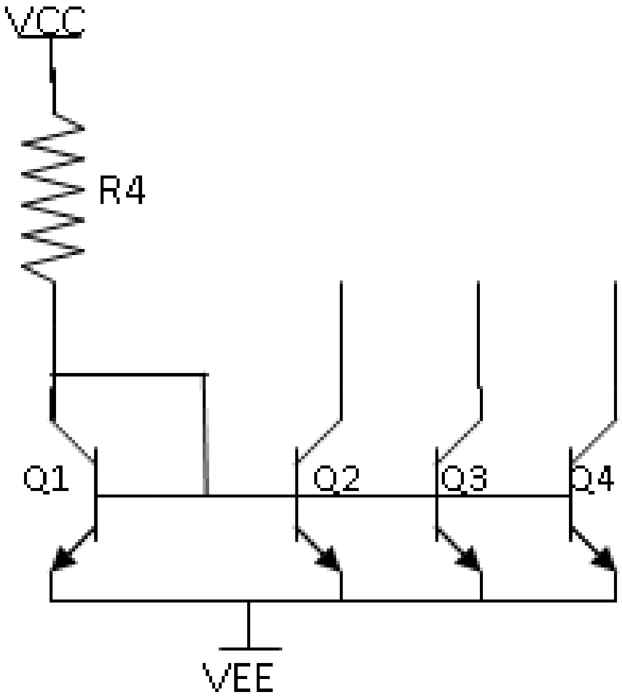
Analog Integrated Circuit Configurations

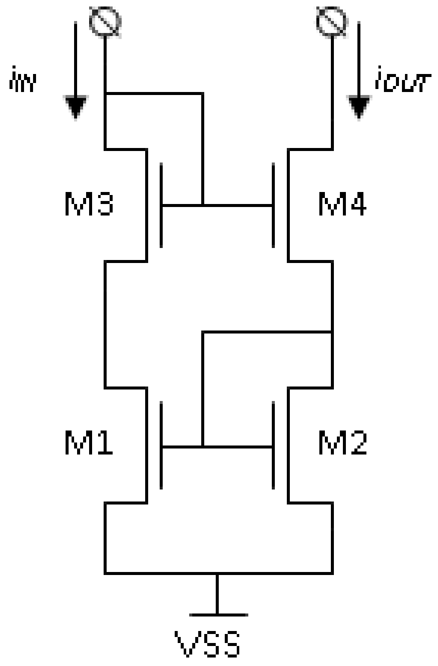
- Basic stages: differential pairs, current biasing, mirrors, etc.
- Approximate analysis for initial design
- MOSFET and Bipolar circuits

Basic Current Bias Sources



Identical devices with the same VBE have roughly the same collector current.
Approximate constant current outputs with output impedance equal to the Early resistance of the device.
All you need to know for Lab 6

Four Transistor Wilson Current Mirror in MOSFETs

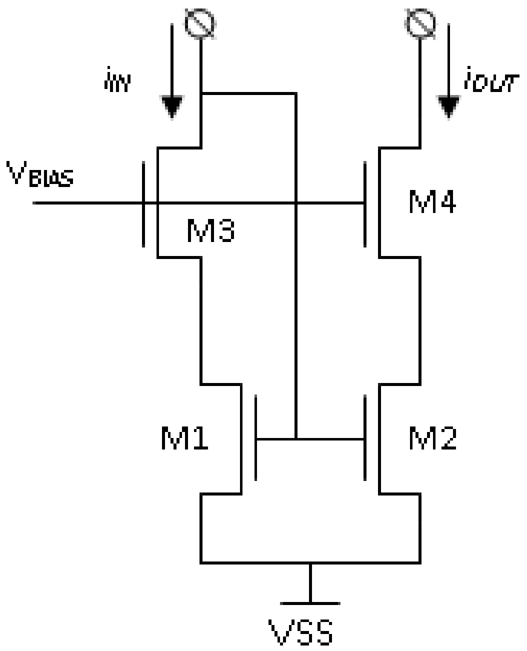


- The input current charges that node until M4 acting as a CD amplifier turns M1 on enough that ID3 balances i_{IN}
- M1 and M2 have the same VDS and VGS so the input and output currents are very well matched.
- The output impedance is improved over the value of ro4 by negative feedback through the M4 to M1 coupling. Careful analysis shows

$$z_{out} = r_{o4}\left(1 + gm_1 r_{o2}\right)$$

- The downside of this circuit is that the input voltage can never be less than 2*VGS and the output has to be greater than VGS + VOV. For circuits that need to run on 3 to 5 volt power, this leaves little room for voltage swings. (Remember VTH > .6 volts usually.)

Using a Cascode Connection to Improve a MOSFET Current Mirror



- A cascoded current mirror with M3 and M4 as the cascoding transistors. Cascoding raises the output resistance.
- The calculation is exactly the same as in the Widlar current source and $z_{out} = r_{O4}\left(1 + gm_4 r_{O2}\right)$
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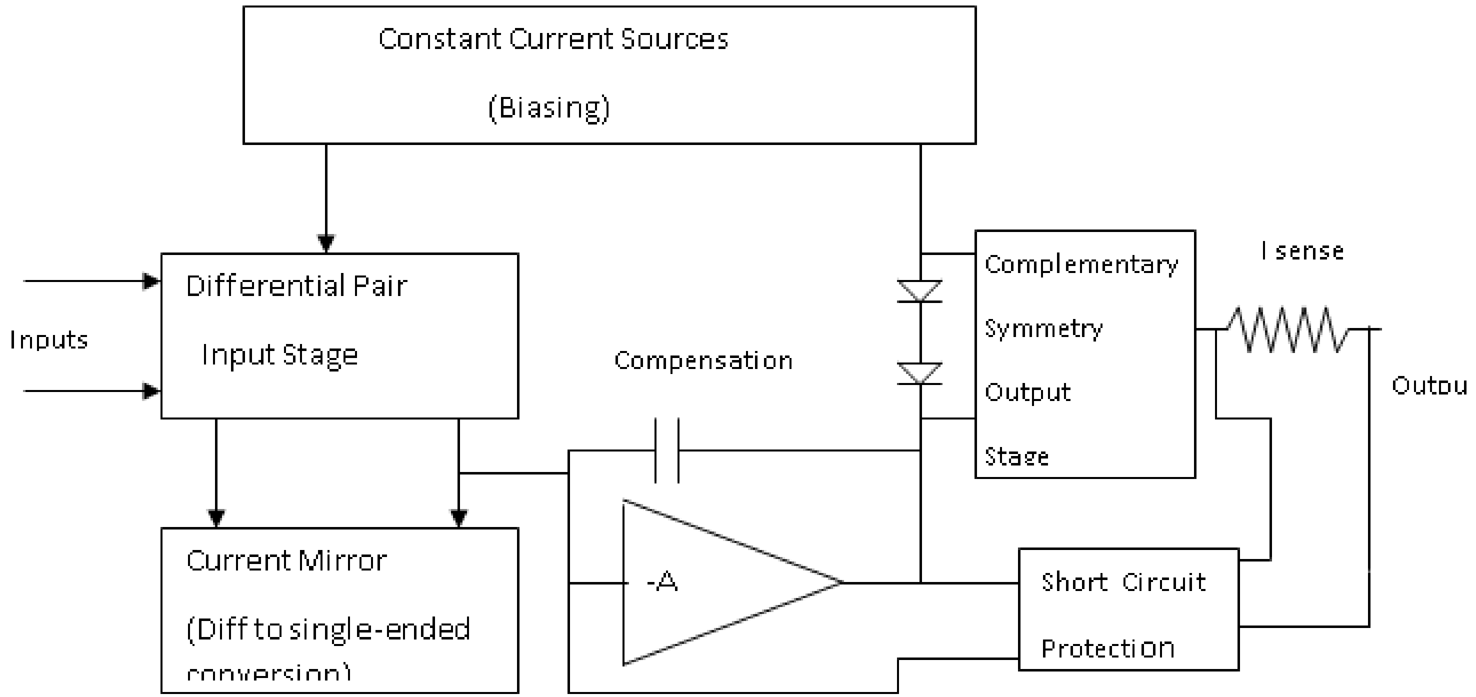
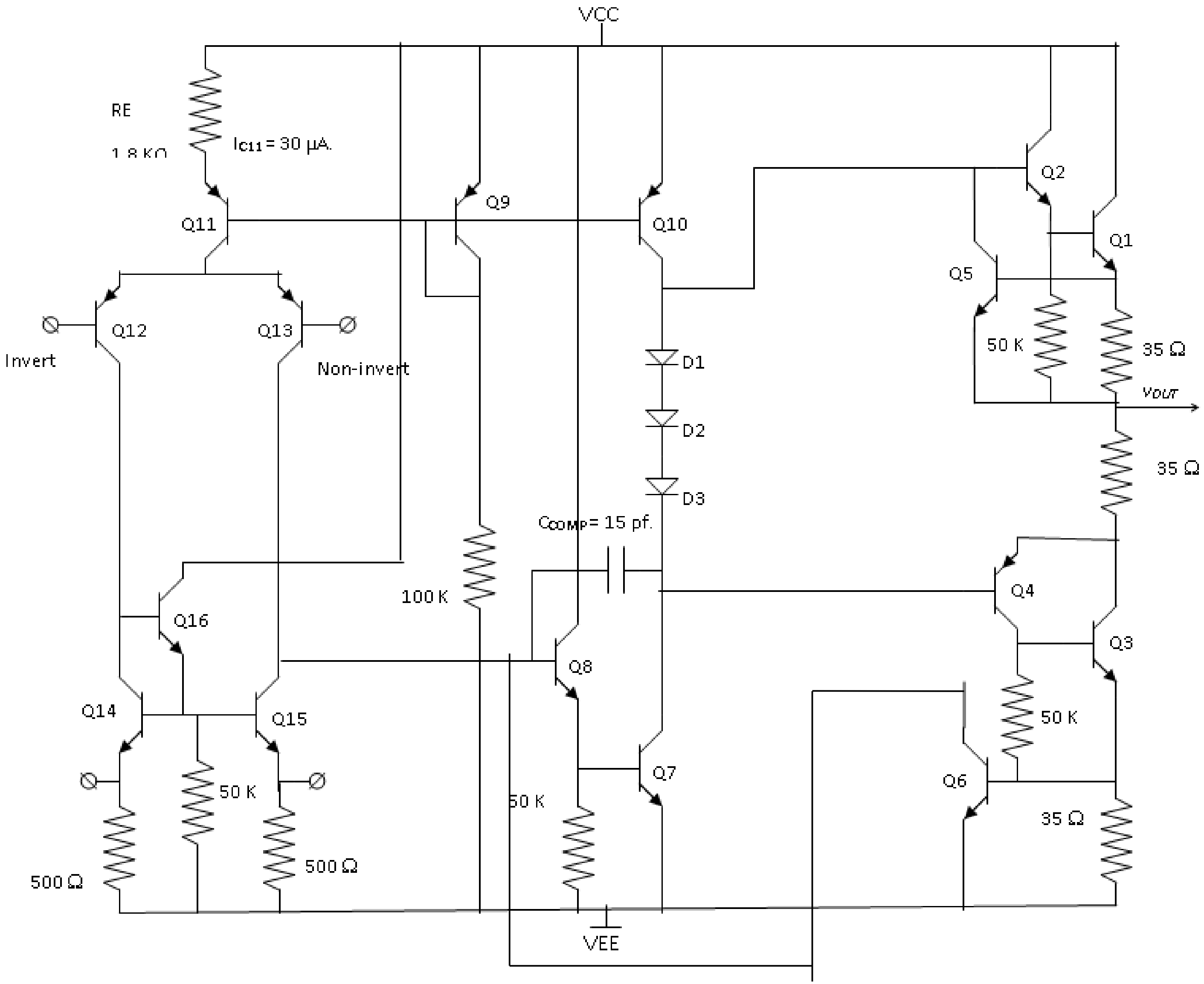
- The advantage over the Wilson configuration is that it can operate with input to V_{SS} drop of only $V_{TH} + V_{OV}$ and from output to VSS of $2V_{OV}$

A Simple (ca. 1975) Opamp – Block Diagram



Schematic Diagram

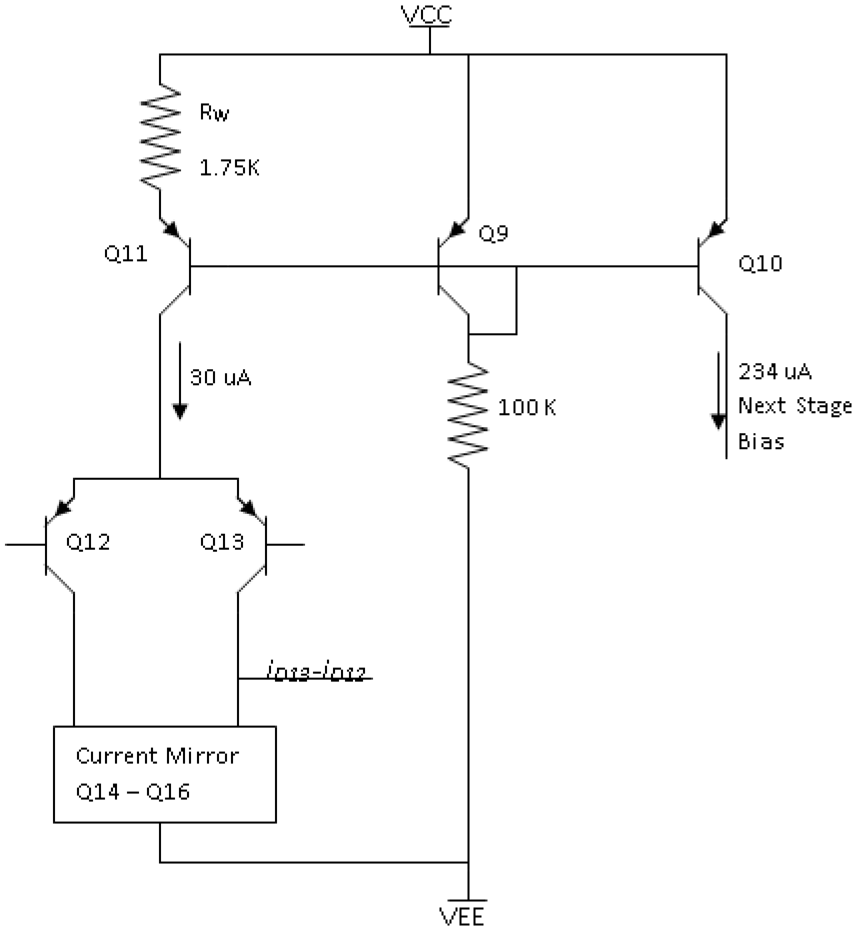


Quiescent Conditions

Device Type	V_{BE}	$h_{FE} = \beta$	V_A	V_{CESAT}
NPN	0.6 volts	100	150 volts	0.2 volts
PNP	0.6	70	30	0.3

Quiescent Currents and Transistor Model Parameters					
Transistor	IC	IB	re	ro	gm = IC/kt/q
Q7	227 ua.	2.27 ua.	113 ohm	704 kohm	8790 usie.
Q8	14.2	0.142	1.8 K	12.4 Meg.	549 usie.
Q9	227	3.35	113	132 K	8720
Q10	227	2.3	113	174 K	8720
Q11	30	0.43	860	1.3 Meg.	1150
Q12, Q13	15	0.21	1.72 K	2.7 Meg.	573
Q14, Q15	15	0.15	1.72 K	10.7 Meg.	576
Q16	12.3	0.12	2.1 K	14.2 Meg.	477

Biasing and Differential Stage



- With power supply +/- 12 V, the voltage across the 100 K resistor is about 23.4 volts and IC9 is about 234 uA.
- Want 30 uA for the tail bias of the differential pair which makes

$$R_W = \frac{kT}{qI_{C11}} \ln\left(\frac{I_{C9}}{I_{C11}}\right) = \frac{.0256}{2.34 \cdot 10^{-4}} \ln\left(\frac{234}{30}\right) = 1.75K$$

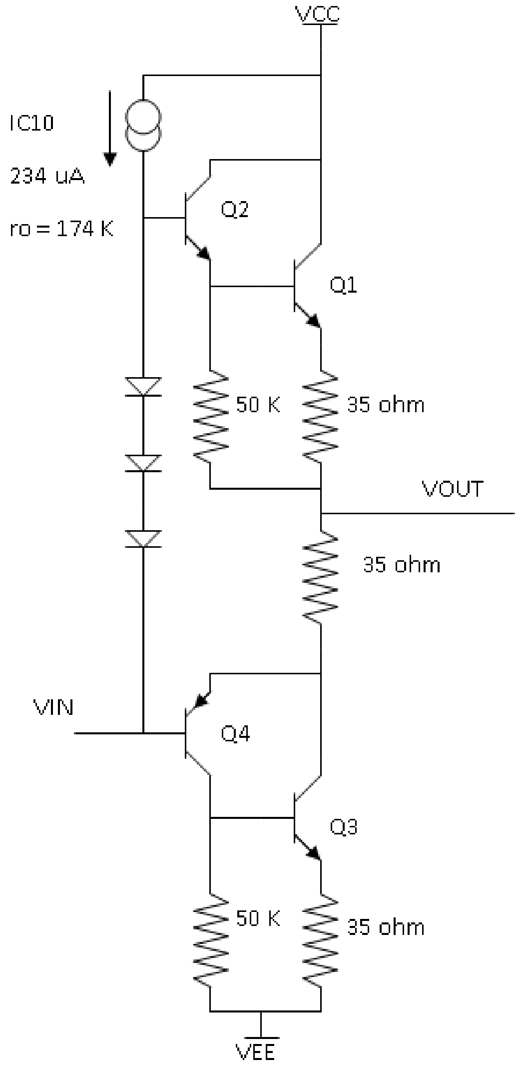
- Then the input impedance, input bias current and current gain of the stage are:

$$z_{in} = 2r_\pi = \frac{2kT}{qI_{E12}} = 242K$$

$$I_{B12} = \frac{I_{E12}}{1+\beta_{12}} = 210nA$$

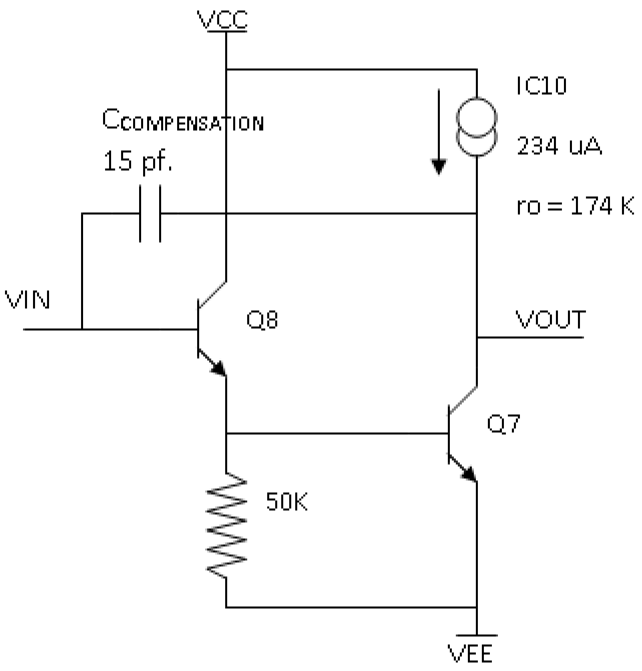
$$\frac{i_{d13} - i_{d12}}{v_{in}} = g_{m12} = 5.7 \cdot 10^{-4}\, sie.$$

Output Stage: Complementary Symmetry Buffer



- Two common collector stages tied together so that the output current can be high in either positive or negative direction.
- The 50 K resistors set a minimum current in Q2 and Q4 while assuring that Q1 and Q3 can be turned off even when hot.
- The transistor pairs are called Darlington pairs and have effectively a current gain of the product of the individual gains.
- The diodes separate the potentials on the bases of Q2 and Q4 enough to turn on Q1 and Q3 even with no output. The diodes are probably diode-connected transistors matched to Q1, Q2 and Q4.
- With a 1K load on the output (common specification) the input impedance is at least 7 Meg from the stage in parallel with 174K from the Early resistance of Q10.

Middle Stage: High Gain with Dominant Pole from Miller Compensation Capacitance



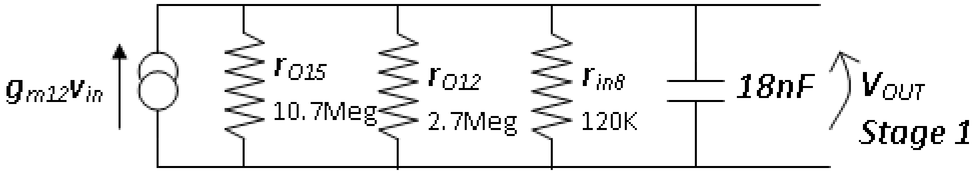
Common collector and common emitter stage combined. CC raises input impedance and CE gives a large voltage gain
The collector load of the CE stage is the Early resistance of the current source Q10 in parallel with the 7 Megohm input resistance of the CSA stage.
The gain is the product of the gains of Q7 and Q8.
The overall gain, input resistance and Miller capacitance are:

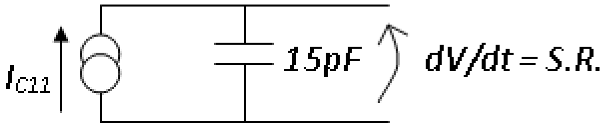
$$G = G_{Q8}G_{Q7} = \frac{(50K \parallel r_{\pi 7})}{r_{e8} + (50K \parallel r_{\pi 7})} g_{m7}\left(r_{o10} \parallel z_{inCSA}\right) = .84 \bullet 1490 = 1200$$

$$z_{in} = (1+\beta_8)\left(r_{e8} + (50K \parallel r_{\pi 7})\right) = 120K$$

$$C_{MILLER} = (1+G)C_{COMP} = 18nF$$

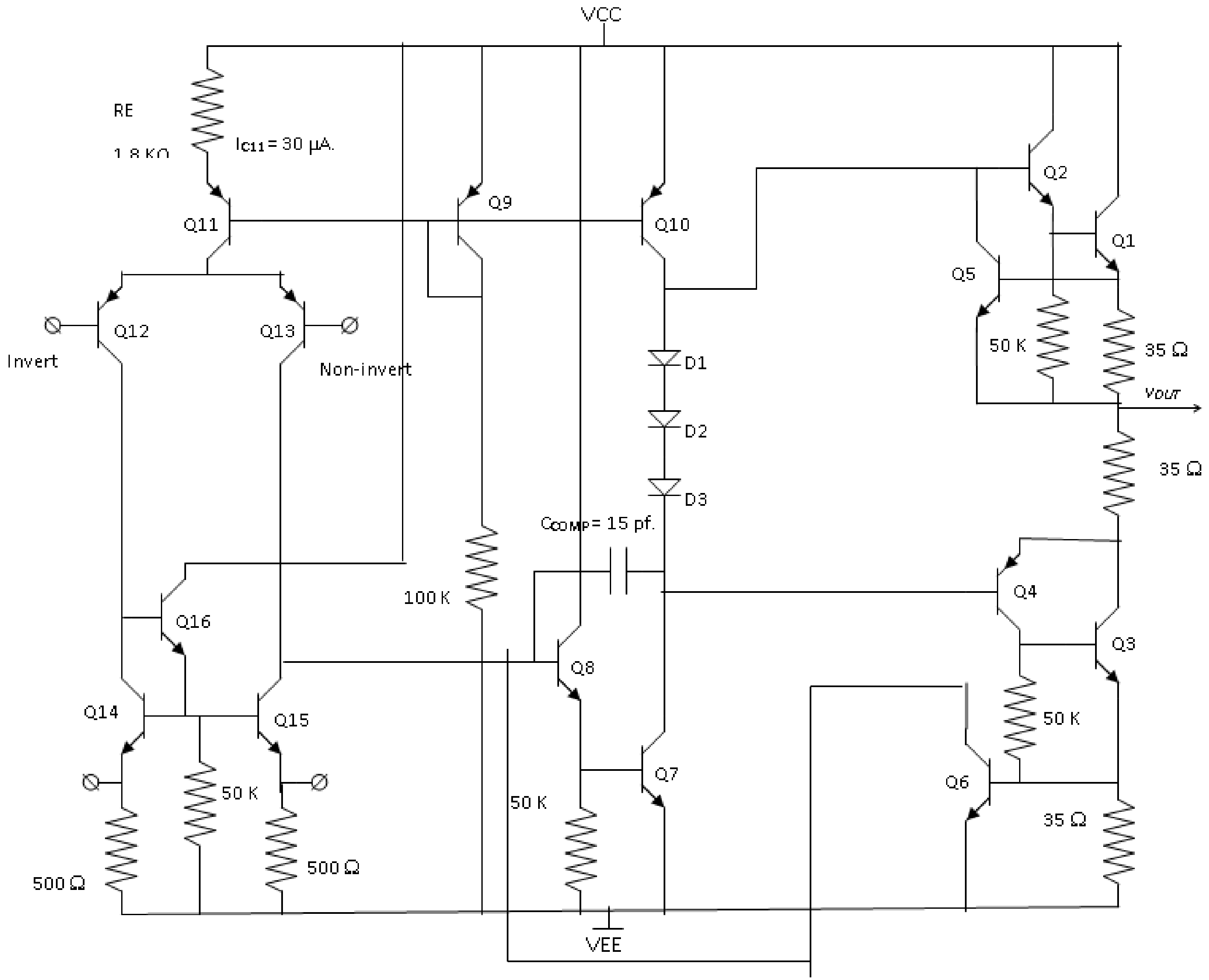
First Stage Voltage Gain & Slew Rate





- The output resistance of the first stage is the parallel combination of the Early resistance of Q13 and Q15.
- The 500 ohms in the emitter of Q15 has little effect. It is there to allow the user to adjust the input offset voltage.
- The dominant pole is from the Miller capacitance and the net resistance of the node.
- The amplifier slews as fast as possible when the first stage is overdriven by enough to route all the collector current of Q11 into the compensation capacitor. To reflect the difficulty of sufficient overdrive, the spec is sometimes set at 80 % of the absolute maximum.

Final Detail: Short-Circuit Output Protection



- When Iout > 0, Q5 senses the voltage across the 35 ohm resistor and diverts base current from Q2 to prevent the output current from exceeding VBE/35 or about 20 mA.
- When $I_{OUT} < 0$, Q6 senses the voltage across 35 ohms and diverts base current from Q8 to limit output current similarly.

Property Summary:

Bipolar Operational Amplifier Properties	
Property	Value
First Stage Gain	520
Second stage gain	1100
Overall gain	$5.7 \cdot 10^5$ 115 DB.
Dominant pole frequency	8.5 Hz
Gain-bandwidth product, f_{GBW}	4.8 MHz
Slew rate, S_R	1.6 V per μsec (80 % of max.)
Low frequency input resistance	242 Kohm
Input bias current, I_B	210 namps
Output impedance	60 ohm