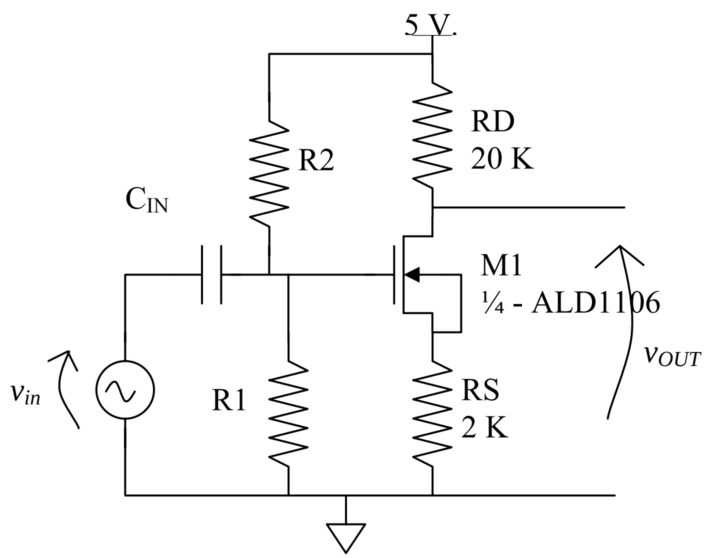
An Example of a Single-Transistor Discrete MOSFET Amplifier

Single-transistor amplifiers built from the sort of low current MOSFET devices that are used for complex analog, digital, and mixed-signal circuits are very rare because they do not perform well and the devices are not very flexible. (Power MOSFETs are used in such circuits, and Lab 3 is an example of that.)

The ALD1106 N-MOS transistor array is one of the few examples of discrete low-power MOSFETs on the market. Since I want to begin treatment of MOSFET amplifiers with something parallel in structure to what we have done with bipolar devices, here is an example of using one of the transistors from that array with resistors to form a circuit analogous to the ones I did with the 2N2222A.



Generally the ALD1106 transistors carry much less current and have lower transconductance than the 2N2222A. The choices of RD and RS reflect that fact – in our 2N2222A example, the equivalent values were 1 K and 100 ohms. When I measured an ALD1106 for lab 2 a couple of years ago, I fitted the following parameters to the data: (This fit was the basis for the recent class handout showing you the measurements graphed to help you gauge how well the equations fit the data.)

$K_N = \frac{W}{L} C_{OX} \mu_e = 9.7 \cdot 10^{-4}$ amp/volt^2 $a = .39$ $\lambda = .042$ (1/24) volt^{-1} and $V_{TH}(V_{SB} = 0)$ = .64 volts. [Note: One has to expect some manufacturing variation in the threshold voltage. A similar vintage process for custom circuits from another vendor has worst case V_{THO} listed as .35 to .59 volts.]

I now want to find the optimum drain current, the corresponding transconductance, and gain and finally the required gate bias voltage. In computing the optimum drain current, I will use γ, the ratio of i_{DMIN} to ID, as γ = 0.0 and the v_{DSMIN} = 0.5 volts. These are convenient very rough values. I am not being especially careful because the example is not very realistic. With this assumption, R_{DC} = 22 K and $|Z_{AC}|$ is also 22 K. The optimum I_D is $I_{DOPT} = \frac{V_{DD} - V_{DSMIN}}{R_{DC} + (1-\gamma)|Z_{AC}|} = \frac{5 - .5}{2 \cdot 22 \cdot 10^{+3}} = 1.02 \cdot 10^{-4}$ amps. Before I can calculate the transconductance and gain, I need to calculate $V_{GS} - V_{TH0}$ from the equation

$I_D = K_N \frac{(V_{GS} - V_{TH0})(1 + \lambda V_{DS})}{2(1+a)}$. From the optimum current, the drain-source quiescent voltage ought to be 5 - .102*22 = 2.8 volts. Upon substitution, $V_{GS} - V_{TH0} = .262$ volts. Note that I was able to use the threshold voltage for no body voltage because the circuit connected the substrate terminal of the array to the amplifier transistor source. This limits what one can do with other devices in the same package and may not always be practical. Also, if you look back in the handout in which I showed the data fit, there is a small but readily detectable error in the basic equation – it is just not as accurate a theory as one might like to have.

Given drain current and gate voltage, the transconductance is:

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2.04 \cdot 10^{-4}}{.262} = 7.8 \cdot 10^{-4} \text{ sie.}$$

The gain is $G = \frac{-g_m Z_D}{1 + g_m Z_S} = \frac{-7.8 \cdot 10^{-4} \cdot 20 \cdot 10^{+3}}{1 + 7.8 \cdot 10^{-4} \cdot 2 \cdot 10^{+3}} = -6.09$ (15.7 dB)

The gain of the corresponding bipolar circuit was -9.8, almost a full 20 dB. This lower gain is typical of long-channel MOSFETs in resitively loaded circuits because the devices have lower transconductance.

Finally, we need the DC gate voltage from which one could in principal select the bias resistors. The calculation is very simple since we have already calculated the gate-source voltage and the source to ground voltage is simply Ohm's law with the source resistor.

$$V_{GG} = V_{OV} + V_{TH0} + V_{SGND} = .262 + .64 + .204 = 1.11 \text{ volts.}$$