EN162—Analysis and Design of Electronic Circuits

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LAB MANUAL

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General Information:

Admonition: We have to ask that you be especially careful about neatness in the lab. The lab can be a difficult experience for everyone if you don't put things away when you are done. There are around 30 people in the course and that number can make quite a mess. We try to have enough parts, but we cannot accommodate your habits of dropping used materials wherever you happen to be when finished. You are not done with a lab until your breadboard is disassembled and shared parts are returned to their boxes. This is especially true of capacitors.

Introduction: There are eight labs set in this manual, two measurement labs and six labs for which you design, build, and test a circuit to meet fixed performance criteria. You must complete and document six laboratory exercises in order to get credit for the course. (Although there are eight exercises set, I will base grades on only six reports. You will not receive extra credit for extra reports.) You must do Lab 2 on the characterization of devices, but the others may be your choice from all the experiments. **THERE WILL BE NO EXCEPTIONS TO THIS POLICY**. In addition to this manual, you will receive a protoboard on which to assemble your circuits, a pair of wire strippers, and a small packet of semiconductors. Please return the breadboard and strippers at the end of the semester. Passive components and some semiconductors must be shared communally. We have labeled, multi-compartment cabinets and boxes for storage of these materials. Your cooperation in **returning parts to their proper place is absolutely necessary** for the success of the lab. Also, please do not keep components longer than necessary to do your lab. Capacitors in particular are bulky and expensive so that we do not keep enough available for everyone to have complete sets simultaneously.

The labs are done in the Hewlett Electronics Laboratory, room 196 of the new Giancarlo addition. The lab will be shared with Engineering 164 and Engineering 158 this semester. Equipment and parts for this course will be on the benches farthest from the doors. This room is open all the time during the semester. There does not have to be a lab instructor there for you to work, but such assistance will be available eighteen or so hours per week. (The hours will be announced on the class website.) You hand in lab reports in a box in the lab that is marked "EN162 Lab Reports," and they will be graded by a TA under guidelines I set.

Collaboration: Design concepts and measurement techniques may be discussed freely. Each student must build and test the circuits on his or her own protoboard. ALL lab work and all written reports must be done individually. All data reported must be your own measurements – copying data and representing it as yours is a cardinal sin among scientists of all types.

Concise, complete, polished lab reports will be rewarded with higher marks. **A TA must witness the measurements you present to prove that you have met the lab specifications.** He or she will record the fact that you did the lab on a spreadsheet and will give you an ID number to print with your data plots. While you can design, build and test your circuits without a TA if you wish, the final run of measurements does require a TA for this recording process.

Lab reports must be typeset in a word-processing program. The format for the design lab write-ups would be appropriate for an in-house report prior to a design review at an electronics firm:

I. Introduction: Discuss briefly the major goals of the lab.
II. Schematic: Show component values and, where appropriate, the measured quiescent node voltages.
III. Tables: Compare design versus measured values of all important quantities
IV. Design. Description of the design procedure and design equations. Prove that the worst-case conditions are met by design. You do not have to show the algebra by which you may have fit the equations, but you do have to show that a suitable equation set is satisfied.
V. Questions. Answer the specific questions set in the handout.

For the characterization experiments, follow the directions in the lab handout.

For each experiment there is a deadline by which your report must be turned in. These will be announced in class and posted on the class web site. Reports that are turned in after the deadline will have penalties assessed against them. The penalty may be as much as 10 % per week off! Be forewarned -- your classmates **also** like to wait until the last minute to do their work, so start early and try to get a bit ahead of the deadlines -- overcrowding in the lab will not be accepted as an excuse for turning in lab reports late. Also remember the deadlines have been set as late as practical. The labs are intended to teach, and you will have the benefit of that knowledge earlier if you do them earlier. This is particularly true of doing some of the earlier labs before the mid-semester exam, which comes a little late in the semester.

There are several general textbooks, which I will put on reserve in the Sciences Library, including older texts by Neaman and Savant. Gray and Meyer's ***Analog Integrated Circuit Design***, now in its 4th edition, is also an excellent reference for some of the later topics in the course. It is considered a classic in the field.

Several of the lab exercises, particularly Labs 4, 5 and 7 require measurements of the gain and phase shift of amplifiers as functions of frequency. We have assembled a computer driven system for automatic measurements of these quantities. You can take that data home either by emailing a file or by putting it into your Engineering account. The TA still has to witness the measurement and issue the ID number, and in doing so will check your circuit board serial number. The parameter analyzer supplies a similar set of files with data for Lab 2, and labs 1 and 6 require making plots and FFT calculations from a digital oscilloscope. All files are subject to the same checkoff system and properly formatted printouts of them are a major part of your reports.

Components: Of the various passive components in the lab, the capacitors require special comment. There are three principal types: electrolytic capacitors, film capacitors and ceramic disk capacitors. Electrolytic capacitors are made with aluminum or tantalum plates by electrolytically forming an insulating oxide on one plate. (If you don't know what the term "electrolytically" means, then please either ask me or look it up.) Since that oxide is very thin, a large capacitance per unit volume is possible. These are the only types of capacitor available for you that have values over a microfarad. Unfortunately, the chemical reaction that forms the oxide is reversible if the potential across the capacitor is of opposite polarity to the forming voltage for an appreciable length of time. The capacitors are marked for the terminal that was positive during manufacture. In use, one must be careful that the applied voltage is in the same direction. Failure to do so will ruin the capacitor and make the circuit malfunction. Aluminum electrolytics are often unsuitable for some high frequency applications because of high series inductance. Another feature of electrolytic capacitors based on aluminum is that the tolerance on their capacitance is very poor, typically -30% to +80% of nominal value.

Disk ceramic capacitors use simple blocks of a ceramic with a very high dielectric constant. All are nearly ideal capacitors to quite high frequency (10's of Megahertz). However, inexpensive types usually have poor tolerance (-20% to +50%) and very high temperature sensitivity. They are used primarily where exact values of capacitance are not critical. A common application for these is power supply bypass. There are a couple of large reels of bypass caps in the lab – you should never lack for enough.

Film capacitors have generally good performance with tolerances no worse than +/-10%. Their primary disadvantage is that they are usually physically large for a given value of capacitance. You are likely to find capacitor tolerance a significant issue only for lab 7.

Resistors: Resistors have three principal ratings: resistance in ohms, tolerance in percent, and power dissipation in watts. Most of the resistors we have in the lab can dissipate ¼ watt and have tolerances of ± 5 %. They are manufactured only with certain standard resistance values that are separated by about 10 %. We have most of these values and it usually does not make

sense to put resistors in series to come closer to calculated values. The attempt is illusory because the tolerance variation is bigger than the adjustment you would be trying to make. Resistance values are coded on the resistors with color bands. The first two bands give two significant digits of the value, the third band is a multiplier expressed as a power of 10, and the fourth band is the tolerance. The table below shows the color code. For example, red-red-orange-gold is 22 Kohms ± 5 %. Sometimes ¼ watt is not enough for a circuit application and then a physically larger resistor is required. We have some 2-watt resistors in a relatively narrow range of values anticipating a need for such a device in Lab 5.

Color	Significant Digit Value (Band 1 or 2)	Multiplier
Black	0	1
Brown	1	10
Red	2	100
Orange	3	1000
Yellow	4	10000
Green	5	100000
Blue	6	1000000
Violet	7	
Gray	8	
White	9	

Resistor Color Codes

EXPERIMENT NO. 1 - Oscilloscope Use

I hope that the structure of this experiment gets you familiar with the full range of measurements possible with a digital oscilloscope and also demonstrates some of the problems involved in their use. The first problem is that oscilloscopes can affect the circuit you are measuring so that what you see is different from how the circuit works when you are not looking at it. Such effects can be serious and while they can be minimized with the proper cables and probes, they cannot be eliminated. The second problem is a set of complications that arise from sampled data. Our Agilent scopes sample the input signal and convert it to discrete measurements that are stored in RAM memory, allowing one to read that data out into files on a PC. (The scope can also do mathematical operations including Fourier transforms on its stored data, but getting those results out is difficult. You will read some of that information from the screen but you will then do the operations over in Excel with more insight.). One must be sure that the sampling rate and voltage resolution are adequate to represent the signal you are measuring. With our new scopes, this is not usually a problem. The scopes seem so automatic and your calculations so easy that you may think finding the spectrum of a signal accurately is a piece of cake. When you do it however you will find the results subject to errors from inadequate sampling or mismatch of sampling time to the period of the waveform are significant.

We have built two circuits that generate complex, periodic waveforms roughly analogous to a slow scan television video signal. (There are two independent circuits so that more than one person can work at a time.) You are to measure several features of the signal including its shape, its fundamental period, its vulnerability to corruption by capacitive loading, its relationship to a second, "synchronizing" signal, and finally its Fourier spectrum. We have two types of probe for connecting the scopes to the generator. One is a “10X” attenuator probe that reduces the signal amplitude by a factor of 10 before it reaches the scope. The other probe, called a 1X probe, passes the signal without attenuation. The difference is not only the attenuation but also the amount of capacitance that the circuit “sees” when you connect the probe. You will find that the tradeoff for the reduced gain of the 10X probe is that its lower input capacitance affects the circuit less. I have tried to design the experiment to lead you to think about why this is the case.

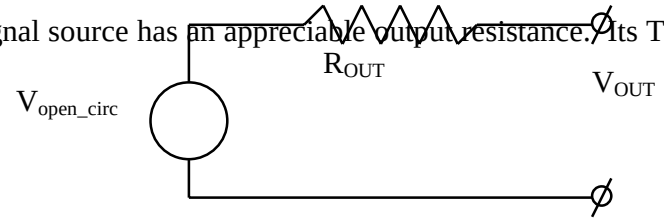
Measurements:

1 There is synchronization or “synch” pulse output available from a BNC connector on the waveform generator. Using a coaxial cable, connect that signal to one channel of the scope and set the scope for a stable measurement. With the scope cursor controls and digital readout, determine the maximum and minimum voltages (be careful about offset), the period, and the pulse width at the 1.5-volt level. (The 1.5-volt reference

level is standard for 3.3-volt CMOS logic and the older 5-volt TTL logic. Do not confuse the reference voltage level for time measurements with the pulse amplitude.)

2 Now connect the synch signal to the "Ext, Trigger" input of the scope's time base and set the scope to trigger on the falling edge of this signal, *i.e.*, use external synch mode with negative slope and appropriate level. Connect the actual waveform, available only as a terminal on the protoboard itself, to a vertical input of the scope (*i.e.*, Ch1 or Ch2), setting the vertical sensitivity and horizontal time base to display between one and two periods of the signal with as large a height as can be set without clipping. Measure the period and the maximum and minimum amplitudes.

3 The signal source has an appreciable output resistance. Its Thevenin equivalent circuit is:



Determine R_{out} by loading the circuit with a suitable empirically-determined resistor and inferring the value of R_{out} from the change in output voltage. WARNING: think carefully and even experiment to determine which probe to use for this measurement.

4 On the PC connected to your oscilloscope, open a new EXCEL spreadsheet to collect the data for your write-up. Capture a trace of the waveform measured with the 10X probe taking 2000 samples of data. Leaving the scope controls unchanged, make this measurement again connecting the signal with just the 1X probe, and again one final time with both probes connected to the generator. (Obviously, you still only need one trace for this last measurement as both probes see the same signal.) Each captured waveform will appear in your workbook as a separate sheet; you probably want to annotate each sheet with what measurement it contains.) Notice that the waveform changes shape as you change probe! This is the effect on the actual signal of connecting it to the scope and it is non-negligible. Be sure to record the horizontal time base, the vertical sensitivity, and the screen size in cm for both axes, as you will need that data for your calculations.

5 A change of shape in a signal implies a change in its spectrum. Measure the frequency spectrum of the signal from first the 10X probe and then from the 1X probe as follows. (**Do NOT** have both probes connected to the source at the same time!) Change the

scope time base so that many cycles of the waveform are displayed (try 100 μs per division, for example). Set up a fast Fourier transform (FFT) of the waveform using the scope's "Math" menu. Try a span of 500 kHz and a center frequency of 250 kHz.

What are the frequencies of the peaks in the spectrum, and how do they relate to the fundamental frequency measured in part (1)?

Note the sampling rate that is indicated on the scope display. Compute how many samples are taken during the displayed time interval of the waveform. Watch what happens to the spectrum display and the sample rate as the time base control is changed. Also compare the spectra obtained with a "Hanning" window versus a "flattop" window. These windows are specific ways of weighting the samples at the ends of the time interval in order to minimize the effects of having a finite sample interval. The Hanning window is preferred for accurate frequency measurements, while the flattop window is used for amplitude measurements.

Set the flattop window and a sample/sample rate that gives good resolution of the peaks. Set the channel sensitivity so that the waveform occupies most of the screen without any clipping. Note these settings for reference later. Measure the amplitudes of the first 5 harmonics relative to the fundamental in dB for the waveforms from both probes.

6 Capture in EXCEL the same traces you analyzed with the scope's FFT module so that the data is available to analyze yourself.

7 Measure the length of the probe cables with a ruler. (You will use this to find their capacitance per foot.) Record the values of resistance and capacitance marked on both the 10X and 1X probes and the input of the oscilloscope. These values are the equivalent impedance seen at the probe or scope input expressed as a parallel combination of a resistor and capacitor. For the probes, the circuits are for the probe and scope together. They do not necessarily correspond to any actual physical components.

8 I do not wish to offer an occasion of sin and take a very dim view of copied data. Therefore, you must have your work signed by the TA in one of two ways, depending on how fast I get some software to work. Either the TA will initial a graph printed out from your EXCEL file in the lab or he will paste a software-generated ID number unique to you into your spreadsheet. If the latter, you must print that on one of the graphs in your write-up, as discussed below.

Guidelines, Issues, and Questions for Write-Ups:

Please begin your write-up with a short introduction that talks of the features of measurements and spectra that seemed important to you from this lab. Then use the following list as guidance for the rest of the report. (Doing so will make it easier to write and easier for us to grade.)

1. Tabulate your synch pulse measurements.

2. Show the measurements and calculation by which you found the output resistance of the source.

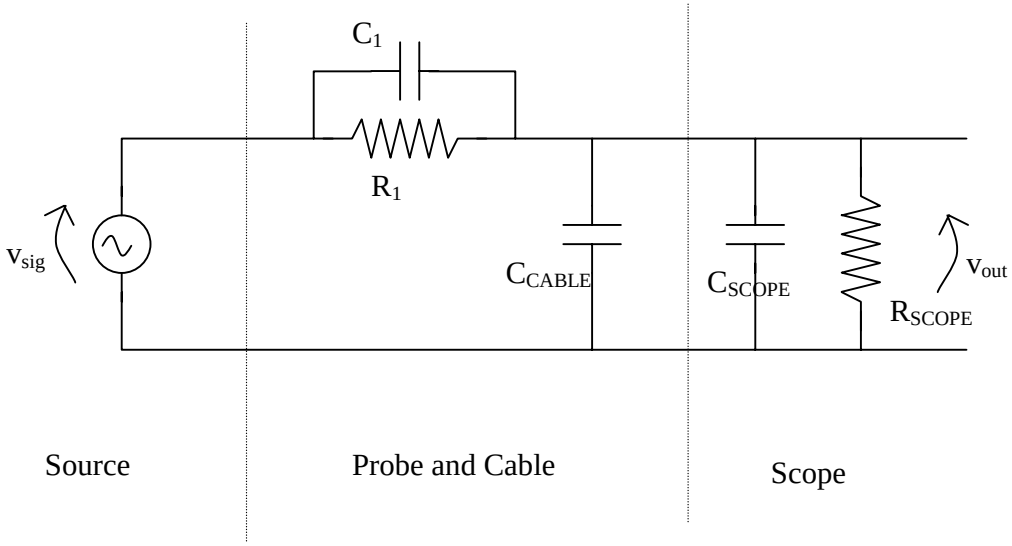
3. Analyze the operation of the 10X probe. The equivalent circuit of the 10X probe is shown below. The components R_1 and C_1 are actual physical elements in the probe body. The capacitor C_{CABLE} represents the cable capacitance. Let C_T be the total capacitance of cable and scope given by $C_T = C_{CABLE} + C_{SCOPE}$. Please do the following for this circuit:

   - Derive the transfer function of this system and show that it is independent of frequency if $C_T/C_1 = R_1/R_{SCOPE}$.

   - The real probe is designed and adjusted to meet this constraint. (There is a screwdriver adjustment of C_{CABLE}, an adjustable lumped capacitor in parallel with it, that we try to keep set properly.) Prove that this condition also makes the input impedance equivalent to a single resistor and capacitor in parallel. The probe is marked with **the values of these equivalent components** rather than any of the values of the actual components: R_1, C_1, R_{SCOPE}, C_{SCOPE} or C_{CABLE}. The scope itself is marked with its input resistance (1 megohm) and capacitance.

   - Find the values of the real components of the probe and scope system (R_1, C_1, C_{SCOPE} and C_{CABLE}) from your theory and measurements.

4. Typical coaxial cable usually has about 30 pf of capacitance per foot. How does that compare to your estimate of the capacitances per foot of the two probe cables? What is the total capacitance of the 1X probe, including both its cable and the scope connection?



Equivalent Circuit for a 10X Probe Connected to an Oscilloscope

5. Using your EXCEL results, plot the data you took of the single cycle traces. Overlay the data taken with the 10X probe, the 1X probe, and both probes on the same graph. Distinguish the traces by color, line type or small vertical offset. Try to design the presentation so that the change in signal features is clear as the load capacitance increases. Comment qualitatively as to why the curves change. I had you synchronize the horizontal sweep using the "External" input primarily for this part of the measurement. What advantage for this plot does such synchronization have?

6. Look at your raw data and determine what the minimum voltage step is that the scope stored, that is, what is the vertical resolution of the scope on this scale. How many such steps are in your trace? How many fill the screen? How many bits per sample does the scope store?

7. Show that output impedance of the generator, R_0, in conjunction with the scope probe forms a low pass filter and compute the cutoffs for the three cases you just plotted. How do those frequencies compare to the fundamental frequency of the waveform?

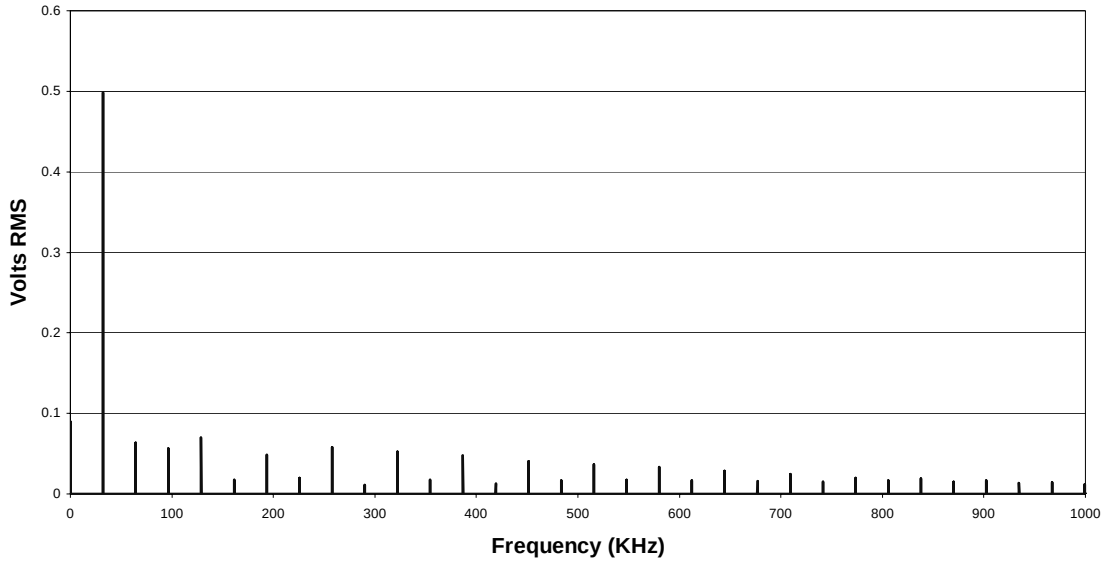
8. From the measurements you took of the amplitudes of the first five harmonics in section 5 of the measurements, what is the lowest harmonic frequency at which the 1X

measurements were attenuated by 3 DB (a factor of $1/\sqrt{2}$) or more than the 10X ones? Is this consistent with the calculations of the cutoff frequencies of your probe setups?

9. Prepare FFT spectra from the data you took over long traces with the 10X and 1X probes in section 6 of the measurements. You can do this within EXCEL using the Fourier Analysis tool that is part of the Data Analysis add-in or you can import the data into MATLAB. Because that transform is done with an FFT – Fast Fourier Transform – algorithm, the number of data points must be an integer power of 2 – in your case 2048 points. You may pad the waveform with zeros or repeat a portion of the waveform. The transform produces 2048 complex numbers, but because the input is real, only the first 1024 contain unique data. The rest contain duplicate data. You are interested in the magnitude spectrum and can use the IMABS() worksheet function to show only the magnitude of a complex number. Scale your results so that your plot will give the RMS value of each frequency component. (Scaling is probably by $\sqrt{2}/2048$.) The lowest FFT component is DC and is not reliable because it may be changed with the scope's vertical offset control. You may ignore it. The remaining frequencies are separated by constant steps given by $1/T$ where T is the total time interval of the original measurements. There are a total of $N/2$ such frequencies where N is the number of points in the set. For example, a trace taken with 2000 samples at 100 μsec per cm horizontal scale, will have a frequency step size of 1/(10cm*100usec/cm*2048/2000) = 976 Hz. Its data will span frequencies to 1 MHz. Plot the 10X and 1X data.

10. Because the waveform is known to be perfectly periodic, the proper spectrum is given by a Fourier series. I have used sine and cosine coefficient calculations to derive the spectrum quite accurately from the single cycle data taken with the 10X probe. The graph below shows my results and the data on which it is based is available on the class web site. Overlay the 10X probe spectrum you calculated on a single graph along with my results. Comment on the accuracy of your calculation with respect to both harmonic frequencies and amplitudes.

11. As a final test of your powers of observation, here is a challenge question. The scope automatically compensates its gain for whether you use a 10X or a 1X probe. (It does not work for any other probe range – there are, for example, 100X probes for high voltage that do not display correctly.) How does the scope know what probe you are using?



Magnitudes of the Harmonics of the Lab 1 Waveform Calculated from its Fourier Series

EXPERIMENT NO. 2 - Characterization of a Diode and a Transistor

The object of this experiment is to measure of some of the device characteristics discussed in class for a typical diode and for typical bipolar and MOSFET transistors. The diode is a 1N4003 diode designed for rectifier service with a nominal breakdown rating of 200 volts and an average forward current rating of 750 ma. The bipolar transistor is the 2N3904 a low power transistor with a V_{CB0} rating of 30 volts, a maximum collector current rating of 150 ma and a power dissipation rating of 0.3 watt maximum. The MOSFET is one of four found on an integrated transistor array from Advanced Linear Devices, their ALD1106PB. Full data sheets on these devices are on the class website and I have put extracts in an Appendix to this manual. The MOSFET is not something we will have talked about before you do the lab. Before the class is over, I hope to have you compare this data to the simulation models from the SPICE program. (The MOSFET measurement will also give you the basic idea of the device used in lab 3.)

Current and voltage measurements are done with one of two instruments, a Hewlett Packard parameter analyzer for low voltages and currents and a much older Tektronix Model 575 curve tracer for higher voltages or currents. Data from the analyzer can be captured on the PC that controls it and you can email those files to yourself. The software for the analyzer is still evolving and the TAs will have to explain its condition and operation to you as soon as I tell them. (It is actually in pretty good shape now and I hope to finish it soon.) Most of the measurements will be made with the analyzer. Instructions for the curve tracer are included with this write-up. As much as possible we will try to let you do the measurement yourself.

1. Measure the capacitance of a reverse biased diode using our Boonton™ capacitance meter. This instrument applies a small 1 MHz signal to one side of the unit under test and senses the current in other lead, while that lead is effectively grounded. Readout is by a panel meter graduated directly in picofarads. Be sure the meter is zeroed before putting in your diode and make use of the mirror scale to minimize parallax. Two terminals on the back of the meter, labeled "bias," allow one to apply a DC voltage to the unit under test while the capacitance is being measured. There is a high voltage power supply available to give bias voltages over 100 volts, but its minimum output is about 6 volts. Both you and the meter need protection from this voltage and I have an appropriate network for that purpose connected to the back of the meter already. Please do not disturb it.

There is a second supply to use for bias in the range from 0.2 volts forward to 15 volts reverse. The meter on the high voltage supply is not very accurate and the protection network I have on the meter reduces the voltage at the diode. Therefore, use a separate digital voltmeter to measure the voltage being supplied to the Boonton and to determine the polarity of the bias on the diode. (Remember you are interested in the reverse bias capaci-

tance.) To avoid problems with including the capacitance of the meter with that of the diode, connect the DVM to the bias terminals on the back of the meter. You can use the meter across the diode terminals to determine polarity before connecting the diode. Measure and plot the reverse bias capacitance of the 1N4003 (or equivalent) diode from zero to 100 volts reverse with enough points to determine whether it approximately follows the expected curve for an abrupt junction:

$$C = C_0 + \frac{C_{J0}}{\sqrt{1 - V / V_{BI}}}$$

where C_O is a fixed capacitance due to the case of the diode, C_{J0} is the junction capacitance at zero bias, and V_{BI} is the junction built-in potential. Because this equation varies more rapidly near zero volts, you will have to take points more closely spaced near zero than you do for higher voltages. V_{BI} must be less than the bandgap potential (1.18 volts for silicon) and is likely to be more than .7 volts. Using Excel or a math package, find the best estimates for C_0, C_{J0}, and V_{BI}. Then overlay your data with a theoretical plot based on these estimates.

2. Using the semiconductor parameter analyzer, measure the forward current of the 1N4003 as a function of bias zero volts until the current reaches 100 ma. Does this curve fit a relation of the form:

$$I_D \propto I_S e^{qV/nkT}$$

where n is a constant? What value of n fits best? Over what range of V and I_D is this fit to within 20 %? (You can take this data home as a file for later processing.)

3. Again using the semiconductor parameter analyzer, make a Gummel plot for your 2N3904 transistor with V_{CE} = 3 volts, keeping I_C under 100 ma. Begin with V_{BE} at zero volts so that any heating effects will affect only the high current measurements. (A Gummel plot has overlaid curves of I_C and I_B as functions of V_{BE} at a fixed, usually low value of V_{CE}. The curves are drawn on a log-linear scale so that a wide range of current can be shown.) From this plot, make a sketch of h_{FE} versus I_C. Over what range and with what value of n is I_C proportional to exp(qV/nkT)? Does I_B behave the same way?

4. Still with the parameter analyzer, measure h_{fe} for the 2N3904 at collector currents of 5μamp, 0.5 ma, 10 ma, and 80 ma with V_{CE} = 5 volts. Note that h_{fe} is the differential gain $\Delta I_C/\Delta I_B$ that you approximate as $\Delta I_C / \Delta I_B$ where the incremental currents are their changes for one or two steps of the base current. It may not be very different from h_{FE}.

5. Measure I_C as a function of V_{CE} from 0 to 10 volts using I_B as a parameter, taking enough data to be able to draw one of the sets of curves we use in class to show amplifier operation. Cover the range of I_C up to 10ma with 5 – 7 base current curves. Plot this in your report and derive from it the Early voltage at $I_C \approx 5$ ma and V_{CESAT} at the same current.

6. In principle and in practice the emitter and collector of a bipolar transistor can be interchanged, and the device will still show appreciable common emitter current gain. In this configuration, the old collector is, of course, the new emitter. This is called "reverse operation" of the transistor, and the current gain is called h_{RE} or β_R. Measure this quantity for I_C = 1 ma. How does this compare to h_{FE} as derived from your Gummel plot? Calculate the corresponding common base gains α_F and α_R? Why are the relative magnitudes of h_{FE} and h_{RE} what they are?

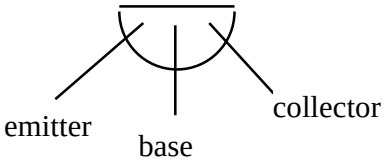
7. For the MOSFET using the parameter analyzer, measure I_D as a function of V_{GS} for a fixed drain voltage of 4.0 volts and a gate voltage from 0.3 to 2 volts. Use a logarithmic current scale so you see the full drain current behavior. Set the analyzer current limit for the drain current at 10 ma. Plot this data on the same log scale in your report. Replot it on linear axes as $\sqrt{I_D}$ versus V_{GS}.

8. Define the breakdown voltage of a junction to be the voltage at which the reverse leakage current rises to 10 μamp. Using the curve tracer, determine the breakdown voltage of a 1N4003 and of the collector-base (V_{CB0}) and emitter base (V_{EB0}) junctions of a 2N3904. (**NOTE**: Any diode in the 1N4001 to 1N4007 family is suitable for this measurement. The curve tracer has a maximum supply voltage of 200V. **This may not be sufficient to cause breakdown**, in which case, report an approximate upper limit to the leakage current at 200V instead.) Why do the two junction breakdown voltages for the 2N3904 have such different values?

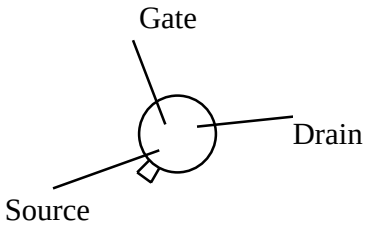
NOTES:

1. Please try to avoid damaging components by limiting reverse, leakage current to 10 μamp. None of these junctions are designed with sufficient thermal dissipation to serve as a zener diode.

2. Here are the base diagrams (bottom view) for the 2N3904 and the MOSFETs:

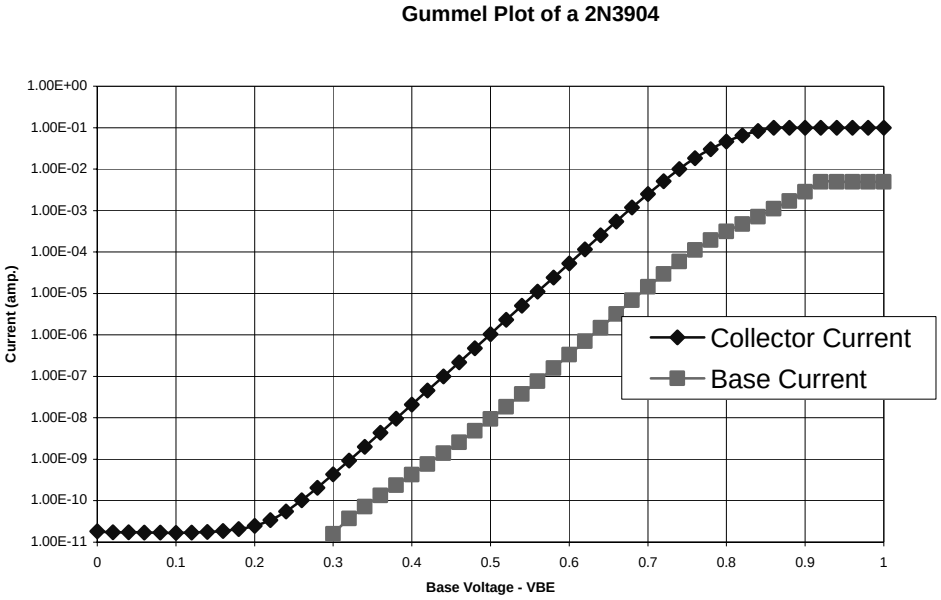


2N3904 - bottom view



TO-18 MOSFET - bottom

Quad MOSFET array



Example of a Gummel Plot

USE OF THE TEKTRONIX 575 TRANSISTOR CURVE TRACER

The following is a brief description of the procedure that should be followed to find the characteristics of a typical transistor.

STEP 1: Study the accompanying Figures 1 and 2 until you understand how the tracer works and until you can associate each control on the instrument with the portion of the system it affects. It may take you some time to fully understand it, and actually trying to use the instrument may help clarify its operation.

STEP 2: Turn the curve tracer on. While the tracer is warming up, set the vertical and horizontal scale controls for appropriate ranges of collector current and collector voltage. These controls set the sensitivity of the display and are analogous to the sensitivity controls of an oscilloscope. Normally one knows in advance what range of current and voltage is of interest. The voltage or current per division is set so that full scale of 10 divisions encompasses the range of interest.

STEP 3: Even before putting a transistor into the test socket set the "Peak Volts Range" and "Dissipation Limiting Resistance" knobs to limit the voltage and power available to the device. Doing so will reduce the changes of burning anything out. The peak volts should be kept below the breakdown rating of the device. There is a graph on the top of the 575, which shows the relation between power, peak volts and resistance. Use this to select a resistance to limit the power. Small plastic transistors generally withstand about .36 watt while larger metal ones withstand about .6 watt. Power transistors without heat sinks may absorb 1 watt but over 1 watt is usually possible only with heat sinks.

STEP 4: For common emitter measurements, set **BOTH** polarity knobs on -(minus) for PNP and + (plus) for NPN devices

STEP 5: Turn the base generator "Step Selector" knob to a current range about $1/50^{th}$ of the vertical current sensitivity range. Set the step generator flick switch to "repetitive" and the "steps per family" control to mid-range.

STEP 6: Check that the switch next to the test sockets is in the "emitter grounded" position.

STEP 7: Place your transistor in one of the test sockets with collector, base and emitter leads in the proper slots. You may need to consult a data sheet to find the ap-

propriate connections. Turn the transistor on by flicking the selector switch toward the test socket.

STEP 8: Use the position knobs to shift your beam. A PNP transistor should have the beam in the upper right-hand corner, while an NPN transistor should have it in the lower left.

STEP 9: Adjust the "Peak Volts" control to obtain a trace of the collector characteristics. Then set focus, intensity, astigmatism and scale illumination to suit your personal taste.

STEP 10: If you do not obtain a trace recheck these steps, particularly Steps 4 and 5. It is always possible that your transistor is burned out, and you may want to try another. Even when you do get a trace you may want to make slight adjustments to the "Step Selector" and "Dissipation Limiting Resistor" to have the trace fill the screen conveniently.

MISCELLANEOUS REMARKS

The curve tracer can be used to make common base measurements by interchanging the base and emitter leads and using the base generator to drive the emitter. The interchange of leads can be made with the "base grounded" knob for transistors in one of the sockets. For transistors attached to the binding posts, it is necessary to interchange the actual wires. When using the base step generator to drive the emitter, one has to reverse the polarity of the generator (+ for PNP, - for NPN) and to increase the current level to the same range as the vertical sensitivity.

The curve tracer can also be used to measure diodes, JFETs and MOSFETs Diodes connect between the emitter and collector terminals, and the base generator is ignored. MOSFETs connect drain to collector terminal, gate to base and source to emitter. Then the step generator is set to **voltage** steps rather than current steps. It is important to use a base **current** drive for bipolar transistors since collector current varies so rapidly with base voltage, and to use a **voltage** drive on the gates of FETs since they are voltage controlled devices whose gates are not supposed to draw current and can be damaged if such gate current flows.

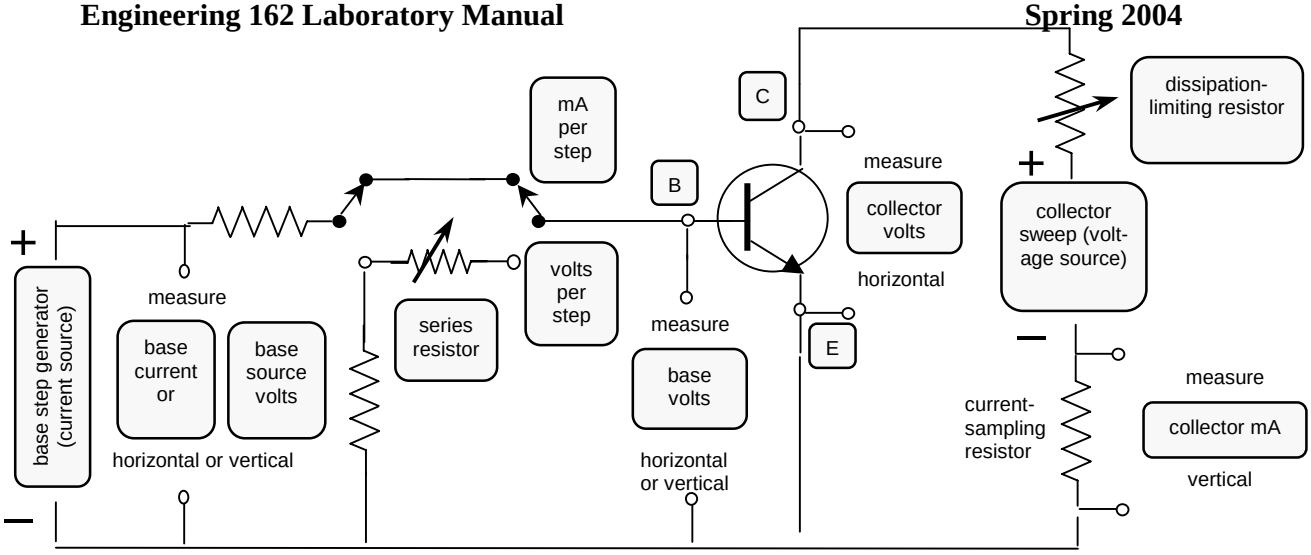


Figure 1. Functional block diagram for the Type 575 curve tracer, shown with an *npn* transistor under test. This instrument places the transistor in a common-emitter circuit with a continuous sweep for the collector voltage and a base current that remains constant during one (or one-half) of a collector sweep but then changes by a fixed amount. Every call-out in a shaded box refers to a corresponding label on the front of the instrument. The up position of the switch gives constant base current steps while the down position gives constant voltage steps through a series resistor.

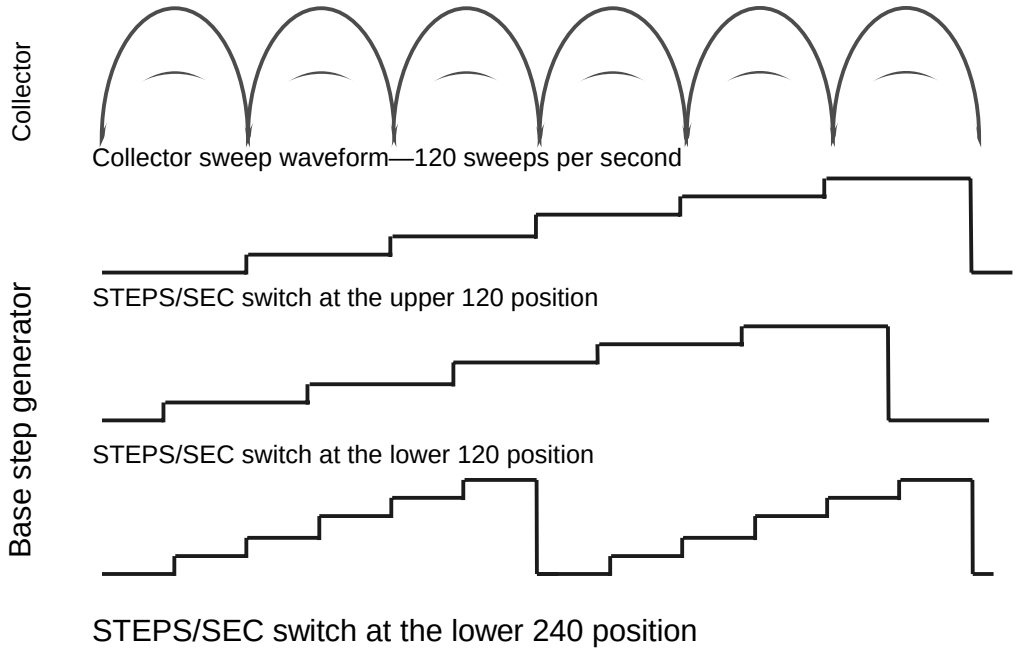


Figure 2. Waveforms of the collector sweep generator (top) and the base step generator (bottom three). The number of base steps is selectable.

EXPERIMENT NO. 3 - Half a Cheap Stereo

This experiment introduces the idea of biasing for linear amplification. It is intended primarily to introduce the capabilities of FETs (Field Effect Transistors), to remind you of the rules for Q point selection in circuits that use matching transformers, and to give you a chance to think about simple RC circuits. Build the circuit shown below, designing the required RC network and measuring its performance. It has a transformer to drive a low-resistance speaker with an amplifier made from a single MOSFET. Using the primary taps marked 2.5 and 5 watts and the C and 8 Ω secondary connections to the speaker will result in a transformer primary with a primary magnetizing inductance of 0.5 H, a turns ratio 4.6:1 from primary to secondary, and a primary wire resistance of 30 ohms. (By comparison, the secondary resistance is negligible.) The speaker acts roughly as an 8 Ω resistance.

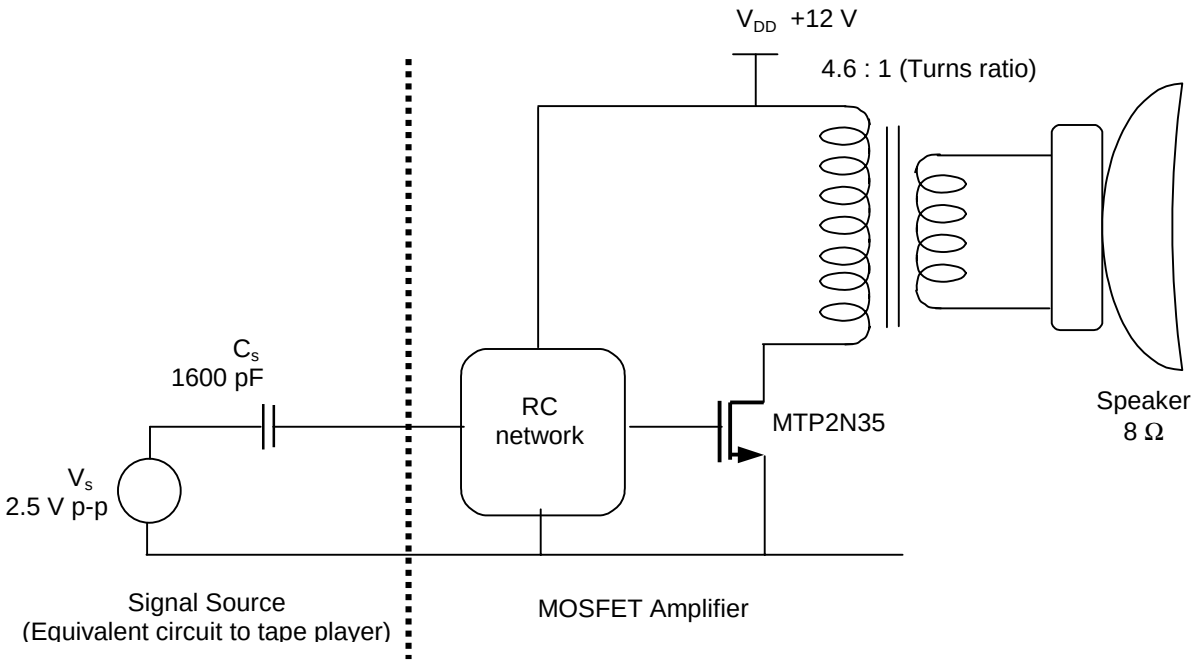
There are also a number of MTP2N35 (Motorola) power MOS field effect transistors or similar devices in the lab that are already mounted on heat sinks with extension wires on their leads. These wires let you plug the transistor into the rest of the circuit on your protoboard. Unmounted transistors are intended only as backups. The pin connections and basic ratings of the MOSFETs are shown below. The gate bias voltage in operation is usually about 3.5 V but may vary up or down by several tenths of a volt. You may have to adjust your circuit to get the correct (optimum!) quiescent current.

There is a tape player in the lab that we have modified for use as a signal source by adding an output cable and limiting impedance. It is equivalent to a 2.5 volts peak-to-peak signal with a source impedance equivalent to 1600 pf capacitor. The figure below shows the connection of the MOSFET to the coupling transformer and speaker. Designing an RC network to connect the tape player to the MOSFET and to provide MOSFET bias is part of your job. It should take either three resistors and one capacitor or two resistors and two capacitors. (I rather like the latter circuit for aesthetic reasons. At least, you should know what the two choices are.) The MOSFET gate can be considered an open circuit for this design. The signal voltage from the tape player at full volume is somewhat bigger than the MOSFET can handle without distortion. To fix this problem, your RC network should attenuate the signal by a ratio of 5:1. In your write-up, you are expected to show this is attenuation is realized by design. The low frequency cutoff associated with the capacitor of the signal source (1600 pf equivalent source impedance) has to be placed at 50 Hz.

Select the bias from the network to make the quiescent current optimal for maximum possible output. The choice of an appropriate value for the ratio of the minimum dynamic drain current to its quiescent value is up to you. Determining the bias voltage that corresponds to the optimum drain current may be done empirically. You may use the curve tracer or parameter analyzer to determine an appropriate value of gate voltage V_{GS} or you may use trial and error to

find the right I_{DS}. This is the one lab that allows a cut-and-try approach of adjusting one resistor value while measuring the quiescent drain current I_{DS}. Note that the selection, adjustment, and confirmation of I_{DS} are an important part of the basis on which your report will be graded.

In your report, you should show data for the quiescent gate and drain voltages, and the quiescent drain current. You may measure the latter by inserting a 10-ohm resistor in series with the power supply VDD line and measuring the voltage drop across it with a digital voltmeter. If you wish, you may use this same method in setting the drain current value. In addition to a qualitative evaluation of the functioning of the circuit, you should indicate how you designed your RC network. Also calculate the expected low frequency cutoff due to the transformer magnetizing inductance.



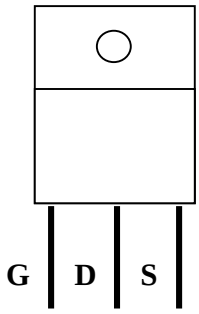
The circuit has been designed without a volume control because, as nearly as I can tell, such controls are of no interest to anyone under thirty. If, however, you are amused by the idea, you might, optionally, add one. The challenge will be to prevent the volume control from changing the bias point. I will try to remember to have a 1-megohm potentiometer in the lab for the purpose. If you are not satisfied with the program material we have supplied, feel free to try some of your own.

NOTE: MOSFETs are discussed in chapter 4 of Sedra and Smith. If you have done lab 2, you will already have some idea of how the drain current of a MOSFET is controlled by the voltage from gate to source. We will discuss MOSFETs in class near the end of March. You do not need to know much about them to do the lab since the lab is largely independent of the details of the device! Field effect transistors differ from BJTs in a couple of ways that are important here and which make the lab easier. The gate of an FET is its control terminal in the same sense as the base of a BJT is for it. However, the gate draws no steady DC or bias current at all. Superficially the drain current vs. drain voltage curves with V_{GS} as the curve parameter look just like those of a BJT. The main difference besides the lack of gate current is that the gate voltage for a given drain current is larger than V_{BE} for a BJT and tends to be less repeatable from unit to unit. Interestingly nothing in the consideration of the "best" Q-point for a single stage amplifier depends on the differences in the device types.

MTP2N35: *n*-channel enhancement-mode MOSFET made by the DMOS (diffused MOS) process

Maximum V_{DS}	350 V
Maximum I_{DS}	2 A
Maximum P	40 W (on heatsink with ambient temperature 25 °C)
Threshold, V_T	2.5 V (typical)
Saturation, V_{DSSAT}	1 V (approximate - V_{GS} dependent)

MTP2N50 MOSFET
Front View



EXPERIMENT NO. 4 - Audio Frequency Amplifier

This lab introduces you to some very common aspects of design through a very simple single transistor amplifier. In this lab you will get your first design experience with the concepts of small signal analysis and biasing. These concepts are extremely fundamental to circuit design, so make sure you understand them, and the distinction between them. This lab has been introduced into the course primarily because students have had trouble with these concepts. In addition, this lab requires you to use some common measurement techniques. The experiment is quite simple relative to some of the later ones, and should not take you much time in the lab. As your first design, it may require substantial thought beforehand.

The Experiment

You must design, build, and characterize an amplifier having the following specifications

Gain:	$\lvert A_v \rvert$ = 15 ± 20%, (23 DB +/- 1.5 DB) from 100Hz to 10kHz
Input Impedance:	10 kΩ ± 2 kΩ @ 1kHz
Output Impedance:	<6kΩ @ 1 kHz
Output Voltage Swing:	at least ±2.5 volts from quiescent point
Low Frequency Rolloff:	-3dB point (relative to midband gain) must be kept below 30Hz

Your amplifier should run from a single 12V power supply, and be based on the 2N2222A (npn) transistor, which has the following specifications:

BV_{CEO} = 30V
$70 < h_{FE} \approx h_{fe} < 230$ @ l mA
P_D = 300mW
$1/h_{OE} > 150k\Omega$ typical @ 1 mA

Through the proper choice of biasing components, your circuit should meet design criteria for the full range of h_{FE} (70 to 230) and for $0.50V < V_{BE} < 0.70V$. It is not sufficient for you to make your circuit work for one particular set of components - it must be designed to work for any components that meet the appropriate specifications (i.e. $65 < h_{FE} < 250$, resistor values ± 5%, etc.). You will be graded stringently on this point.

A common emitter amplifier with a partially bypassed emitter circuit will work. You must choose the passive component values so that your circuit functions as required. Your report should contain:

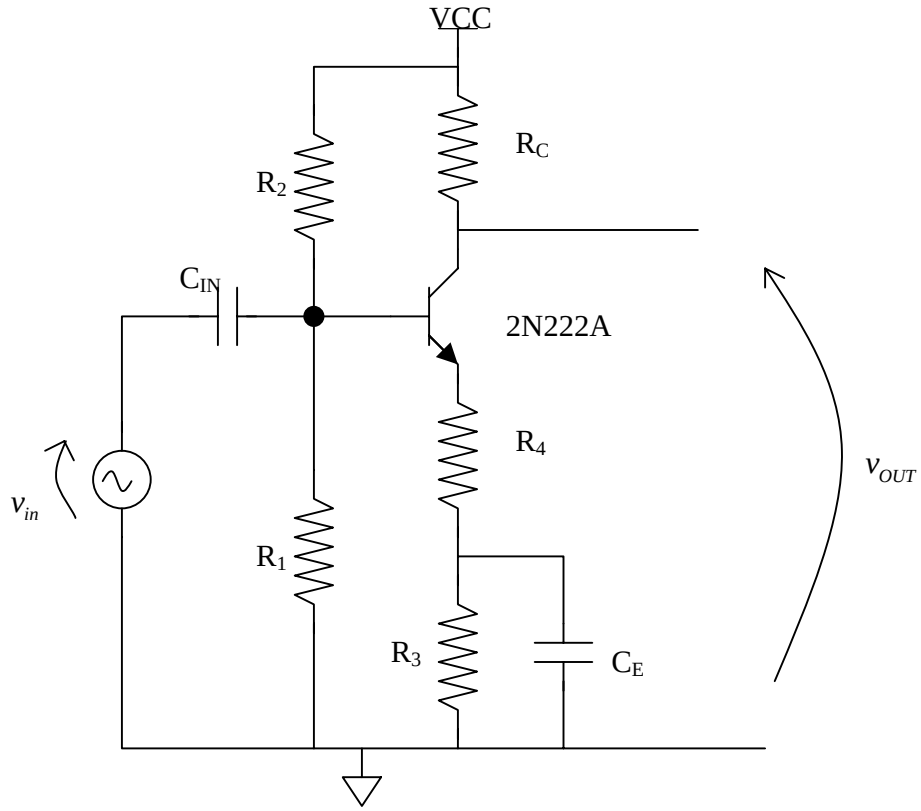
- Schematic
- Description of how you chose your component values, along with calculations of quiescent voltages and currents, gain, input impedance and output impedance
- Measurements of quiescent voltages
- Printout of the Bode plot of the amplifier taken on our computerized plotter showing that the amplifier conforms to the design specifications. The printout must show your protoboard number and be initialed by the TA.
- Measurements of input and output impedances at 1kHz.

HINTS

1. It is often easier, in this type of design, to satisfy the small-signal design specifications first, and then choose biasing components, which, consistent with small-signal requirements, fulfill the remaining requirements of quiescent point stabilization and large-signal properties such as output voltage swing.

2. Input impedance is most easily measured by placing a resistor comparable to the expected input impedance in series with the signal source. You measure the input current from the voltage across this resistor. Use two oscilloscope probes, one connected to each side of the resistor, and set the scope to measure the difference in the voltages (invert one scope channel and sum them). Be sure both channels are set to the same sensitivity. (This approach to measuring the input current is suggested because it is simple to predict when it will work. Instruments such as bench voltmeters and DVMs usually have too much capacitance and too little frequency response to be used except at quite low frequencies. The differential scope method works well to quite high frequencies.)

3. The output impedance can be measured using a similar technique to what you used in lab #1. The only trick is to connect the load resistor so that the quiescent point is not disturbed so much that the amplifier ceases to work properly.



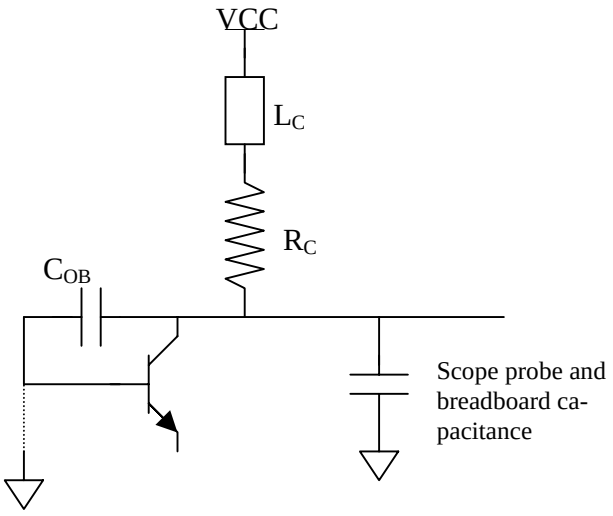
Circuit Topology for a Common Emitter Amplifier Based on the 2N222A

EXPERIMENT NO. 5 - Video Amplifier

The bandwidth for television video signals in the United States (NTSC standard) is approximately 30 Hz to 4 MHz. Congress has recently passed legislation defining a new digital TV standard that will require a 3 DB bandwidth of 30 Hz to 6 MHz. This is comparable to other video applications, particularly computer displays. (Video displays are often even wider because of their high resolution and high frame rate.) When the display is a large-screen, cathode ray tube, a common design problem arises in which a modest video signal level on the order of 2.2 volts pp is to drive the grid of a CRT electron gun directly. An amplifier capable of providing the required gain, bandwidth, and output voltage is a standard feature of all TVs and monitors. Suppose that our new 6 MHz TV requires a CRT drive level is from +20 to +65 volts relative to ground and that in addition to the +12V supply (from which to derive base biases), 80 VDC can be obtained from the high voltage supplies in the lab. Design and build an amplifier that will give a 30 Hz to 6 MHz bandwidth as defined by its lower and upper 3 DB points. The circuit is to have a minimum input impedance of 1,000 ohms over the entire frequency range. Simulate the capacitive loading of the CRT grid with the 10x oscilloscope probe (about 15 pf capacitance).

You will probably find that these design requirements cannot be met with a simple common emitter amplifier, and that a cascode configuration will be necessary. The cascode connection reduces the Miller effect, which helps keep the input impedance high. Also, it is difficult to combine high cut-off frequency, high breakdown voltage, and high power handling in one transistor. The cascode circuit eases these demands by dividing the requirements between two transistors. Design the circuit around 2N3440 and 2N2222A transistors. The maximum power dissipation for a 2N3440 is 1 watt in an ambient temperature up to 50°C. Design your circuit conservatively to have the 2N3440 dissipate no more than about .65 W. Design around typical values of all transistor parameters. A table of some of the parameters is given below; more complete data is available in the Appendix.

A complication in the problem is that the capacitances shunting the output are substantial. In addition to the scope probe and C_{OB} of the 2N3440 there can be up to 2 pf between terminals of the breadboard. You will probably find that this capacitance limits the upper frequency cutoff from the collector load pole to something under 3 MHz. There is a standard method for increasing the bandwidth by putting a coil in series with the collector resistor as shown below.



For this circuit, the data shown below gives the relation between the inductance L_C and the bandwidth. The frequency f_{max} is the cutoff frequency with no inductor, *i.e.*, $f_{\max} = \frac{1}{(2\pi R_C C_{shunt})}$ where C_{shunt} is the total capacitance to ground from the output node. Use this configuration to move the 3DB cutoff frequency (i.e., the frequency at which the gain decreases by a factor of .707) out as needed. There is a selection of small RF chokes (coils) available from the TA. You may check out and return what you need. (The coils look much like resistors ($ .02 ea.) but cost over two dollars each. You must return these and not treat them as casually as resistors.) The color code on coils is the same as for resistors; the units are microhenries. (The coil color code can be difficult to be sure of because the colors are not well printed. There is an R-L-C meter in the lab to check with.)

Note that 6 MHz is an appreciable fraction of the 250 MHz common base cutoff frequency of the 2N2222A. In calculating input impedance you will have to take account of that fact. The Q-point will have to be stabilized in such a way as to account for the range of h_{FE} of the common emitter transistor and for $.5 < V_{BE} < .7$ volt. I_{CBO} should not be a problem. Be sure to show you have met this requirement by design.

Wiring can cause problems in a circuit like this. You will reduce or avoid such problems if you keep it neat with short leads. One unhappy fact of life at high frequencies is that power supplies may not be high frequency signal grounds unless one puts a small capacitance (typically .1 to .01 μfd.) between the supply and ground physically located right at your circuit. The best kind of capacitor is a ceramic disc type; it is commonly called a bypass capacitor. This observation applies to both the 12-volt supply on the breadboard station and to the 80-volt supply, which will have to come from one of the large Lambda supplies. Any electrolytic capacitors should be bypassed as well, because they often have significant series inductance.

Measure the gain over the range from 10 Hz to 10 MHz. This requirement must be met with a plot from the automated Bode plotter. Make a separate measurement to show that you have met the input impedance requirement. Also, record the quiescent circuit voltages. Please try to minimize component damage by checking your wiring before applying power. If you have a problem, check the devices on the curve tracer.

Write-up: In your write-up do the following:

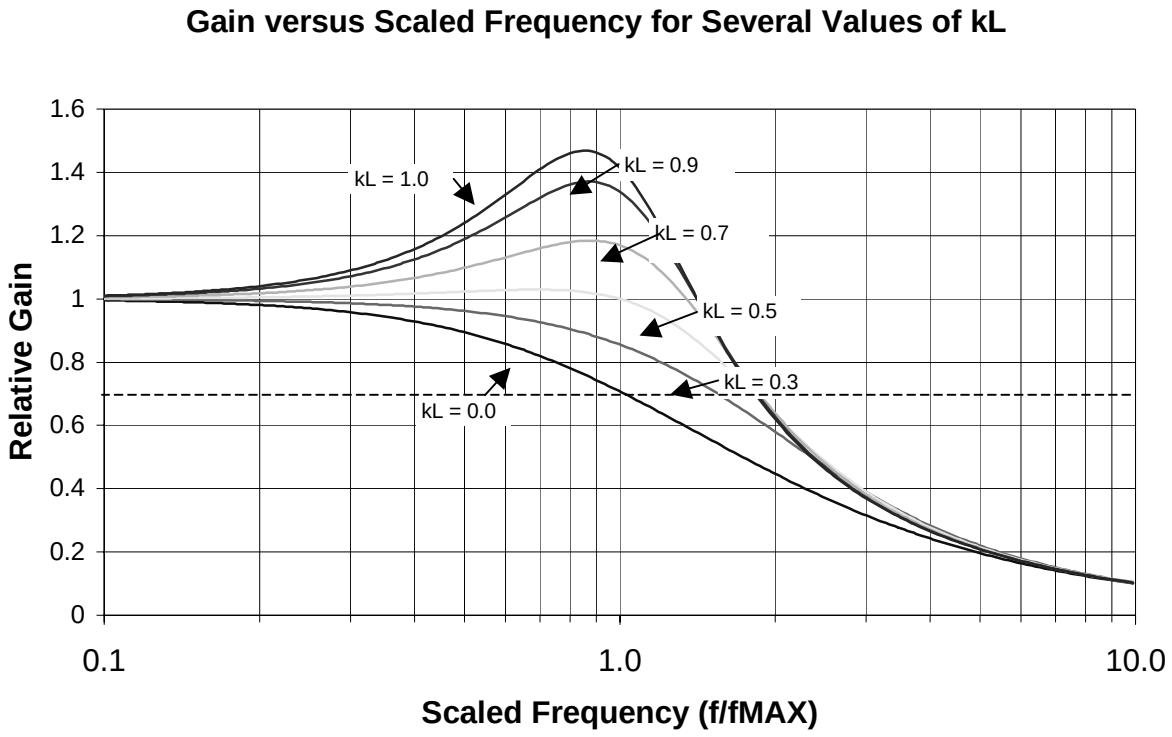
I. Indicate how you arrived at component values.

II. Calculate the input impedance of the whole circuit for typical transistor parameters at 6 MHz. Compare this to the measured value. (Note that if you meet the input impedance requirement at 6 MHz, you do so automatically for all frequencies below that too.)

III. Calculate the limits on the quiescent current due to transistor parameter variations.

IV. Derive the relative gain formula for the circuit including the effects of the inductor. (See discussion below.)

V. Report your measurement results for both the Q-point and the frequency response (Bode plot) with an explanation of any discrepancy with calculation.



Relative Gain Calculations: The collector impedance, Z_C, made up of R_C, L_C, and C_{SHUNT}, dominates the high frequency gain of this circuit and its dependence on frequency determines the relative gain of the amplifier. This combination of passive components occurs at various scales in many applications and is best analyzed in dimensionless terms. The relative amplifier gain will be the dimensionless ratio $|Z_C|/R_C$. If the inductor is not present the circuit has single pole behavior with a cutoff frequency given by f_{MAX} defined above. Scaling all frequencies by this value makes the frequency scale dimensionless too. Finally, one can express the inductance as the product of a dimensionless coefficient k_L as:

$$L_C = k_L R_C^2 C_{shunt}$$

As **part of your write-up, show** that the relative gain is given by the expression:

$$\frac{|Z_C|}{R_C} = \frac{\sqrt{1+[k_L^2(f/f_{\max})^3 + (1-k_L)(f/f_{\max})]^2}}{(f/f_{\max})^2 + [k_L(f/f_{\max})^2 - 1]^2}$$

This formula was used to calculate the family of curves on the graph above. The graph is quite handy for picking L_C based on how much additional frequency response is required.

Selected transistor data. See the data sheets for more details.

Transistor type	Parameters				
	C_{OB} (pF)	f_T (MHz)	BV_{CBO} (V)	BV_{EBO} (V)	P_D (W)
2N2222	7 @ V_{CB}=10 V	250	60	30	0.3
2N3440	4 @ V_{CB}=40 V	25	300	250	1.0

HINTS:

1. The collector resistor is fixed by the maximum power dissipation requirements. Use the maximum power theorem, which states that a voltage source in series with a resistor R and

a load will transfer maximum power to that load when half the voltage is across R and half across the load. That power is $V^2/4R$. The trick is to identify the voltage that goes with applying this theorem to your circuit.

2. Pay attention to heat in the collector resistor – it may be too much for the standard quarter watt resistors you use for most of the labs. See the comments on resistors in the introduction.

3. The quiescent current is set by the midpoint of the output drive levels.

4. V_{CB} for the 2N2222 is set by a compromise between too low a value increasing the value of C_{OB} and too high a value giving an unstable Q point. A reasonable compromise here is $\approx$ 4 to 8 V.

5. Input current can be determined by placing a resistor in series with the input and using two scope probes with the scope set to measure the difference in voltage across the resistor. In making this measurement, remember that the voltage across the amplifier input is out of phase with either the generator output or the voltage across the series resistor. You must measure the amplifier voltage separately of the drop across the resistor. The capacitance of the scope probes may not be negligible in the measurement of input impedance at 8 MHz. (The reactance of 15 pf at 6 MHz is 1700 ohms!) Be sure to account for this.

6. The output of the oscillators in the lab is not completely independent of frequency especially above 1 MHz. The Bode plotter compensates for this, but input impedance and your own checkout measurements may be affected by it.

EXPERIMENT NO. 6 - Sine Wave Oscillator

Sinusoids are useful waveforms, because they are convenient basis functions for analyzing the response of (linear) systems involving time derivatives and/or integrals of signals. Any sufficiently well-behaved signal can be represented by a linear combination of sinusoids (through Fourier transforms) and derivative and integral operations on any of the basis functions yields another basis function. In fact, sinusoids are the only functions that retain their original shape during processing by a linear system, which makes it easy to characterize the effect of the system by specifying only the amplitude and phase change. In mathematical language, sinusoids, or rather imaginary exponentials, are the eigenfunctions of linear systems. Consequently, sine wave generators are useful tools for circuit testing and diagnosis (as you have already seen in the previous labs). In this lab, you will design a variable frequency sine wave generator. Although the approach you use cannot yield a sine wave of sufficient purity (*i.e.* low harmonic content) for use in a high quality generator, the quality of its waveform is sufficient for many less demanding applications. This is a fairly inexpensive way of producing a versatile waveform generator (sine, triangle and square waves simultaneously) over a broad frequency range.

The approach you will use involves the generation of a triangle wave followed by a conversion of the triangle wave to a sine wave using a nonlinear conversion circuit. It is relatively easy to generate a high-quality variable frequency triangle wave using an op amp integrator circuit with a variable input resistor. (Alternatively, it is easy to convert a variable frequency square wave to a triangle wave using an integrator). The triangle wave generator will be made using a combination of an integrator and a Schmitt trigger as shown in the figure below. Although in practice the integrator and Schmitt trigger functions can be integrated into a single fairly simple circuit, the approach outlined in this lab will give you exposure to two opamp applications (integrators and Schmitt triggers separately).

A circuit having the block diagram shown on the next page can generate a triangle wave. When the Schmitt trigger output is negative, the integrator output ramps positive. When that output reaches the positive-going threshold of the Schmitt trigger, the Schmitt trigger output goes positive. This causes the integrator output to ramp downward until the Schmitt trigger's negative going threshold is reached. This sends the Schmitt trigger output negative, and the cycle repeats. The symmetry of the triangle wave depends on two things. First the negative and positive outputs of the Schmitt trigger must be equal in magnitude to obtain equal slopes for the positive and negative going parts of the triangle wave. Second, the positive and negative switching points of the Schmitt trigger, which must be equal magnitude, control the positive and negative peaks of the triangle wave. Although an opamp-based Schmitt trigger will not precisely meet these two conditions, the accuracy will be acceptable

for the purpose of this experiment. Your task is to determine how to implement the integrator and Schmitt trigger in such a way as to yield a triangle wave generator having a frequency range of at least 100Hz to 10kHz. You will be allowed one 10 kΩ potentiometer for adjusting the oscillator frequency. The amplitude of the square wave need only be greater than 5 volts pp, however, the triangle amplitude should be as near a practicable to 5 volts pp.

The triangle to sine conversion circuit you will use is an example of a class of nonlinear circuits. It utilizes the nonlinear I-V characteristics of the base-emitter junctions of bipolar transistors. Attached is a copy of the original journal article (W.M.C. Sansen, S. Lui, S. Peeters, and Robert G. Meyer, *The Differential Pair as a Triangle-Sine Wave Converter*, IEEE J. Solid-State Circuits, Vol. SC-11, June 1976, pp. 418-420) describing this triangle to sine conversion technique. Using a single CA3086 NPN transistor array chip, design and construct a circuit following the technique outlined by Meyer, et al. It is almost certainly easiest to use the collector output option rather than the emitter option that they also mention. The combination of this circuit with your triangle wave generator will be a variable frequency sine wave generator. You probably have to put something between the triangle output and the sine-converter input to reduce the signal amplitude to an appropriate value. The output sinusoid shall be 5 volts pp too and have a zero mean value. The output source impedance shall not exceed 100 ohms. (This does not mean you could load the circuit with 100 ohms! You may meet this requirement by design.) You very likely need another opamp to do this. It is probably best to use it as a differential amplifier, taking the difference in potential between the two collectors of the sine converter. This reduces distortion and saves a capacitor. As a difference amplifier is a little harder to design, I will reserve points on the lab grade specifically for doing this successfully.

In demonstrating your circuit to the TA, you must show reasonably distortion-free sine wave generation from 100 Hz to 10 kHz. Distortion must be reduced by proper selection of passive components in the triangle wave oscillator. To establish a quantitative measure of the distortion of the sine wave, use an oscilloscope to capture the signal when your generator frequency is about 1 kHz. Use a sampling rate of at least 100 kHz and try to adjust for as nearly ten cycles of the waveform on screen as practicable. Fill the vertical scale as much as possible without clipping. Use Excel to calculate the FFT and from the peaks in that transform calculate the ratios of the second through fourth harmonics to the fundamental. To meet the requirements of the lab, the amplitudes of the second and third harmonics must be at least 23 DB below the fundamental. Also capture the square and triangle outputs of your circuit at 1 KHz. In your report, overlay them with the sine wave data **all on the same time axis**. As in lab 1, the TA will either initial a printout of your waveforms or give you an electronic signature to include on your graph when you demonstrate your triangle and square wave outputs to him.

In the section of your report that has the tabulation of measured and designed values, please include at least:

1. Amplitudes of all waveshapes at 100 Hz, 1 kHz, and 10 KHz.
2. Distortion of the sine wave -- FFT printout and the derived ratio of the second and third harmonics to the fundamental amplitude. Make your FFT printout have a DB scale and normalize so that the fundamental is at 0 DB.
3. Waveshapes of all outputs at 1 KHz overlaid on the same time axis.
4. Maximum and minimum frequencies.
5. Quiescent values of the voltages in the sine converter
6. DC or mean value of the sinusoidal output -- i.e. is it really zero mean?

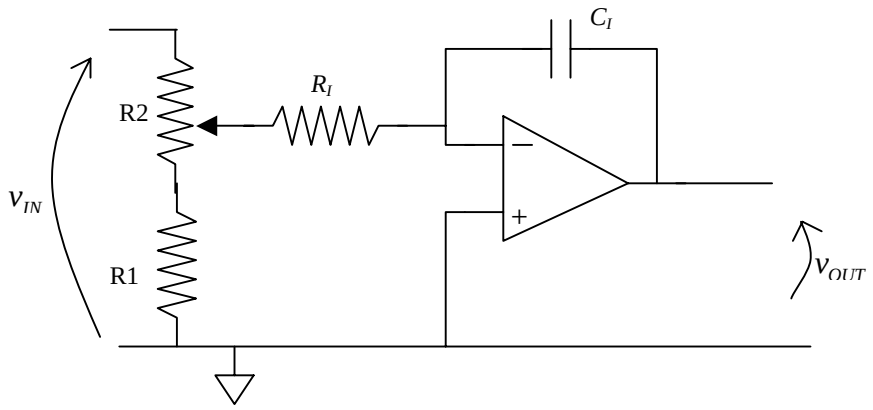
Hints:

1. Bypassing the power supplies with small ceramic capacitors <u>on</u> the breadboard will help avoid spurious oscillations.

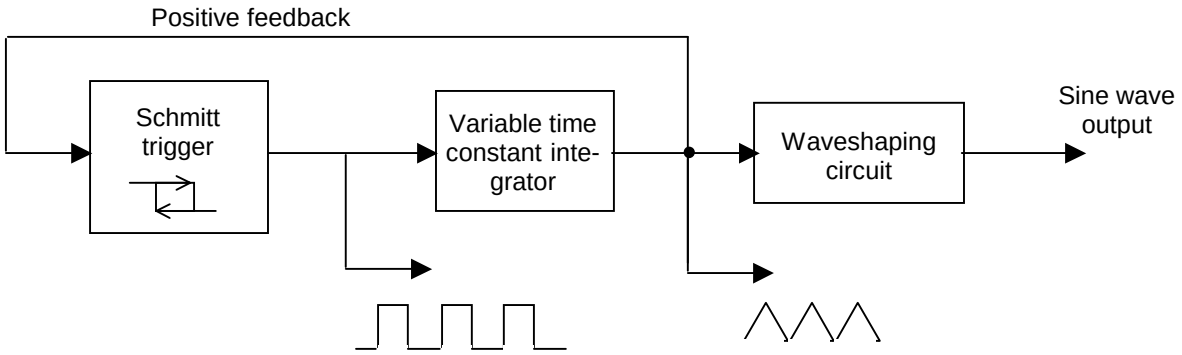
2. Keep the bias currents in the CA3086 transistors below 1mA for best results**.**

> ***<u>WARNING</u>: Pin 13 (SUBSTRATE) must be connected directly to the*** V_{EE} (-12 volt) supply line in order to isolate one transistor from another. This limits how one can use transistor Q5. Failure to observe this requirement may destroy the IC. We do not take kindly to wholesale destruction of CA3086s. You check these out from the TA, who is able to check their operation before you receive them and after you return them.

3. One technique for realizing a variable time-constant integrator is shown below:



Variable Time Constant Integrator



Function Generator Block Diagram: the Schmitt trigger and integrator form a square and triangle generator. The waveshaping circuit uses a differential pair with current source biasing and an emitter resistor. (See attached article.) You should have an opamp buffer in that circuit to minimize distortion and lower the output impedance.

Correspondence

The Differential Pair as a Triangle-Sine Wave Converter

ROBERT G. MEYER, WILLY M. C. SANSEN, SIK LUI, AND STEFAN PEETERS

Abstract—The performance of a differential pair with emitter degeneration as a triangle-sine wave converter is analyzed. Equations describing the circuit operation are derived and solved both analytically and by computer. This allows selection of operating conditions for optimum performance such that total harmonic distortion as low as 0.2 percent has been measured.

I. Introduction

The conversion of triangle waves to sine waves is a function often required in waveshaping circuits. For example, the oscillators used in function generators usually generate triangular output waveforms [1] because of the ease with which such oscillators can operate over a wide frequency range including very low frequencies. This situation is also common in monolithic oscillators [2]. Sinusoidal outputs are commonly desired in such oscillators and can be achieved by use of a nonlinear circuit which produces an output sine wave from an input triangle wave.

The above circuit function has been realized in the past by means of a piecewise linear approximation using diode shaping networks [1]. However, a simpler approach and one well suited to monolithic realization has been suggested by Grebene [3]. This is shown in Fig. 1 and consists simply of a differential pair with an appropriate value of emitter resistance R. In this paper the operation of this circuit is analyzed and relationships for optimum performance are derived.

II. Circuit Analysis

The circuit to be analyzed is shown in Fig. 1(a). The sinusoidal output signal can be taken either across the resistor R or from the collectors of $Q1$ and $Q2$. The current gain of the devices is assumed large so that the waveform is the same in both cases.

The operation of the circuit can be understood by examining the transfer function from V_i to current i flowing in R. This is shown in Fig. 1(b) and has the well-known form for a differential pair. The inclusion of emitter resistance R allows the curvature to be adjusted for optimum output waveform, as will be seen later.

When a triangle wave input of appropriate amplitude is applied as shown in Fig. 1(b), the output waveform is flattened by the curvature of the characteristic and can be made to approach a sine wave very closely. As with all such circuits, the distortion in the output sine wave is dependent on the input amplitude and this must be held within certain limits for acceptable performance.

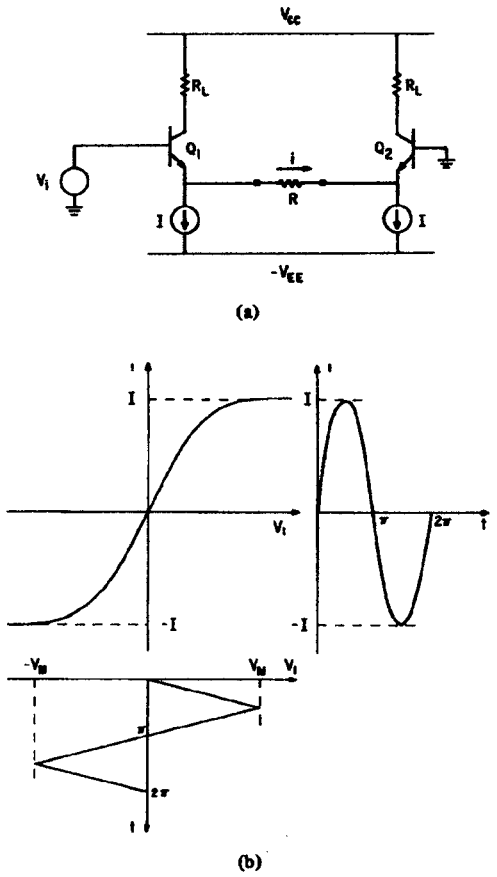


Fig. 1. Triangle-sine wave converter. (a) Circuit schematic. (b) Transfer function.

In the following analysis, $Q1$ and $Q2$ are assumed perfectly matched, although in practice mismatches will occur and give rise to second-order distortion (typically less than 1 percent). However, introduction of an input dc offset voltage has been found to reduce second-order distortion terms to negligible levels and they will be neglected in this analysis. The presence of such an offset does not affect the following analysis. From Fig. 1(a)

$$V_i = V_{BE1} + iR - V_{BE2} \tag{1}$$

but

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_K} \tag{2}$$

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$$V_{BE2} = V_T \ln \frac{I_{C2}}{I_K} \tag{3}$$

where

$$V_T = \frac{kT}{q}. \tag{4}$$

Substitution of (2) and (3) in (1) gives

$$V_i = iR + V_T \ln \frac{I_{C1}}{I_{C2}}. \tag{5}$$

If $\alpha \simeq 1$ for $Q1$ and $Q2$ then

$$I_{C1} = I + i \tag{6}$$

$$I_{C2} = I - i. \tag{7}$$

Substitution of (6) and (7) in (5) gives

$$\frac{V_i}{V_T} = \frac{i}{I}\left(\frac{IR}{V_T}\right) + \ln \frac{1 + \frac{i}{I}}{1 - \frac{i}{I}}. \tag{8}$$

Equation (8) is expressed in normalized form and shows that the output signal i/I normalized to I depends only on normalized input voltage V_i/V_T and factor IR/V_T. Because of the small number of parameters in (8), it is readily solved in normalized form by computer to yield a series of curves specifying the circuit performance. Before this is pursued however, it is useful to consider an approximate analytical solution of (8) which gives some insight into the circuit operation.

The log term in (8) can be expanded as a power series

$$\ln \frac{1 + \frac{i}{I}}{1 - \frac{i}{I}} = 2\frac{i}{I} + \frac{2}{3}\left(\frac{i}{I}\right)^3 + \frac{2}{5}\left(\frac{i}{I}\right)^5 + \cdots \tag{9}$$

for

$$\frac{i}{I} < 1. \tag{10}$$

Substitution of (9) in (8) for the circuit transfer function gives

$$\frac{V_i}{V_T} = \left(\frac{IR}{V_T} + 2\right)\frac{i}{I} + \frac{2}{3}\left(\frac{i}{I}\right)^3 + \frac{2}{5}\left(\frac{i}{I}\right)^5 + \cdots. \tag{11}$$

This can be expressed as

$$\frac{1}{\frac{IR}{V_T} + 2}\frac{V_i}{V_T} = \frac{i}{I} + \frac{2}{3}\frac{1}{\frac{IR}{V_T} + 2}\left(\frac{i}{I}\right)^3 + \frac{2}{5}\frac{1}{\frac{IR}{V_T} + 2}\left(\frac{i}{I}\right)^5 + \cdots. \tag{12}$$

The desired transfer function for the circuit is [see Fig. 1(b)]

$$i = K_1 \sin K_2 V_i \tag{13}$$

where K_1 and K_2 are constants, and thus

$$K_2 V_i = \arcsin \frac{i}{K_1}. \tag{14}$$

Expansion of (14) in a power series gives

$$K_2 V_i = \frac{i}{K_1} + \frac{1}{6}\left(\frac{i}{K_1}\right)^3 + \frac{3}{40}\left(\frac{i}{K_1}\right)^5 + \cdots. \tag{15}$$

By comparison of (12) and (15) it is apparent that in order to realize the desired transfer function, it is necessary (but not sufficient) that

$$K_1 = I \tag{16}$$

$$K_2 = \frac{1}{\frac{IR}{V_T} + 2}\frac{1}{V_T}. \tag{17}$$

Equation (16) shows that the peak value of the output current should equal the current source value I. If the input triangle wave has peak value V_M then (13) indicates that for a perfect sine wave output it is necessary that

$$K_2 V_M = \frac{\pi}{2}. \tag{18}$$

Substitution of (17) in (18) gives

$$\frac{V_M}{V_T} = 1.57\frac{IR}{V_T} + 3.14. \tag{19}$$

Equation (19) gives the normalized input triangle wave amplitude for minimum output distortion.

The circuit transfer function given by (12) is to be made as close as possible to the arcsin expansion of (15). If we equate coefficients of third- and fifth-order terms in (12) and (15) we obtain IR/V_T equal to 2 and 3.33, respectively. It is thus expected that the best performance of the circuit will occur for this range of values, and this is borne out by experiment and computer simulation.

III. Computer Simulation and Experimental Results

The solution of (8) was obtained by computer simulation for various values of V_M/V_T (normalized triangle wave amplitude) and factor IR/V_T, and the output signal was analyzed into its Fourier components. Third-harmonic distortion (HD_3) is defined as the ratio of the magnitude of the signal at the third harmonic frequency to the magnitude of the fundamental. Total harmonic distortion (THD) is $\sqrt{HD_3^2 + HD_5^2 + \cdots}$. A typical plot of HD_3 and THD is shown in Fig. 2 for $IR/V_T = 2.5$. It can be seen that the THD null and the HD_3 null occur at about the same value of V_M/V_T, and this is true for any value of IR/V_T. The measured points in Fig. 2 show good agreement with the computed curves and both show a minimum value of THD of about 0.2 percent for $V_M/V_T \simeq 6.6$. This corresponds to $V_M \simeq 175$ mV for $V_T = 26$ mV.

The effect of variations in IR/V_T on the minimum value of THD is illustrated by the computed curve of Fig. 3. At each point on this curve, V_M/V_T was adjusted for minimum distortion. This curve shows that best performance is obtained for $IR/V_T \simeq 2.5$, and this is within the range of 2–3.3 predicted earlier. These results were verified by experimental data.

The effect of temperature variation on circuit performance was investigated by setting $IR/V_T = 2.5$ at room temperature and holding I, R, and V_M constant as T was varied. Measured and computed THD were less than 1 percent from 0° to 55°C. The measured rms output amplitude decreased 5 percent over this temperature range.

The results described above were measured and computed at low frequencies. The measurements were made at frequencies of the order of 100 kHz where the distortion was still frequency independent. Computer simulation neglected all capacitive effects in the transistors. In order to investigate the performance of the circuit at frequencies where charge storage

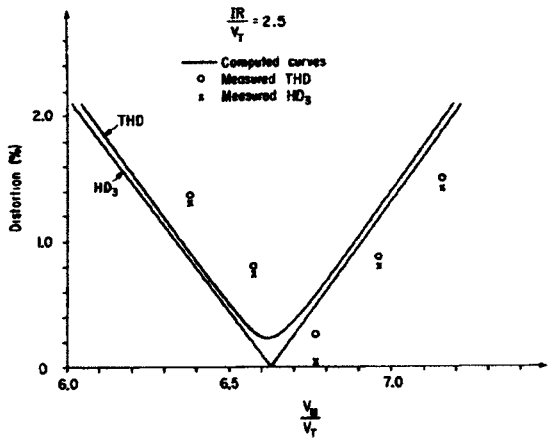

Fig. 2. Computed and measured distortion versus normalized input voltage of the circuit of Fig. 1(a) with $IR/V_T = 2.5$.

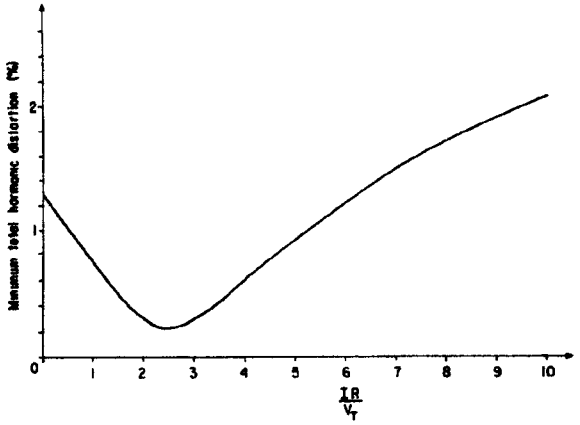

Fig. 3. Computed minimum total harmonic distortion versus IR/V_T for the circuit of Fig. 1.

in the transistors is important, computer simulation was used with input frequencies up to 10 MHz and including a complete, large-signal high-frequency device model. The results showed that THD was independent of frequency up to about 1 MHz. Above this frequency, THD increased rapidly due to irregularities in the peaks of the output sinusoid. This is due to the fact that at the signal peaks, the output current i approaches the current source value I [see (16)], and thus $Q1$ and $Q2$ alternately approach cutoff. The f_T of the transistors in this condition is quite low and they are unable to follow the input signal.

IV. Conclusions

The performance of a differential pair with emitter degeneration as a triangle-sine wave converter has been approached by forming a nonlinear equation in three normalized parameters. The output normalized waveform i/I is a function only of the input amplitude V_M/V_T of the triangle wave, and factor IR/V_T. Computer solution shows that the output sine wave THD has a minimum of about 0.2 percent for $IR/V_T = 2.5$ and $V_M/V_T = 6.6$.

Acknowledgment

The authors wish to thank Dr. A. B. Grebene for suggesting to them the potential of the differential pair as a triangle-sine wave converter.

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[1] E. H. Heflin, "Compact function generator with enhanced capability–cost ratio," *Hewlett-Packard J.*, pp. 15–20, July 1973.
[2] A. B. Grebene, *Analog Integrated Circuit Design*. New York: Van Nostrand Reinhold, 1972, p. 313.
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Integrated TV Tuning System

W. JOHN WU AND ERIC G. BREEZE

Abstract—**This paper presents a frequency synthesized digital tuning system for UHF/VHF TV receivers and the integrated circuits developed to implement this scheme. The design and performance of the GHz ÷ 248/256 programmable prescaler is described in detail.**

Recent trends in the consumer and communication industry toward more cost effective and more reliable systems place the following requirements on advanced TV tuning systems: meet new FCC regulations; tune all channels (VHF and UHF) individually without complex alignment; be capable of interfacing with digital displays and remote control circuits; have keyboard entry for channel selection; and allow provisions for fine tuning. This correspondence presents a frequency synthesizer which meets all the above requirements and is highly accurate as the phase-locked loop is self-compensating for parameter drifts and component tolerance.

Fig. 1 gives the block diagram of the frequency synthesizer. The dotted block represents a standard VHF or UHF varactor tuner. An amplifier is connected to the VCO output of the tuner to increase the voltage to the acceptable level to drive the digital prescaler. The purpose of the prescaler is to divide down the local oscillator high frequencies to a range that can be processed and counted by TTL or MOS logic circuits. Output of the prescaler is then fed to the programmable counter programmed by the keyboard entry. The output is then compared with a crystal controlled reference frequency. The phase/frequency comparator drives an integrator which in turn provides voltage control to the varactor tuner input [1]. Physical implementation of this scheme requires 5 integrated circuits and will precisely tune 99 channels, the air channels (2 through 83), and the cable channels (84 through 99). The fine tuning provides ±1 MHz in 128 steps. It also has the capability of keyboard entry, channel searching, and channel number display.

The 1 GHz ÷ 248/256 prescaler is designed for this specific

Manuscript received December 28, 1975.
The authors are with Fairchild Semiconductor, Mountain View, CA 94042.

EXPERIMENT NO. 7 - Telephone Anti-Aliasing Filter

WARNING: I have started on redesigning this lab using MOSFET array transistors. If I complete the redesign before anyone does this lab, it will be superceded by the new exercise.

It is now standard practice to send telephone voice service over digital links by filtering the analog signal and sampling this bandwidth-limited signal with an ADC. The standard service uses an 8 Ksps sampling rate, which requires that the signal bandwidth be restricted to below 4 kHz. (Although you are not expected to know this as a result of prerequisite courses, all systems which use analog to digital conversion must be careful to limit the high frequency content of the original signal. It is a sampling theorem due to Nyquist that the original signal can only be recovered from the digital samples if the signal had no components beyond one-half the sampling frequency. If this condition is not met, then not only is data lost, but false information is folded into the real data. If you played around with the FFT scope in Experiment 1, you may have seen this effect.) Voice service requires that frequency components in the original signal be maintained as well as possible out to beyond 3 kHz. Usually the 3 DB down point is placed at around 3.1 to 3.3 KHz. In this lab you are to design and build a filter which might be used for this purpose using active circuits based on operational amplifiers.

The main difficulty in realizing such a filter is the need for out of band suppression. The minimum suppression I will consider acceptable is 9 DB at 4 kHz. and 30 DB at 8 kHz. The midband gain of the filter subsystem at 1 kHz. should be 20 DB (or 10X) +/- 1.5 DB. At the low frequency end, there should be at least a single pole high pass response so the DC components are removed from the signal. The low frequency response should be down no more than by 6 DB at 100 Hz. You are free to choose any standard transfer function that will be reasonably smooth. If you choose one which exhibits passband ripple (the Chebycheff response, for example) then that ripple should not exceed 1 DB. Probably the simplest acceptable solution is a Butterworth filter of odd order. (Odd order because most of the complication of construction goes into the quadratic pole pairs, and extra rolloff comes with minimal effort with one more simple pole.) You are free to make that filter from cascaded sections of any of the designs that are discussed in your text or in class. There is an automated response measurement available as with labs 4 and 5.

To meet the requirements for response with the tolerances of the components in the lab may require adjusting some resistor values. (You should use mostly film capacitors, as their tolerance of +/- 10 % is the best we can manage. Resistor values come in roughly 10 % increments.)

While I am setting the rolloff requirement fairly leniently, you should be aware that real systems require more suppression near 4 kHz. This extra attenuation can come at some increase in the transfer function at higher frequencies. The way this is usually done is to use a filter that

has one or more zeros on the imaginary axis. A zero of this kind means the filter has no response to sinusoids at the zero frequency. The figure below shows two transfer functions overlaid. The first curve drops very rapidly past 3.1 kHz, going to zero transmission at 4.05 kHz before rising to -37 DB at a little over 5 kHz. This is the transfer function:

$$H(s) = \frac{1}{1 + s\tau_1} \cdot \frac{(s\tau_z)^2 + 1}{(s\tau_2)^2 + \frac{s\tau_2}{Q_2} + 1} \cdot \frac{1}{(s\tau_3)^2 + \frac{s\tau_3}{Q_3} + 1}$$

where

$\tau_1 = 1.51 \cdot 10^{-4}$ sec [1053 Hz]

$\tau_2 = 7.05 \cdot 10^{-5}$ sec [2256 Hz]

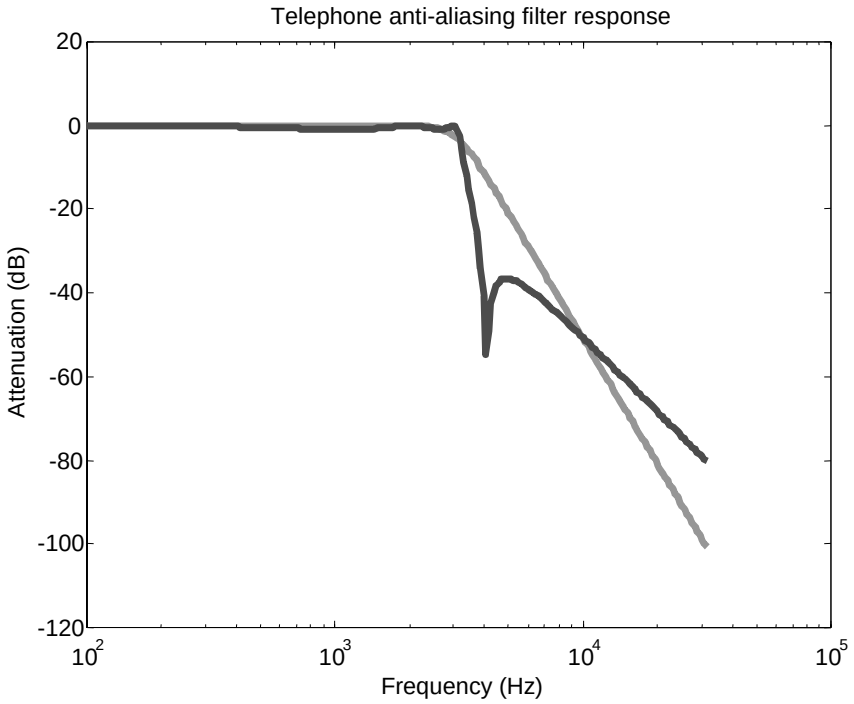
$Q_2 = 1.57$

$\tau_z = 3.88 \cdot 10^{-5}$ sec [4100 Hz]

$\tau_3 = 5.14 \cdot 10^{-5}$ sec [3096 Hz]

$Q_3 = 8.07$

The second curve is a 5th order Butterworth filter with its cutoff at 3.1 kHz. Notice that eventually the Butterworth will attenuate more than the first curve, but the filter with a zero does better up to 10 kHz. I am including a reprint from a book, *Principles of Active Network Synthesis and Design* by Gobind Daryananni (John Wiley, NY, 1976) on how to build the section of the filter with the zeros using three or four opamps. If you are feeling adventurous, I would encourage you to try this circuit. It actually is only two or three more opamps than the least complicated acceptable solution. Please feel free to take or ask for more opamps as you need them. You can make the two factors of H(s) that have no zeros in any of the usual low pass topologies – they are not particularly high Q. The section with zeros can be done by following the discussion below.



Realization procedure for zeros on the $j\omega$ axis from Daryannani, *op. cit.:*

10.2 REALIZATION OF THE GENERAL BIQUADRATIC FUNCTION

In this section we describe two methods for the realization of the general biquadratic function of Equation 10.1. The first is based on the summation of the voltages already available in the basic circuit developed in the last section. This

summation requires an extra summing amplifier. The resulting circuit will be referred to as the **summing four amplifier biquad**. The second method uses the feedforward scheme, developed in Chapters 8 and 9, in which the zeros are formed by introducing the input signal at appropriate nodes in the basic three amplifier circuit. This circuit will be called the **feedforward three amplifier biquad**.

10.2.1 THE SUMMING FOUR AMPLIFIER BIQUAD

In the last section it was shown that the voltage at node 1 of the basic three amplifier circuit (Figure 10.4) yields the band-pass function:

$$V_1 = V_{BP} = \frac{-\frac{1}{R_4C_1}s}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}} V_{IN} \tag{10.18}$$

while node 3 exhibits the low-pass function:

$$V_3 = V_{LP} = \frac{-\frac{1}{R_2R_4C_1C_2}}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}} V_{IN} \tag{10.19}$$

The voltage at node 2 is the same as that at node 3 with the sign reversed, that is,

$$V_2 = -V_{LP} \tag{10.20}$$

The band-pass, low-pass, and input voltages may be summed, using a fourth amplifier, as shown in Figure 10.5. The output of the summing amplifier is

$$V_O = -\frac{R_{10}}{R_8}V_{LP} - \frac{R_{10}}{R_7}V_{BP} - \frac{R_{10}}{R_9}V_{IN} \tag{10.21}$$

and the resulting transfer function, obtained by substituting Equation 10.18 and 10.19 for V_{BP} and V_{LP}, respectively, is

$$\frac{V_O}{V_{IN}} = \frac{\frac{R_{10}}{R_8}\frac{1}{R_2R_4C_1C_2} + \frac{R_{10}}{R_7}\frac{s}{R_4C_1} - \frac{R_{10}}{R_9}\left(s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}\right)}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}} \tag{10.22}$$

Comparing this with the general biquadratic (for $m = 1, n = 1$):

$$T(s) = -K\frac{s^2 + cs + d}{s^2 + as + b} \tag{10.23}$$

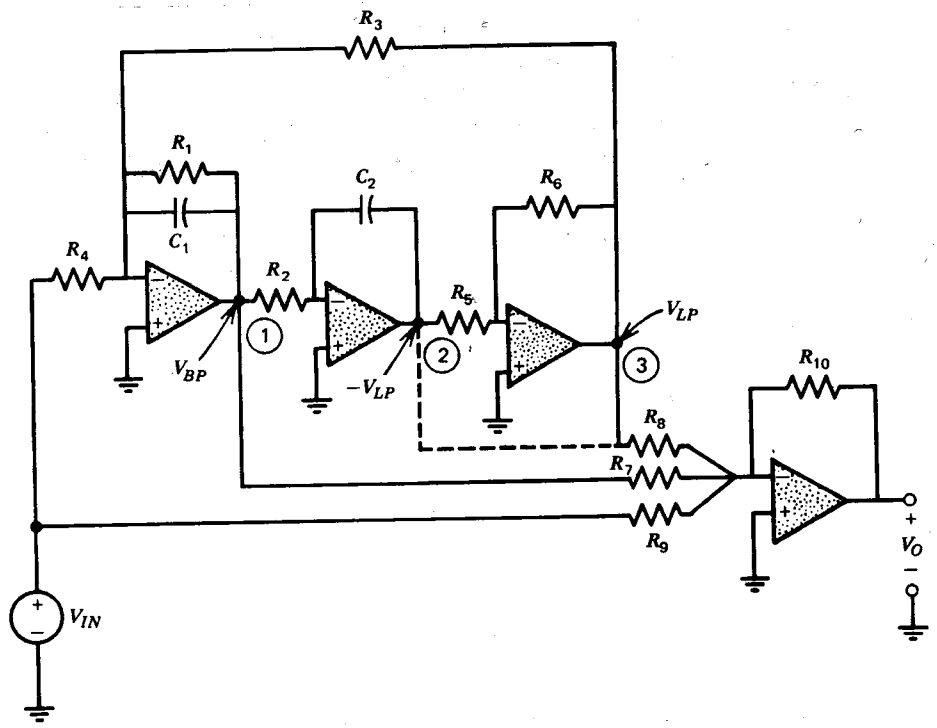


Figure 10.5 Summing four amplifier biquad.

the following relationships are obtained:

$$a = \frac{1}{R_1 C_1} \tag{10.24a}$$

$$b = \frac{1}{R_2 R_3 C_1 C_2} \tag{10.24b}$$

$$K = \frac{R_{10}}{R_9} \tag{10.24c}$$

$$c = \frac{1}{R_1 C_1} - \frac{R_9}{R_7}\frac{1}{R_4 C_1} = a - \frac{R_9}{R_7}\frac{1}{R_4 C_1} \tag{10.24d}$$

$$d = \frac{1}{R_2 R_3 C_1 C_2} - \frac{R_9}{R_8}\frac{1}{R_2 R_4 C_1 C_2} = b - \frac{R_9}{R_8}\frac{1}{R_2 R_4 C_1 C_2} \tag{10.24e}$$

We have five equations and ten elements. Therefore, five of the elements can be fixed. One choice for the fixed elements is

$$C_1 = 1 \qquad C_2 = 1 \qquad R_2 = R_3 = R \qquad R_7 = R_{10} = R \tag{10.25a}$$

Then the remaining elements are given by

$$R_1 = \frac{1}{a} \qquad R_2 = R_3 = \frac{1}{\sqrt{b}} \qquad R_4 = \frac{1}{K(a-c)}$$
$$R_7 = R_{10} = \frac{1}{\sqrt{b}} \qquad R_8 = \frac{a-c}{b-d} \qquad R_9 = \frac{1}{K\sqrt{b}} \tag{10.25b}$$

These synthesis equations yield nonegative element values for

$$a \geq c \qquad \text{and} \qquad b \geq d \tag{10.26}$$

The first inequality requires the zero to have a smaller real part than the pole. This condition is satisfied for all the approximation functions described in Chapter 4, since their zeros were constrained to lie on the $j\omega$ axis.* The second inequality requires that the magnitude of the pole frequency be larger than that of the zero frequency. This restriction can be removed by using V_2 instead of V_3 as the input to the summing amplifier (dotted lines in Figure 10.5). Then the output of the summer is

$$+\frac{R_{10}}{R_8} V_{LP} - \frac{R_{10}}{R_7} V_{BP} - \frac{R_{10}}{R_9} V_{IN} \tag{10.27}$$

It can easily be seen that the resulting synthesis equations will be the same as Equation 10.25, except in this case

$$R_8 = \frac{a-c}{d-b} \tag{10.28}$$

Thus, we see that the summing four amplifier biquad can be used to realize the general biquadratic function of Equation 10.1.

EXPERIMENT NO. 8 - Design of a Bipolar OTA Circuit

WARNING: I have started on redesigning this lab using MOSFET array transistors. If I complete the redesign before anyone does this lab, it will be superceded by the new exercise.

When an integrated circuit was being designed, it was once customary to breadboard it using standard chips with transistors similar to those expected to be made by the ultimate production technology. Now it is usually done by computer simulation alone, but you can still try one the old way. The point of breadboarding is to be sure that there are no undesirable operating modes for the device. It also gives the designer a chance to try the device in practical applications and to revise the specifications if necessary to make them more useful without having to commit to the large costs involved in a set of masks. Although some of the techniques for such breadboarding are not readily available to us, we do have two types transistor arrays (3 npn's and 2 pnp's on one chip) available.

Design and breadboard an IC circuit which is a voltage input to current output amplifier. (This type of amplifier is called an operational transconductance amplifier or OTA.) If v_1 and v_2 are two input voltages relative to ground and i_0 is an output current running through an arbitrary impedance to ground, then your circuit should realize the function $i_0 = A(v_1 - v_2)$ where A is a constant with units of conductance. If the amplifier output voltage is v_0 and the power supply is ± 12 V then this formula shall hold for $|\ v_0\ | \leq 10$ V and $|\ i_0\ | \leq 1.5$ ma. The common mode rejection ratio is to be ≥ 200 at 100 Hz. The input offset voltage is to be ≤ 10 mvolts; the common mode voltage ≥ ±7 volts; the maximum differential input voltage 5 volts; the minimum value of A = 0.4 amp/V and the minimum differential input impedance 30 kohms.

<u>WARNING: DO NOT USE</u> A
MILLIAMMETER OR A VOLTMETER
ON A MILLIAMPERE RANGE
TO MEASURE CURRENT IN THIS CIRCUIT

Milliammeters have very low input resistance. Connected between the wrong points in this circuit they can blow out an IC instantaneously. These integrated circuits are expensive so use them with care. Check wiring before applying power and ask a TA to check your circuit

configuration for safety. (He will not tell you if it is right, only if he thinks it would destroy an IC.) For current measurements use a voltmeter across a 1.5 K ohm resistor.

In class, in the discussion of operational amplifiers, we cover circuit configurations for all but the current amplifier. The creative part of the experiment is devising a **current output** stage that can both source and sink current. (**Hint:** The output can be the difference between a constant current and a unidirectional, variable current amplifier.)

A block diagram of the circuit is given below. A simple version of the circuit can be built with 8 transistors from 2 chips. The super fanciest version might take as many as 20 transistors. Build the circuit according to the rules of the next paragraph and test all the above parameters except the maximum input voltage. We expect to have an automated arrangement for measuring the differential gain and input offset. A circuit is given below for measuring the CMRR. It may give you ideas for testing other parameters.

Since this is an IC design, there are certain restrictions on the components that lead to the following rules:

1. No capacitors bigger than 40 pf may be used.

2. Resistors fall into two classes according to the voltage across them. Class 1 resistors may have any voltage across them, but no individual resistor may exceed 39 K and the sum of all Class 1 resistors in the circuit may not exceed 70 K. Class 2 resistors may only have ≤ 3 volts across them, but may have any value from 2 K to 100 K with essentially no restriction on the total number.

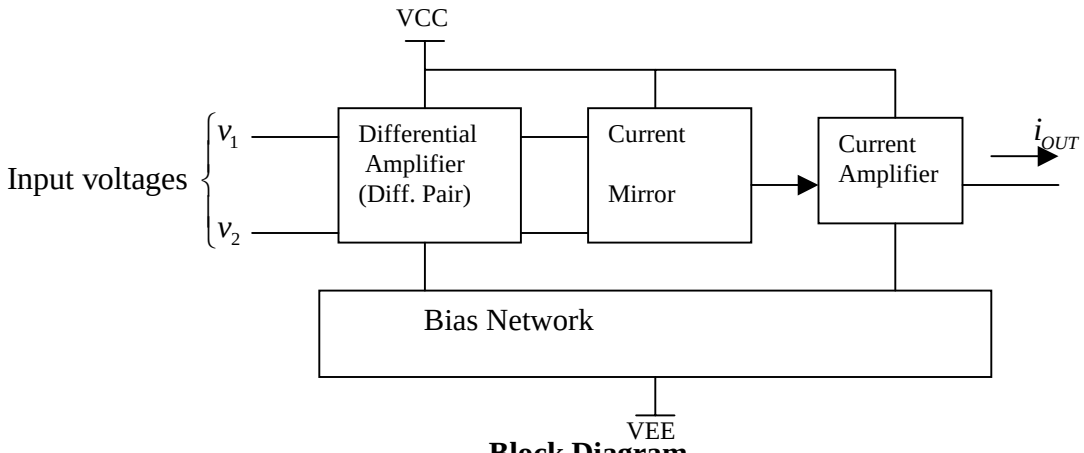
Also, in using the CA3096 transistor arrays, **you must connect the substrate (pin 16) to the most negative voltage** in the circuit in order to keep the transistors isolated. Those of you who find the problem interesting might optionally consider how to add the following features to the circuit:

1. Two nearly identical outputs instead of one, so that one might be a true current output while the other is used for feedback. Alternatively, some OTAs have two differential outputs, that is, one output is the negative of the other.

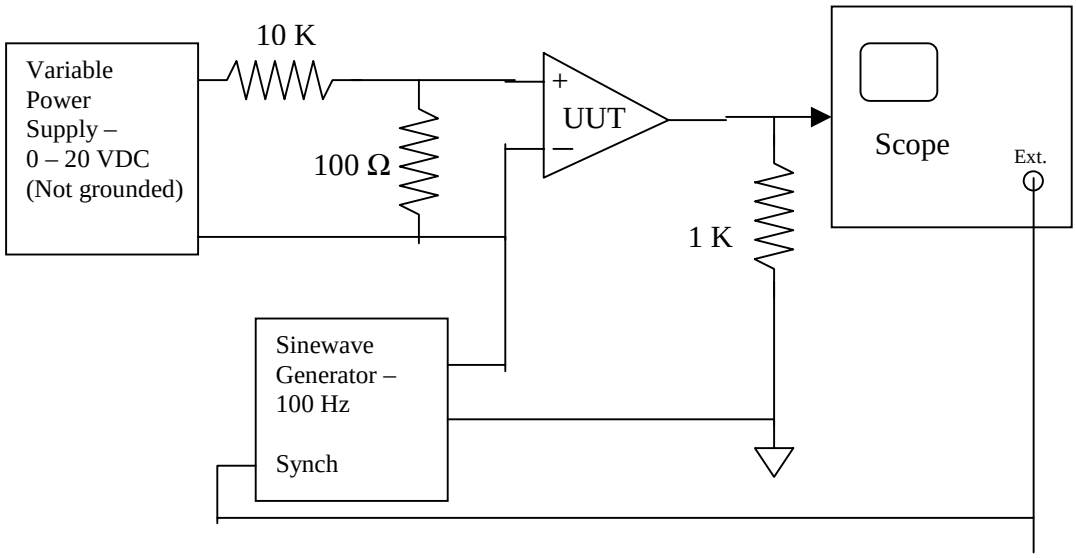
2. Ten times as much input impedance with three times the overall gain.

3. Provision for external adjustment of the input offset voltage.

4. Higher output current and lower power dissipation with two more current mirrors instead of the current amplifier.



Block Diagram



Common Mode Rejection Test Circuit

APPENDIX: DEVICE DATA SHEETS

1N4154
2N2222A
2N3440
2N3904
ALD1106
ALD1107
CA3086
CA3096
LF353N

Note: these are abbreviated datasheets. Complete datasheets are on the class website.

FAIRCHILD SEMICONDUCTOR™

1N4154

DISCRETE POWER AND SIGNAL TECHNOLOGIES

General Description:

The high breakdown voltage, fast switching speed and high forward conductance of this diode packaged in a DO-35 miniature Glass Axial leaded package makes it desirable also as a general purpose diode.

High Conductance Fast Diode

Features:

- 500 milliwatt Power Dissipation package.
- Fast Switching Speed,
- Typical capacitance less than 1.0 picofarad.

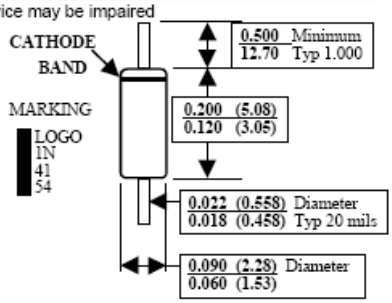
Ordering:

- 13 inch reel, 50 mm (T50R) & 26 mm (T26R) Tape; 10,000 units per reel.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

Sym	Parameter	Value	Units
T_{stg}	Storage Temperature	-65 to +200	°C
T_J	Operating Junction Temperature	175	°C
P_D	Total Power Dissipation at T_A = 25°C	500	mW
	Linear Derating Factor from T_A = 25°C	3.33	mW/°C
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient	300	°C/W
W_{IV}	Working Inverse Voltage	35	V
I_O	Average Rectified Current	100	mA
I_F	DC Forward Current (IF)	300	mA
i_r	Recurrent Peak Forward Current (IF)	400	mA
$i_{F(surge)}$	Peak Forward Surge Current (IFSM) Pulse Width = 1.0 second	1.0	Amp
	Pulse Width = 1.0 microsecond	4.0	Amp

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired



Electrical Characteristics TA = 25°C unless otherwise noted

SYM	CHARACTERISTICS	MIN	MAX	UNITS	TEST CONDITIONS
B_V	Breakdown Voltage	35		V	I_R = 5.0 uA
I_R	Reverse Leakage		100	nA	V_R = 25 V
			100	uA	V_R = 25 V, T_A = 150°C
V_F	Forward Voltage		1.0	V	I_F = 30 mA
C_T	Capacitance		4.0	pF	V_R = 0.0 V, f = 1.0 MHz
T_{RR}	Reverse Recovery Time		4.0	ns	I_F = 10 mA V_R = 6.0 V I_{RR} = 1.0 mA, R_L = 100 ohms

Revision A - September 21, 1998

MAXIMUM RATINGS

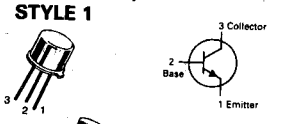
Rating	Symbol	2N2219 2N2222	2N2218A 2N2219A 2N2222A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CBO}	60	75	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	6.0	Vdc
Collector Current — Continuous	I_C	800	800	mAdc
		2N2218A 2N2219,A	2N2222,A	
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.8 4.57	0.4 2.28	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.1	1.2 6.85	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N2218A 2N2219,A	2N2222,A	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	219	437.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	58	145.8	°C/W

2N2218A,2N2219,A★ 2N2222,A★

2N2218, A/2N2219,A
CASE 79-04
TO-39 (TO-205AD)
STYLE 1



A/2N2222,A
CASE 22-03
TO-18 (TO-206AA)
STYLE 1

GENERAL PURPOSE TRANSISTORS
NPN SILICON

★2N2219A and 2N2222A are Motorola designated preferred devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	Non-A Suffix A-Suffix	$V_{(BR)CEO}$	30 40	— —	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	Non-A Suffix A-Suffix	$V_{(BR)CBO}$	60 75	— —	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	Non-A Suffix A-Suffix	$V_{(BR)EBO}$	5.0 6.0	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	A-Suffix	I_{CEX}	—	10	nAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C) (V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	 Non-A Suffix A-Suffix Non-A Suffix A-Suffix	I_{CBO}	 — — — —	 0.01 0.01 10 10	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	A-Suffix	I_{EBO}	—	10	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	A-Suffix	I_{BL}	—	20	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc)(1) (I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = −55°C)(1) (I_C = 150 mAdc, V_{CE} = 10 Vdc)(1)	 2N2218A 2N2219,A, 2N2222,A 2N2218A 2N2219,A, 2N2222,A 2N2218A 2N2219,A, 2N2222,A 2N2218A 2N2219,A, 2N2222,A 2N2218A 2N2219,A, 2N2222,A	h_{FE}	 20 35 25 50 35 75 15 35 40 100	 — — — — — — — — 120 300	—

2N2218A 2N2219,A 2N2222,A

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)(1)	2N2218A		20	—	
	2N2219,A, 2N2222,A		50	—	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)(1)	2N2219, 2N2222		30	—	
	2N2218A		25	—	
	2N2219A, 2N2222A		40	—	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	Non-A Suffix		—	0.4	
	A-Suffix		—	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)	Non-A Suffix		—	1.6	
	A-Suffix		—	1.0	
Base-Emitter Saturation Voltage(1)		$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	Non-A Suffix		0.6	1.3	
	A-Suffix		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)	Non-A Suffix		—	2.6	
	A-Suffix		—	2.0	
SMALL-SIGNAL CHARACTERISTICS					
Current Gain — Bandwidth Product(2)		f_T			MHz
(I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	All Types, Except		250	—	
	2N2219A, 2N2222A		300	—	
Output Capacitance(3)		C_{obo}	—	8.0	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)					
Input Capacitance(3)		C_{ibo}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	Non-A Suffix		—	30	
	A-Suffix		—	25	
Input Impedance		h_{ie}			kohms
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		1.0	3.5	
	2N2219A, 2N2222A		2.0	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		0.2	1.0	
	2N2219A, 2N2222A		0.25	1.25	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		—	5.0	
	2N2219A, 2N2222A		—	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		—	2.5	
	2N2219A, 2N2222A		—	4.0	
Small-Signal Current Gain		h_{fe}			—
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		30	150	
	2N2219A, 2N2222A		50	300	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		50	300	
	2N2219A, 2N2222A		75	375	
Output Admittance		h_{oe}			μmhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		3.0	15	
	2N2219A, 2N2222A		5.0	35	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A		10	100	
	2N2219A, 2N2222A		15	200	
Collector Base Time Constant		$r_b'C_c$	—	150	ps
(I_E = 20 mAdc, V_{CB} = 20Vdc, f = 31.8 MHz)	A-Suffix				
Noise Figure		NF	—	4.0	dB
(I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 kohm, f = 1.0 kHz)	2N2222A				
Real Part of Common-Emitter High Frequency Input Impedance		$Re(h_{ie})$	—	60	Ohms
(I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 300 MHz)	2N2218A, 2N2219A 2N2222A				

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.
(3) 2N5581 and 2N5582 are Listed C_{cb} and C_{eb} for these conditions and values.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = −0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 12)	t_d	—	10	ns
Rise Time		t_r	—	25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 13)	t_s	—	225	ns
Fall Time		t_f	—	60	ns
Active Region Time Constant (I_C = 150 mAdc, V_{CE} = 30 Vdc) (See Figure 11 for 2N2218A, 2N2219A, 2N2221A, 2N2222A)		T_A	—	2.5	ns

FIGURE 1 – NORMALIZED DC CURRENT GAIN

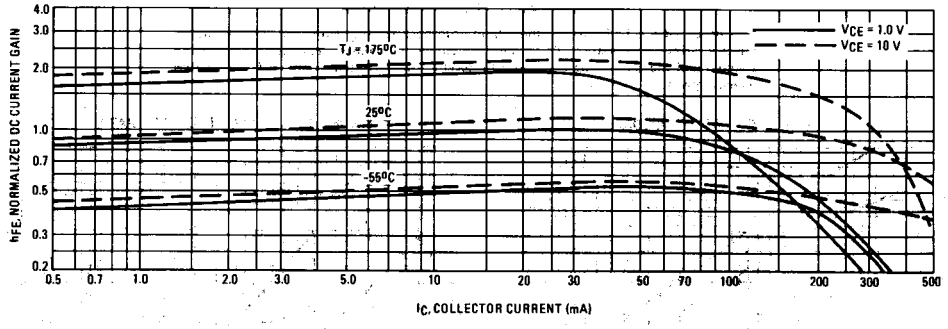
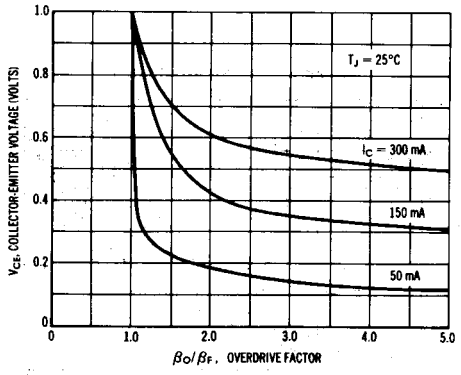


FIGURE 2 – COLLECTOR CHARACTERISTICS IN SATURATION REGION



This graph shows the effect of base current on collector current. β_o (current gain at the edge of saturation) is the current gain of the transistor at 1 volt, and β_f (forced gain) is the ratio of I_c/I_w in a circuit.

EXAMPLE: For type 2N2219, estimate a base current (I_w) to insure saturation at a temperature of 25°C and a collector current of 150 mA.

Observe that at I_c = 150 mA an overdrive factor of at least 2.5 is required to drive the transistor well into the saturation region. From Figure 1, it is seen that h_{fe} @ 1 volt is approximately 0.62 of h_{fe} @ 10 volts. Using the guaranteed minimum gain of 100 @ 150 mA and 10 V, β_o = 62 and substituting values in the overdrive equation, we find:

$$\frac{\beta_o}{\beta_f} = \frac{h_{fe}\ @\ 1.0\ V}{I_c/I_w} \qquad 2.5 = \frac{62}{150/I_w} \qquad I_w \approx 6.0\ mA$$

2N3439
2N3440

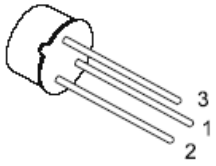
SILICON NPN TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES
- NPN TRANSISTOR

DESCRIPTION

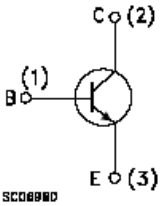
The 2N3439 and 2N3440 are silicon epitaxial planar NPN transistors in jedec TO-39 metal case designed for use in consumer and industrial line-operated applications.

These devices are particularly suited as drivers in high-voltage low current inverters, switching and series regulators.



TO-39

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		2N3439	2N3440	
V_{CBO}	Collector-Base Voltage (I_E = 0)	450	300	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	350	250	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	7		V
I_C	Collector Current	1		A
I_B	Base Current	0.5		A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	10		W
P_{tot}	Total Dissipation at $T_{amb} \leq 50$ °C	1		W
T_{stg}	Storage Temperature	-65 to 200		°C
T_j	Max. Operating Junction Temperature	200		°C

2N3903, 2N3904

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 2) (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	–	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{BL}	–	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{CEX}	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	
Collector–Emitter Saturation Voltage (Note 2)		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc			–	0.3	
Base–Emitter Saturation Voltage (Note 2)		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903		250	–	
	2N3904		300	–	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		1.0	8.0	
	2N3904		1.0	10	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		0.1	5.0	
	2N3904		0.5	8.0	
Small–Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		50	200	
	2N3904		100	400	
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903		–	6.0	
	2N3904		–	5.0	
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc,	t_d	–	35	ns
Rise Time	I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	t_r	–	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, 2N3903	t_s	–	175	ns
	I_{B1} = I_{B2} = 1.0 mAdc) 2N3904		–	200	
Fall Time		t_f	–	50	ns

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

ADVANCED LINEAR DEVICES, INC.

ALD1106/ALD1116

QUAD/DUAL N-CHANNEL MATCHED PAIR MOSFET ARRAY

GENERAL DESCRIPTION

The ALD1106/ALD1116 are monolithic quad/dual N-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1106/ALD1116 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. The ALD1106/ALD1116 are building blocks for differential amplifier input stages, transmission gates, and multiplexer applications, current sources and many precision analog circuits.

FEATURES

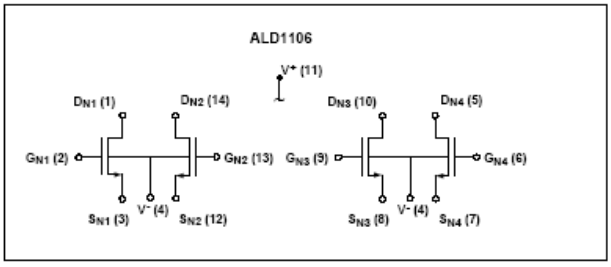
- Low threshold voltage of 0.7V
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- $10^{14}\Omega$ typical
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10^9
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1116 DA	ALD1116 PA	ALD1116 SA
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1106 DB	ALD1106 PB	ALD1106 SB

* Contact factory for industrial temperature range.

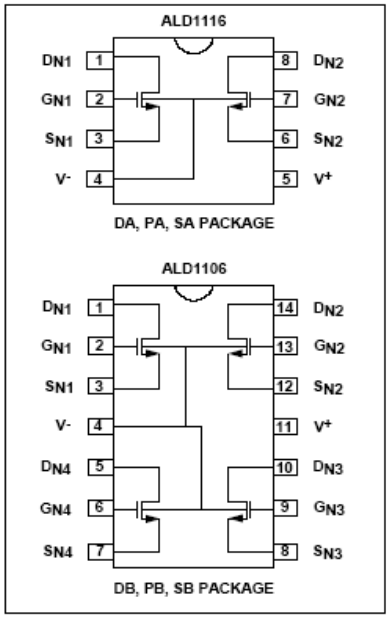
BLOCK DIAGRAM



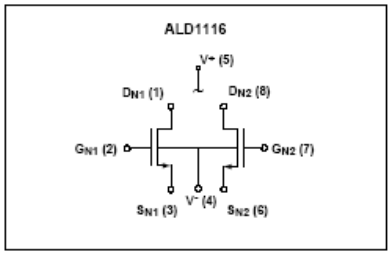
APPLICATIONS

- Precision current mirrors
- Precision current sources
- Voltage choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog signal processing

PIN CONFIGURATION



BLOCK DIAGRAM



ADVANCED LINEAR DEVICES, INC.

ALD1107/ALD1117

QUAD/DUAL P-CHANNEL MATCHED PAIR MOSFET ARRAY

GENERAL DESCRIPTION

The ALD1107/ALD1117 are monolithic quad/dual P-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1107/ALD1117 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for precision analog switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC operating environment. The ALD1107/ALD1117 are builiding blocks for differential amplifier input stages, transmission gates, multiplexer applications, current sources, current mirrors and other precision analog circuits.

FEATURES

- Low threshold voltage of -0.7
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- $10^{14}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10^9
- Low input and output leakage currents

ORDERING INFORMATION

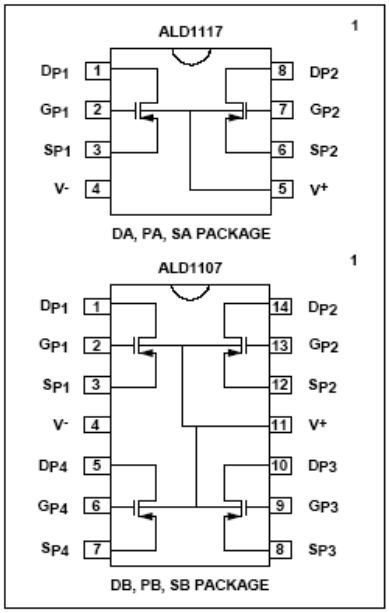
Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1117 DA	ALD1117PA	ALD1117 SA
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1107 DB	ALD1107 PB	ALD1107 SB

* Contact factory for industrial temperature range.

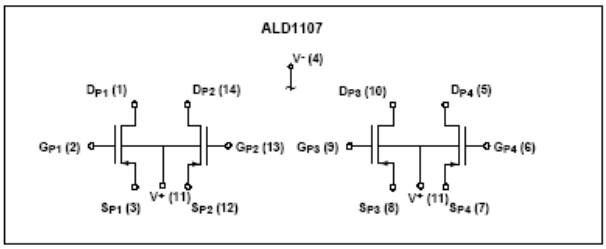
APPLICATIONS

- Precision current sources
- Precision current mirrors
- Voltage Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Precision analog signal processing

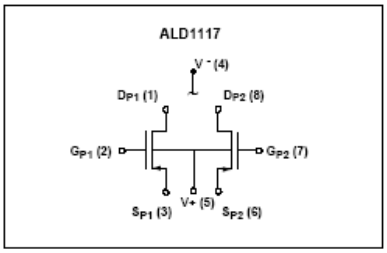
PIN CONFIGURATION



BLOCK DIAGRAM



BLOCK DIAGRAM



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CA3086

Data Sheet **August 2003** **FN483.5**

General Purpose NPN Transistor Array

The CA3086 consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

Ordering Information

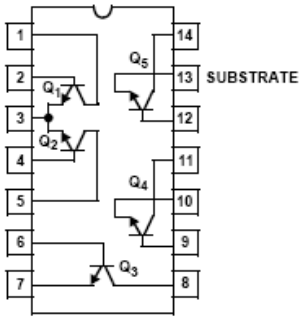
PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
CA3086	-55 to 125	14 Ld PDIP	E14.3
CA3086M96 (3086)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Applications

- Power Applications from DC to 120MHz
- General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

Pinout

CA3086 (PDIP, SOIC)
TOP VIEW



National Semiconductor

December 2003

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

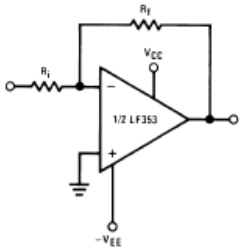
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

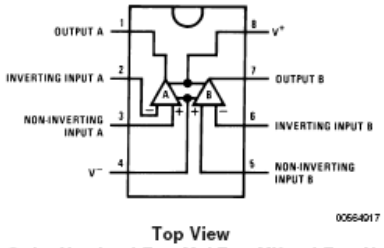
■ Internally trimmed offset voltage:	10 mV
■ Low input bias current:	50pA
■ Low input noise voltage:	25 nV/√Hz
■ Low input noise current:	0.01 pA/√Hz
■ Wide gain bandwidth:	4 MHz
■ High slew rate:	13 V/μs
■ Low supply current:	3.6 mA
■ High input impedance:	$10^{12}\Omega$
■ Low total harmonic distortion :	≤0.02%
■ Low 1/f noise corner:	50 Hz
■ Fast settling time to 0.01%:	2 μs

Typical Connection



Connection Diagram

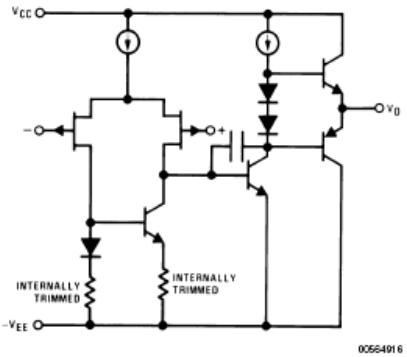
Dual-In-Line Package



Top View
Order Number LF353M, LF353MX or LF353N
See NS Package Number M08A or N08E

Simplified Schematic

1/2 Dual



BI-FET II™ is a trademark of National Semiconductor Corporation.

 DS005649 www.national.com

LF353

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1000V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 5, 6)		25	100	pA
		$T_j \leq$70°C			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 5, 6)		50	200	pA
		$T_j \leq$70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω,		16		nV/$\sqrt{Hz}$
		f=1000 Hz				
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/$\sqrt{Hz}$