Engineering 1620 – Spring 2016

SPICE Assignment – Design of a Two-Stage MOSFET Opamp

Introduction: Design a simple opamp for use within an integrated circuit, estimate its low-frequency performance, and then compare your hand calculations to the response calculated for the circuit using SPICE. Such amplifiers for on-chip filters and other mixed-signal applications often use a two-stage topology similar to the example I gave in class. The first stage is a differential pair with a current mirror load and is biased by a suitable current source. The second stage is a common source amplifier with a current source load. When wider bandwidth or higher gain is needed, cascoding the current sources or even the differential pair is used.

This scheme works well when the load on the amplifier is limited to a high resistance and low total capacitance from on-chip connections. It does not work very well for off-chip connections since the capacitances associated with such connections are usually tens of picofarads and severely limit the frequency response. Worse, off-chip loads vary with the user application and a larger-than-intended capacitive load can cause an operational amplifier to become unstable and too low a resistance will kill the amplifier gain. On-chip loads are better defined. Recognizing this reality, this project is strictly designed for on-chip applications and has a well-defined range of impedance for the load.

The design goal is an amplifier that operates and is simulated with an output load of 20K in parallel with 20pf. The resistor load is tied to 2.5 volts DC to simulate operation in the middle of the output voltage range. Figure 2 shows a schematic of this dummy load. The amplifier also needs to operate properly with the capacitive part of the load reduced to 2pf. With either of these loads, the principal properties of the amplifier should meet the requirements:

- DC Gain ≥ 80 DB (X10,000)
- Phase margin at 0 DB (unity) gain ≥ 60 degrees
- The gain-bandwidth product should be as high as possible with the proper phase margin
- Power supply current $I_{DD} \leq 0.9$ mA
- Common mode rejection ratio > 80 DB
- Output voltage range no less than 2.5 ± 1.5 volts
- Input common mode voltage range 0 to 3 volts minimum
- Slew rate $\geq 4 \cdot 10^6$ V/sec
- Dominant pole position as high as practical given the phase margin requirement, meaning that you are trying to maximize the gain-bandwidth product.
- The amplifier still meets these specifications if the load capacitance is reduced to 2 pf.

This opamp is designed to be built in a process that can make transistors with gate lengths, L, as short as 0.5 microns. Short devices have low values of output resistance and you will need to choose larger values for L.

To use the transistor models for this process, you will need to add the library
P:\programs\MentorGraphics\PCBLibraries\SPICE_Libraries\MOSModels0_5Um.lib to your
deck. Some of the process parameters for hand calculations are given in the table below but cal-
culations for gm and ro are a little more complicated than what we did in class and are discussed
in the Appendix.

The process parameters for approximate hand calculations are:

Parameter	N-Channel	P-Channel
V_{TH0}	0.70 volts	0.95 volts
$K = \mu C_{OX} /2$	75 μA/V^2	26 μA/V^2
C_{OX} (fd/m^2)	$3.6 \cdot 10^{-3}$	$3.6 \cdot 10^{-3}$
Channel length modulation constant: $\lambda = \dfrac{1}{V_A}$ See Appendix I as this parameter depends on L and Vov		

In designing your circuit you may use:

- Any number of transistors with your choice of device length and width. (Note: while the
  process can make devices with L = 0.5 um, these have low voltage gain and are used for
  digital designs. You will want to use longer ones.) Because of manufacturing constraints,
  all values of L and W must be integer multiples of 0.25 um.
- Your first stage differential amplifier transistor pair are to be PMOS devices and the
  manufacturing process is N-well so that pair can have their body terminals tied to the
  source terminals.
- You may use one ideal DC current source of 50 microamperes to bias your circuit.
- You may use one discrete capacitor with value $\leq 12\,pf$ for frequency compensation.
- You may use a discrete resistor $\leq 3\,K$ in series with the compensation capacitor to im-
  prove your phase margin and bandwidth.

Implicit in these requirements is the assumption that you will give the amplifier a dominant pole
by exploiting the Miller effect with a capacitor and resistor in series between the output and input
of the common source second stage. The requirement for the best possible bandwidth with a
minimum phase margin of 60 degrees means you will have to experiment with the resistor and
capacitor values to adjust the frequency response.

Simulations to characterize the completed design are done with the input common mode voltage
= 2.5 volts. The minimum set of such simulations is:

- .OP for quiescent conditions
- Bode plots for full load (20pf) and light load (2pf) of:
    - Small-signal frequency response of both stages to a differential signal
    - Small-signal common mode response
- A .DC sweep over the differential input (VOFFSET in the figure) to show the output
  voltage range of the circuit.

Optional Simulations:

- Test the input common mode range by a .DC sweep of the VCMDC source from 0 to 3.0 volts checking that the output voltage of the first stage remains within 0.7 volts of its initial value. (This is a very liberal specification. My design held the change in output DC voltage to under 0.1 volts.) If you use a cascoded current mirror, then it may be difficult to meet the preference for a common mode range that includes the ground rail. In that case determine how close you can get to that voltage before the output changes significantly.

- Connect the opamp as a unity gain buffer and drive its input with a step function of rise time = 10 ns from 1.5 volts to 2.5 volts at the input. What is the rise time of the step and the maximum of $\dfrac{dv_{OUT}}{dt}$?

Figure 1shows the very simplest possible input circuit and a way of using sources as stimulus for both common mode and differential excitation. VDELTA is the AC source for open-loop frequency response simulation. VDCCM sets the DC common mode voltage and VCM is an AC source used to determine the common mode gain and rejection ratio by simulating a 1.0 volt AC common mode input. By default, the DCCM level should be 2.5 volts during simulation of the open-loop differential gain and the common mode gain. VDELTA and VCM should never both be turned on at the same time.
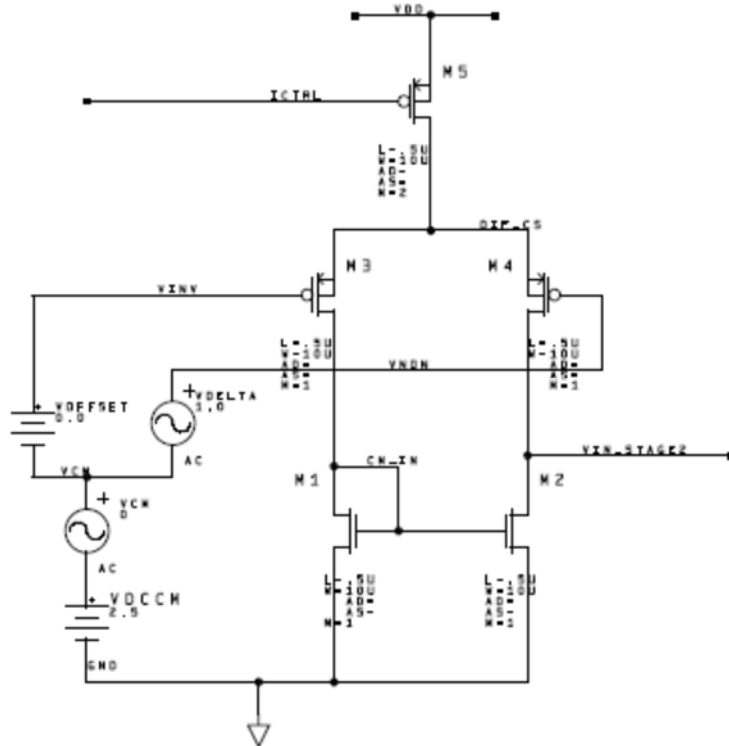

Figure 1: Simple Differential First Stage with Sources for SPICE Simulations. VCM set to 1.0 volts simulates small signal common mode measurement. VDELTA set to 1.0 volts simulates dsmall signal differential open-loop grsponse.
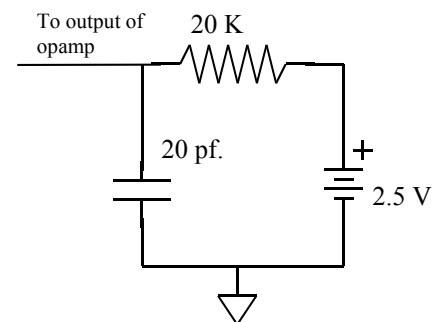

Figure 2: Dummy Load Simulates the Operating Load for Testing Opamp

Your report should include:
1. A very brief introduction describing the circuit topology and whether you used any cascoding to improve gain or bandwidth. Emphasize how much the circuit exceeds minimum requirements.
2. A clear schematic on white background annotated with the L and W values of all devices.
3. A table of simulated quiescent conditions for VGS, VDS, Vov, and ID. Compare these to your target values of ID and Vov. You infer the simulated Vov from the simulation of VGS and the process data given above.
4. Compare your hand calculations of the low frequency stage gains, the overall gain, and the CMRR with the SPICE results. (For CMRR see Appendix II.) Do the same for slew rate and output voltage range. Show enough work including relevant formulas that it is clear how you did the calculation. A table of side by side values is a nice way to present that data.
5. A final table showing the properties of the finished amplifier including the measured gains (again), the slew rate, dominant pole frequency, unity gain frequency, the phase margin at unity gain, and the range of voltage over which the output follows the input without saturation or clipping.

Procedure:

1. You will concentrate first on sizing the transistors and biasing the circuit. Start by selecting lengths for your transistors. While all transistors that must match each other are the same length, not all transistors need to be the same. Lengths must be a multiple of 0.25 microns because of manufacturing constraints. Output resistance (r_o) depends on the channel length because its primary cause is channel length modulation. The change in length due to a change in VDS decreases as a fraction of the total length when the device gets longer. The transconductance also degrades for very short devices. Unfortunately LT Spice does not report its calculated small signal device parameters so I have tabulated some data to make it easier for you to select L and to estimate g_m and r_o. The Appendix has a graph of how the maximum voltage gain for a common source amplifier varies with the channel length that suggests a range of L from 1.25 to 2.0 um is probably optimal.

2. Next select device overvoltages. The device "overvoltage" is defined as $V_{OV} \equiv V_{GS} - V_{TH}$. This term appears directly in the drain current equation and is also the approximate VDSAT of the transistor. You choose the initial overvoltages based on two rules of thumb. There is a generally accepted range for the overvoltage from -0.05 volts to about .4 volts that represents reasonable tradeoffs between noise, gain, and frequency response. Lower overvoltages raise gains but result in larger transistors. Low Vov in the input transistors lowers noise, but it results in higher noise if used in the current mirror. So the second rule of thumb is that the current mirror overvoltage should be approximately twice that of the differential pair. (A negative overvoltage represents subthreshold operation and requires very wide transistors.)

3. Choose device drain currents based on the available bias source exploiting the ability to make copies of the original bias current. The second stage current will be determined by the need to drive the 20 K load resistor in addition to the output resistances of the common source topology. The basic formula for drain current then sets the widths of the devices.

4. If the simulated low frequency gain is sufficient, then set the resistance in series with the compensation capacitor to a trial value twice the inverse of the transconductance of the common source amplifier device. Set a trial value of compensation capacitance and iterate the compensation in SPICE to optimize the gain-bandwidth with unity gain phase margin (60 degrees minimum).

5. Tabulate all the required simulations and consider doing the optional inverter test.

Hints and comments:

*   You need devices with varying widths for the different currents in each part of your circuit. You make wide transistors by paralleling several copies of a small transistor so that current ratios are precise. SPICE allows you to do this with a single symbol by attaching the property "m=10"to the symbol to mean 10 transistors of that size in parallel. Use m instead of proliferating transistor symbols to create large devices.

*   Be careful about suffixes on numerical values. All lengths and areas in SPICE are in meters or square meters so to specify microns you need the suffix U and for areas you usually need P after a product in square microns. You get crazy results if you forget.

*   In the figure showing the use of sources for signals in simulation, the DC voltage VOFFSET can be used to sweep the input range in 50 uV steps to see the output range of the amplifier. It can also be set to a small value to offset any mismatches in the circuit that result in an output much different from 2.5 volts during small signal simulation.

### Appendix I: Selecting Device Length and Estimating gm and ro

In circuits with no discrete resistors, the voltage gain is largely determined by transistor output resistances. That resistance is caused by channel length modulation and the change in length due to a change in VDS decreases as a fraction of the total length when the device gets longer. The larger L is the larger r_O is. The transconductance is directly proportional to the drain current for a given device length and overvoltage. Similarly the output resistance is inversely proportional to I_D. The product of transconductance with output resistance, $g_m r_O$, is a dimensionless figure of merit for a device. From our MOSFET I-V approximation with long-channel devices at high Vov $g_m r_O \approx \dfrac{2}{\lambda V_{OV}}$. Both λ and g_m have a more complex relationship to length and overvoltage in the SPICE model than we assumed in class. This Appendix makes the real relationship easier to use

for hand calculations.   The $g_m r_O$ product represents the voltage gain for a transistor that is bi-ased with an ideal current source and has no other load. Thus it is the highest possible voltage gain for the transistor.
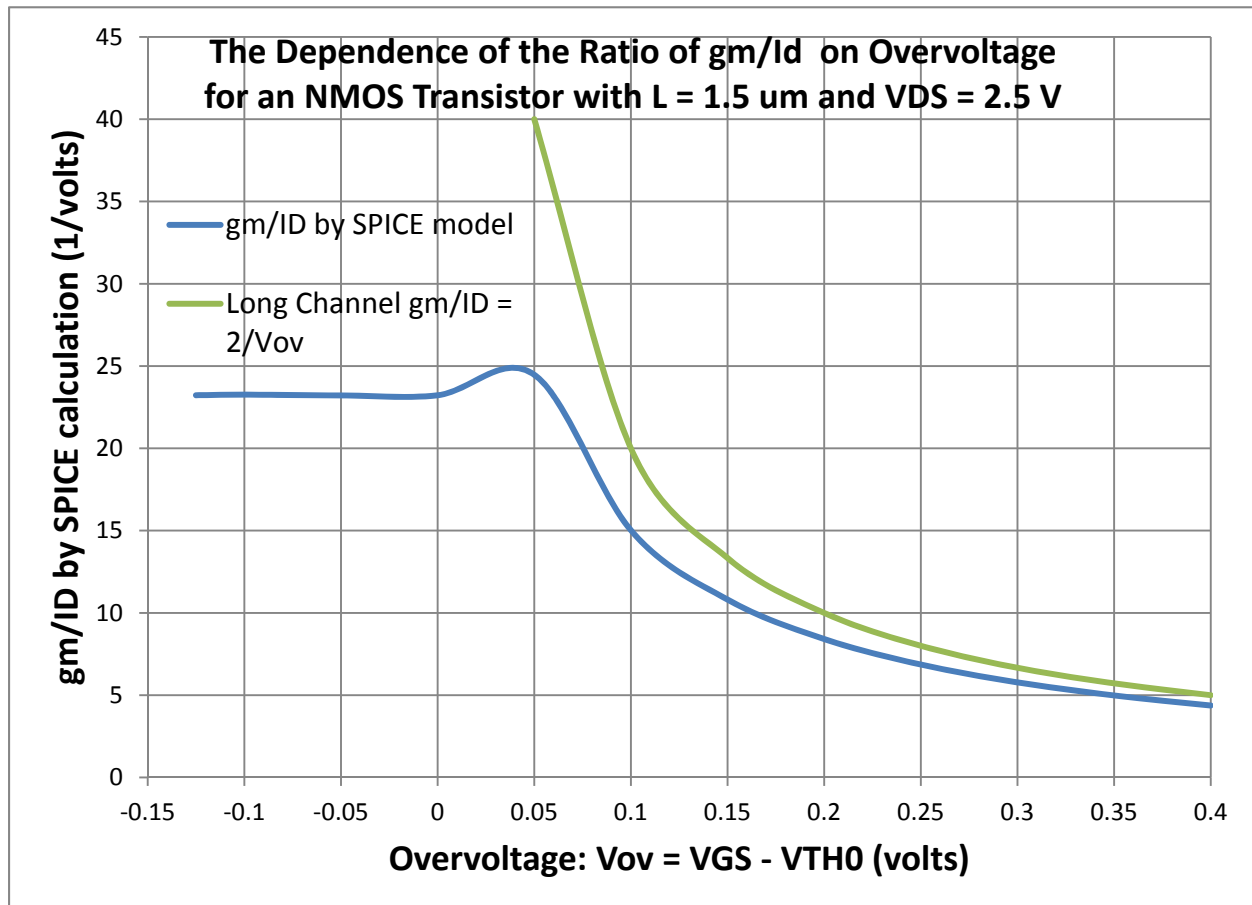
Here is a plot of that figure of merit - the ideal, common-source, voltage gain - for N and P chan-nel devices at several different overvoltages as a function of channel length. Notice that this gain is independent of V$_{OV}$ for P-channel devices but not for NMOS transistors. If a common source transistor is mated with a current source with comparable output resistance, then the resulting stage gain will be roughly half the ideal gain. Your amplifier needs to have gain > 80 DB (X10,000) and it will probably have a second stage gain in the range of 30 to 40 DB. (With the 20 K load and the supply current limitation any higher gain is hard to get.)   That sets a minimum target gain for the first stage and the ideal gains of the figure should suggest a starting point for selecting L. Second stage lengths probably are determined by current matching requirements. Keep in mind that is does not make sense to go much longer in L than necessary as the area of the circuit grows proportionately to L^2 , increasing cost and decreasing bandwidth.

Figure of Merit for NMOS Transistors: Maximum Ideal Voltage Gain = gm*ro
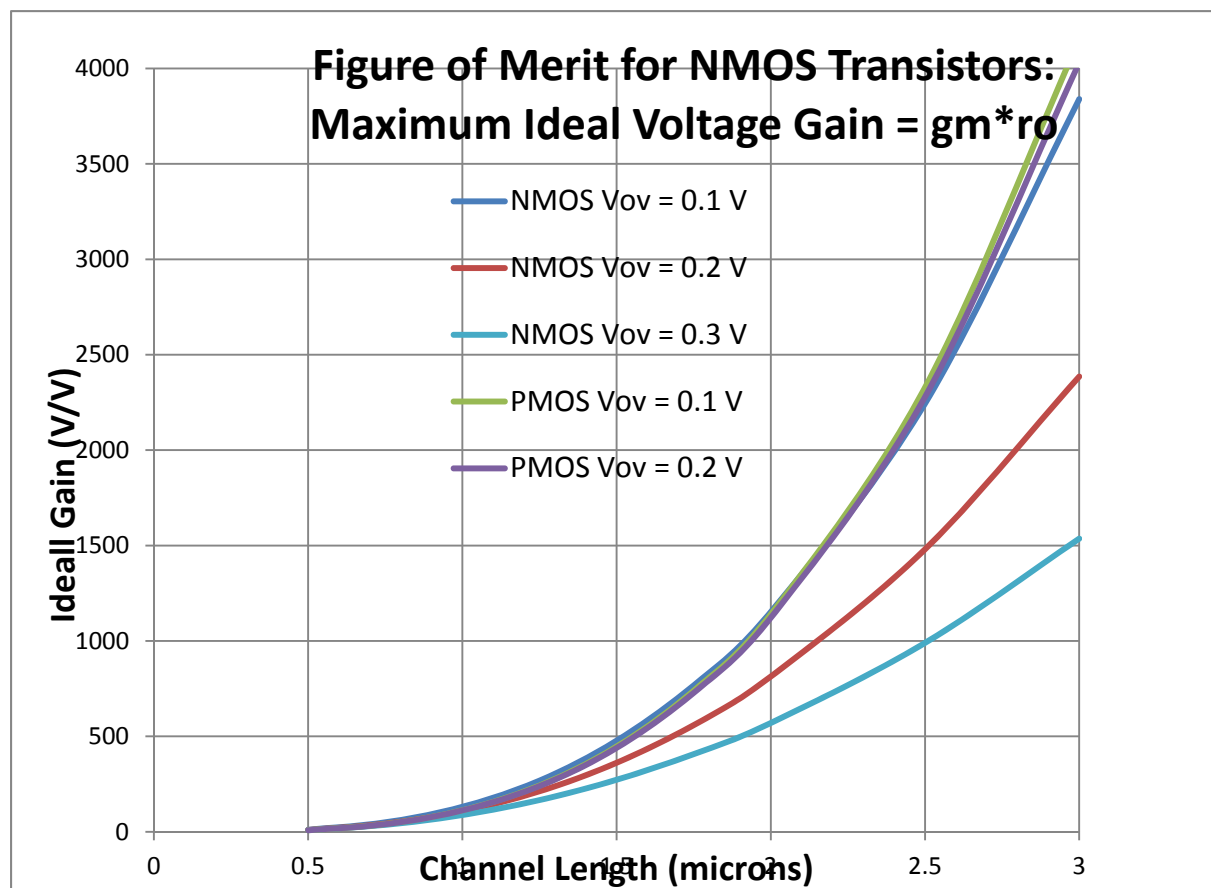
To calculate the low frequency stage gains you need a way to estimate g_m and r_o for each tran-sistor separately. In class and in Razavi we often use the simple relation that $g_m = \dfrac{2I_D}{V_{OV}}$. Unfortu-nately this relation is not helpful when V$_{OV}$ is low. The proportionality with I$_D$ is still true but the

coefficient becomes a more complex function of overvoltage when $V_{OV} \leq 0.3$ volts. The next graph shows that relationship for an NMOS device under very specific conditions. However, the relation is essentially independent of L for $L \geq 1.0$ microns. The same value for the coefficient holds for PMOS devices as well. I do not understand the hump in the curve and suspect it is an error in the SPICE model or model parameters. Notice the deviation from the relation $g_m = \dfrac{2I_D}{V_{OV}}$ that is plotted on the green curve. The way the ratio levels off as the device enters subthreshold operation reflects the fact that a current exponentially dependent on a voltage has a constant ratio of g_m to ID. That ratio is $\dfrac{q}{nkT}$ where n is the ideality factor for the device.

Estimating the output resistance of a device requires a value for the λ parameter in the device current equation. ($r_O = \dfrac{1 + \lambda V_{DS}}{\lambda I_D}$) For PMOS devices, λ depends primarily on the length L. The table below gives λ from SPICE simulations for several candidate values of L.

Dependence of λ on Channel Length, L, for P-channel MOSFETs	
Channel Length (microns)	λ
1	0.079
1.25	0.043
1.5	0.026
1.75	0.017
2	0.012
2.5	0.006
3	0.004

The output resistance of NMOS devices in this process is dependent on both L and Vov. The graph below shows the Vov dependence for a 1.5 micron long device. Estimate the value of lambda for other values of L by multiplying the value from this graph by 0.7 for L = 1.75 microns and by 0.6 for L = 2.0 microns.

Lambda for NMOS Transistors with L = 1.5 um vs Overvoltage
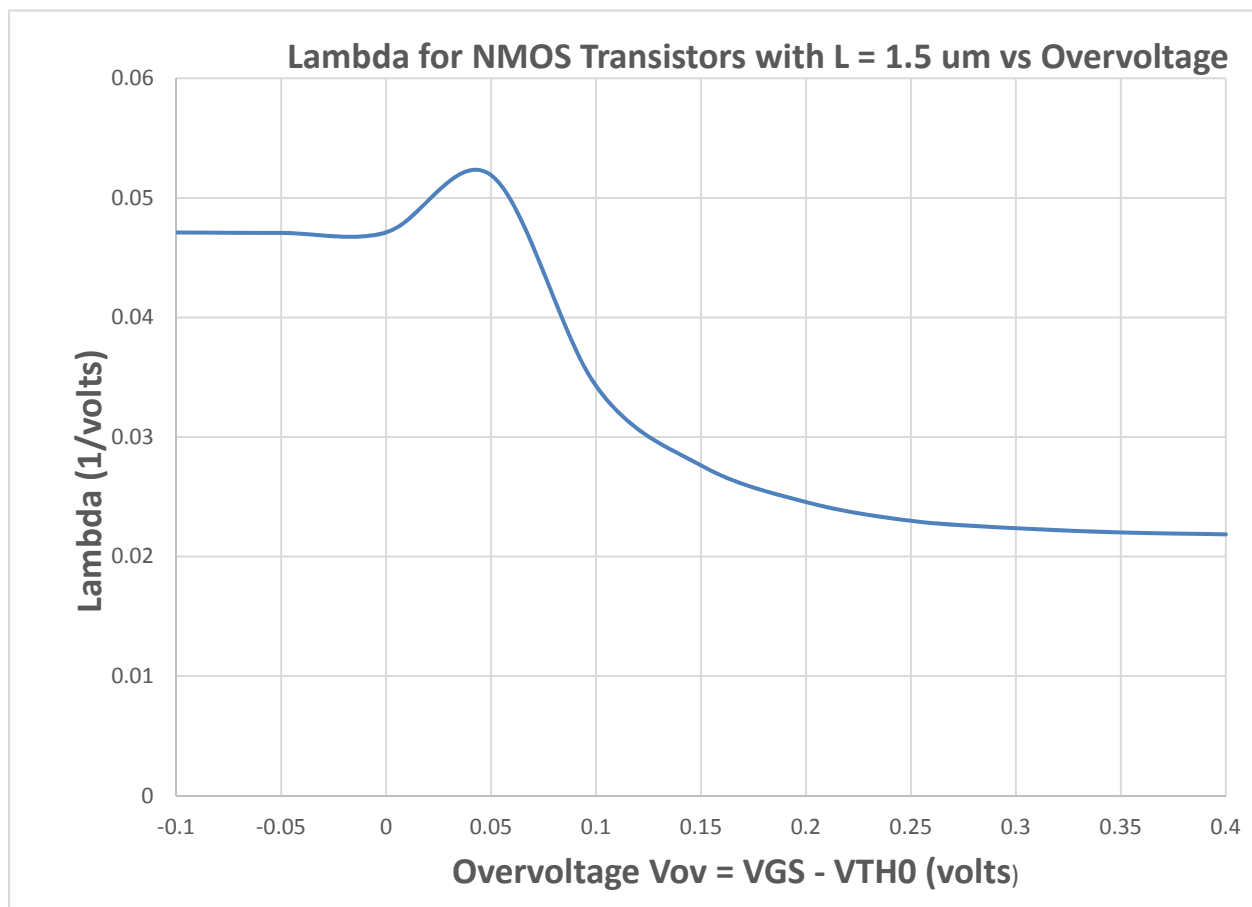
Appendix II: Common Mode Gain and CMRR

A common mode input voltage induces a change in the drain currents of the input differential transistor pair that is the same in both transistors. The value of that current depends primarily on the output resistance of the current source that biases the source terminals of the differential pair. If the resistance of the current source is r_{Ocurr_source} then the drain current is approximately

$$i_{d\_cm} = \frac{v_{cm}}{2r_{Ocurr\_source}} \ .$$

The current mirror that converts the two drain currents into a single current output will take the difference of the two currents, substantially lowering the net common mode current into the output node of the differential amplifier. However the current mirror does not take an exact difference. For a simple mirror with no cascoding, the net difference is the input current divided by

$$\left(1 + g_m r_O\right)$$

where the transconductance and output resistance are those of the input mirror transistor. (*You should be able to derive this formula from the small signal model of the mirror circuit!*). The net common mode output current of the stage is $i_{cm} = \dfrac{v_{cm}}{2r_{Ocurr\_source}\left(1 + g_m r_O\right)}$.

The net current for a differential input is $i_{\Delta} = g_{m\_diff} v_{\Delta}$ where g_{m_diff} is the transconductance of one of the transistors in the differential pair. The common mode rejection ratio is the ratio of the differential current to the common mode current for excitation by the same value of input voltage.

$$CMRR = \frac{i_{\Delta}}{i_{cm}} = 2 g_{m\_diff} r_{Ocurr\_source}\left(1 + g_m r_O\right)$$

Calculate the common mode voltage gain by dividing the differential gain by the CMRR.

Appendix III: Summary of Formulas for MOSFET Properties

All of the MOSFETs in your circuit are likely to be in saturation, the normal active region. Many of the properties of the devices at low frequency are derived from the basic ID-VGS relationship. This table summarizes these relations.

Property	Formula
ID vs VGS and VDS in saturation	$I_D = \dfrac{W}{L} K \left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS}\right)$

Transconductance	$g_m = \dfrac{2I_D}{V_{ov}}$ for $V_{ov} \geq .3$ V_D; for $V_{OV} < 0.3$ $g_m \propto I_D$ see Appendix I for the proportionality factor
Output resistance (Channel length modulation)	$r_O = \dfrac{(1 + \lambda V_{DS})}{\lambda I_D}$
Gain of common source stage with no source degeneration	$g_m r_{output\_node}$
Gain of differential amplifier with current mirror	$g_m \left(r_{Odiff\_transistor} \parallel r_{Omirror} \right)$ where g_m is the transconductance of one of the differential pair transistors
Slew rate of two stage opamp	$S.R. \equiv \left\| \dfrac{dv_{OUT}}{dt} \right\|_{MAX} = \dfrac{I_{BIAS}}{C_{COMP}}$ where I_{BIAS} is the total current biasing the differential pair and C_{COMP} is the capacitor from output to input of stage two that exploits the Miller effect to give the dominant pole .
Common mode rejection ratio	$CMRR = 2 g_{m\_diff} \, r_{O1stStageBiasCurrentSource} \left(1 + g_m r_{Omirror\_transistor} \right)$
Dominant pole position	$f_d = \dfrac{1}{2\pi C_{COMP} \left(1 + A_{2ndStage} \right) r_{O1stStage}}$ See formula for Gain of differential stage for the output resistance of that stage.
Measuring Phase Margin	To measure PM plot frequency response magnitude and phase; find the frequency at which the gain is 1X (0 dB or unity gain). This is the unity gain frequency, f_u. Subtract the phase at that frequency from 180. Should be 60 degrees or more when you are done.