Draft Manual as of 4/18/2016

This manual is complete through lab 9. Lab 9 itself has not been tested or especially well proofread. Remember you are free to choose from labs 6 to 9 to make up a total of 6 labs to pass the course.

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ENGN1620—Analysis and Design of Electronic Circuits

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LAB MANUAL

Wm. R. Patterson III
B.H. 449 ext. 3-1449
William_Patterson@brown.edu

With contributions from and thanks to Prof. Jacob K Rosenstein

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General Information:

Admonition: We have to ask that you be careful about neatness in the lab. The lab can be a difficult experience for everyone if you don't put things away when you are done. There are twenty people enrolled in this course and similar numbers taking ENGN1640 which shares our lab space. That many people can make quite a mess quickly. We spent a lot of time over break cleaning up the lab and would like to see it remain in reasonable shape.

We buy enough parts, but we cannot accommodate your habits of dropping used materials wherever you happen to be when finished. You are not done with a lab until your breadboard is disassembled and shared parts are returned to their boxes. This is especially true of capacitors and inductors as their cost is quite high. It is frustrating to the TAs and me when we find whole boxes full of unsorted resistors, diodes, etc. as the course goes along. Also, wire has gotten quite expensive - it is now about $ 0.10 per foot for plain hookup wire. You use a lot of it! To lower that cost, we ask that you put your used wires in one of a couple of "Give-a-Wire-Take-a-Wire" boxes in the back of the lab. Do not cut more wire off the spool for a new lab unless you cannot find appropriate wires in those same boxes.

Introduction: There are nine labs set in this manual, two measurement labs and seven labs for which you design, build, and test a circuit to meet fixed performance criteria. You must complete and document six labs in order to get credit for the course. (Although there are nine exercises set, I will base grades on only six reports. You will not receive extra credit for extra reports.) You must do Lab 2. You are free to choose five more from the remaining 8 full labs. **THERE WILL BE NO EXCEPTIONS TO THIS POLICY**. In addition to this manual, you will receive a protoboard (with a serial number) on which to assemble your circuits, a pair of wire strippers, and a small packet of semiconductors. Please return the breadboard and strippers at the end of the semester. Passive components and some semiconductors must be shared communally. We have labeled, multi-compartment cabinets and boxes for storage of these materials. Your cooperation in **returning parts to their proper place is absolutely necessary** for the success of the lab. Also, please do not keep components longer than necessary to do your lab. Capacitors in particular are bulky and expensive so that we do not keep enough available for everyone to have complete sets simultaneously.

The labs are done in the Hewlett Electronics Laboratory, room 196 of the Giancarlo addition, aka the Fishbowl. The lab will be shared with both Engineering 1640 and perhaps Engineering 1580 this semester. Equipment and parts for this course will be on the benches farthest from the doors. This room is open almost all the time during the semester. There does not have to be a lab TA present for you to work, but such assistance will be available roughly 18 hours per week. (The hours will be announced on the class web site - http://www.brown.edu/Departments/Engineering/Courses/En162/home.html.) You hand in lab reports in a box in the lab that is marked "Engineering1620/1630 Lab Reports," and a TA will grade them under written guidelines from me.

Collaboration: Design concepts and measurement techniques may be discussed freely. However, each person must build and test the circuits on his or her own protoboard. ALL lab work and all written reports must be done individually. All data reported must be your own measurements – **copying data and representing it as yours is a cardinal sin among scientists of all types**. **I do not like being harsh, but I will not hesitate to refer cases of data copying to the Academic Code Committee however trivial the data or infraction seems to you. Data copying includes the process of one person measuring and the other recording a common set of data. In the world of science and engineering, supposedly independent data sets are relied on for confirmation of results. I want you to develop that mindset early.**

Concise, complete, polished lab reports will be rewarded with higher marks. **A TA must witness the measurements you present to prove that you have met the lab specifications with your own wiring.** He or she will record the fact that you did the lab on a spreadsheet and will give you a magic ID number to print on your data plots report. (If there is any question about the data, we can reverse that number to recover your name and lab number.) While you can design, build and test your circuits without a TA if you wish, the final run of measurements does require a TA to witness this recording process.

Lab reports must be typeset in a word-processing program. The format for the design lab write-ups would be appropriate for an in-house report prior to a design review at an electronics design company:

I. Introduction: Discuss briefly the major goals of the lab.
II. Schematic: Show component values and, where appropriate, the measured quiescent node voltages.
III. Tables: Compare design versus measured values of all important quantities
IV. Design: Description of the design procedure and design equations. **Prove** that the worst-case conditions are met by design. You do not have to show the algebra by which you may have fit the equations, but you do have to show that a suitable equation set is satisfied.
V. Questions: Answer the specific questions set in the handout.

For the characterization experiments, follow the directions in the lab handout.

For each experiment there is a deadline by which your report must be turned in. These will be announced in class and posted on the class web site. Reports that are turned in after the deadline will have penalties assessed against them. Be forewarned -- your classmates **also** like to wait until the last minute to do their work, so start early and try to get a bit ahead of the deadlines -- overcrowding in the lab will not be accepted as an excuse for turning in lab reports late. Also remember the deadlines will be set as late as practical. The labs are intended to teach, and you will have the benefit of that knowledge earlier if you do them earlier. This is particularly true of doing some of the earlier labs, particularly through labs 4 or 5, before the mid-semester exam, which comes rather late in the semester.

Several of the lab exercises, particularly Labs 4, 5 and 7 require measurements of the gain and phase shift of amplifiers as functions of frequency. There are computer driven systems for automatic measurements of these quantities. One system even has an Excel spreadsheet output

that you can put data into and it will make the actual Bode plot. You can take that data home either by emailing the file or by putting it into your Engineering account. **Please do NOT leave your results on the computer "Desktop."** The TA still has to witness the measurement and issue the ID number, and in doing so will check your circuit board serial number. The parameter analyzer supplies a similar set of files with data for Lab 2. (I wrote the Lab 2 software and it is a little buggy – partly my fault and partly because the analyzer is not easy to control. Please be patient.) Labs 1 and 6 require making plots and Fourier transform calculations from a digital oscilloscope. We have a several Agilent oscilloscopes that allow you to transfer screen data to files on a flash drive. Like the computerized tests, this data has to receive TA approval in the form of a magic number. All files are subject to the same check off system and properly formatted printouts of them are a required part of your reports.

Components: Of the various passive components in the lab, the capacitors require special comment. There are three principal types: electrolytic capacitors, film capacitors and ceramic disk capacitors. Electrolytic capacitors are made with aluminum or tantalum plates by electrolytically forming an insulating oxide on one plate. (If you don't know what the term "electrolytically" means, then please either ask me or look it up.) Since that oxide is very thin, a large capacitance per unit volume is possible. These are the only types of capacitor available for you that have values over a microfarad. Unfortunately, the chemical reaction that forms the oxide is reversible if the potential across the capacitor is of opposite polarity to the forming voltage for an appreciable length of time. The capacitors are marked for the terminal that was positive during manufacture. In use, one must be careful that any applied DC voltage is in the same direction. Failure to do so will ruin the capacitor and make the circuit malfunction. Aluminum electrolytics are often unsuitable for some high frequency applications because of high series inductance. Another feature of electrolytic capacitors based on aluminum is that the tolerance on their capacitance is very poor, typically -30% to +80% of nominal value.

Disk ceramic capacitors use simple blocks of a ceramic with a very high dielectric constant as their insulator. (Some ceramics have very high relative dielectric constants, as high as 800 as against typical plastics with value of 2 to 4.) All are nearly ideal capacitors to quite high frequency (10's of Megahertz). However, inexpensive types usually have poor tolerance (-20% to +50%) and very high temperature sensitivity. They are used primarily where exact values of capacitance are not critical. A common application for these is power supply bypass. There are several large reels of bypass caps in the lab – you should never lack for enough.

Film capacitors have generally good performance with tolerances no worse than +/-10%. Their primary disadvantage is that they are usually physically large for a given value of capacitance. You are likely to find capacitor tolerance a significant issue only for lab 7.

Resistors: Resistors have three principal ratings: resistance in ohms, tolerance in percent, and power dissipation in watts. Most of the resistors we have in the lab can dissipate ¼ watt and have tolerances of ± 5 %. They are manufactured only with certain standard resistance values that are separated by about 10 %. We have most of these values and it usually does not make sense to put resistors in series to come closer to calculated values. The attempt is illusory because the tolerance variation is bigger than the adjustment you would be trying to make. Resistance values are coded on the resistors with color bands. The first two bands give two significant digits of the value, the third band is a multiplier expressed as a power of 10, and the

fourth band is the tolerance. The table below shows the color code. For example, red-red-orange-gold is 22 Kohms ± 5 %. Sometimes ¼ watt is not enough for a circuit application and then a physically larger resistor is required. We have some 2-watt resistors in a relatively narrow range of values anticipating a need for such a device in Lab 5.

Color	Significant Digit Value (Band 1 or 2)	Multiplier
Black	0	1
Brown	1	10
Red	2	100
Orange	3	1000
Yellow	4	10000
Green	5	100000
Blue	6	1000000
Violet	7	
Gray	8	
White	9	

Resistor Color Codes

EXPERIMENT NO. 1 - Oscilloscope Use

The principal purpose of the lab is to make you familiar with the use of a digital oscilloscope and to demonstrate some of the subtle problems involved in their use. There are two main complications:

1. Oscilloscopes can affect the circuit you are measuring so that what you see is different from how the circuit works when you are not looking at it. This is not Heisenberg uncertainty but the effect of ***the impedance of the oscilloscope probe*** itself. Such effects can be serious and while they can be minimized with the proper cables and probes, they cannot be eliminated.
2. Digital sampling introduces complications in interpreting data, particularly in the frequency domain. Digital scopes sample the input signal and convert it to discrete measurements that are stored in RAM memory, allowing one to read that data out electronic form. The scope can also do mathematical operations including Fourier transforms on its stored data. The sampling rate and voltage resolution must be adequate to represent the signal you are measuring.

Usually these effects are relatively small for low-frequency circuits. However in high frequency circuits used for wireless communication or for fiber optic communication the effects are inescapable and probe design is a serious challenge. This lab is set up so that probe effects are readily noticeable at a few tens of kilohertz. You should pay close attention to the details of how you have connected all of the oscilloscope probes, and how the instrument itself is programmed. (Do not just use autoscale!)

We have put two "black boxes" in the lab with resistive networks connecting a BNC input to a bare wire output. You will connect these boxes between a function generator and the scope to make several measurements of periodic waveforms using two types of oscilloscope probes. One is a "10X" attenuator probe that reduces the signal amplitude by a factor of 10 before it reaches the scope. The other probe, called a 1X probe, passes the signal without attenuation. The difference is not only the attenuation but also the amount of capacitance that the circuit "sees" when you connect the probe. (A circuit "sees" an impedance, capacitive or not, by sensing the amount of current a source must supply to produce a certain voltage across the input to the probe. The term is casual jargon reflecting a sense of what happens to an output as you connect or disconnect a load.) You will find that the tradeoff for the reduced transmission of the 10X probe is that its lower input capacitance affects the circuit less. I have tried to design the experiment to lead you to think quantitatively about why this is the case.

In the first part of the experiment you will do several basic measurement on a square wave signal for which the frequency spectrum is well-known and the time domain picture is simple and obvious. Finally, I have programmed two of our Agilent arbitrary-waveform generators to produce a rather odd-looking signal. You will take screen shots to see qualitatively what happens to signals that are more difficult to interpret. You will also try out the use of external synchronization with this signal.

Measurements:

1. Apply 5V to the input of the black box. Determine its Thevenin equivalent circuit by measuring its output voltage and output resistance. One way to do this is by measuring its output voltage with & without a resistor load. Think carefully about what resistor value to use and what instrumentation setup to use to do this measurement. If you wish, you may try more than one arrangement or technique of your choice.

2. Configure one of the waveform generators on the back bench to produce a 30-kHz $2V_{pp}$ square wave. Connect a BNC cable directly to an oscilloscope, adjust the display so that the signal takes up more than half of the vertical resolution and set the timescale so that you see 20-30 periods of the signal. Set the scope to trigger on the rising edge of this signal. **Does the scope voltage measurement agree with the function generator scale?**

3. Set up a Fourier transform of the waveform using the scope's "Math" menu. Try a span of 500 kHz and a center frequency of 250 kHz. What are the frequencies of the peaks in the spectrum, and how do they relate to the square wave frequency?

   Experiment with the scope settings to see how the spectrum changes with different parameter choices. Record the sampling rate that is indicated on the scope display and compute how many samples are taken during the displayed time interval of the waveform. Watch what happens to the spectrum display and the sample rate as the time base control is changed up or down by one step. Also compare the spectra obtained with a "Hanning" window versus a "flat-top" or rectangular window. (The selection of a "window" is one of the parameters in the Fourier transform setup menu. These windows are specific ways of weighting the samples toward the ends of the time interval in order to minimize the effects of having a finite sample interval.)

   In saving data for this part of the lab, set the FFT for a rectangular ("flat-top") window and a sample/second rate that gives good resolution of the peaks. Set the vertical channel sensitivity so that the waveform occupies most of the screen without any clipping. Note these settings for reference later. Measure the amplitudes of the first 5 harmonics in the Fourier transform **relative to the fundamental in dB** for the waveforms from both probes. Save your data to a USB drive.

   (You are about to save time traces & frequency spectra for several similar datasets. Each captured waveform will be stored in its own file, so pick the file names carefully to distinguish the measurement conditions for each trace. Notice that the waveform changes shape as you change probes! This is the effect on the actual signal of connecting it to the scope and it is non-negligible. Be sure to record the horizontal time base and the vertical sensitivity, as you will need that data for your calculations.)

4. Now connect the waveform generator to the "black box", and measure the output with a 1X oscilloscope probe. Zoom in to see just two or three cycles on the screen and save the raw trace data. Do you notice any differences in the shape of the waveform? A change of shape in a signal implies a change in its frequency spectrum. Zoom out so that you have 20-30 cycles on the screen and calculate the new Fourier spectrum. Save

both your time and frequency domain data to the USB drive. Be sure to record the horizontal time base, the vertical sensitivity, and the screen size in cm for both axes, as you will need that data for your calculations.

5. Measure the output again with a 10X oscilloscope probe. Zoom in to see just two or three cycles on the screen and save the raw trace data. Calculate the Fourier spectrum. Save your data to the USB drive.

6. Make the measurement one final time with both probes connected to the generator. (Obviously, you still only need one trace for this last measurement as both probes see the same signal.)

   (You should now have 4 sets of similar time and frequency data: (1) from a BNC cable direct from the generator to oscilloscope, (2) through the black box with a 1X probe, (3) through the black box with a 10X probe, and (4) through the black box with both 1X and 10X probes connected. Be sure to name the files so you can associate the measurement configuration with the data.)

7. Now reset the generator to output the preprogrammed arbitrary waveform 'arb1'. This is the signal that I set up to mimic a more complex waveform more typical of an information-bearing signal. Set the output to 2 V pp.

8. There is a synchronization or "synch" pulse output available from a BNC connector on the waveform generator. Using a coaxial cable, connect that signal to one channel of the scope and set the scope for a stable measurement with DC coupling at the input. (You want to measure the actual voltage relative to ground, not just the variation with time.) With the scope cursor controls and digital readout, determine the maximum and minimum voltages (be careful about offset), the period, and the pulse width at the 1.5-volt level. (The 1.5-volt reference level is the standard voltage for measuring time delays for 3.3-volt CMOS logic and the older 5-volt TTL logic. Do not confuse the reference voltage level for time measurements with the pulse amplitude.)

9. Now connect the synch signal to the "Ext, Trigger" input of the scope's time base and set the scope to trigger on the ***falling edge*** of this signal, *i.e.*, use external synch mode with negative slope and 1.5 volts as the trigger level. (The external trigger input is on the back top of the scopes next to the USB output.)

10. Connect the generator 'arb1' waveform to a black box and measure the output with the 10X probe. Set the vertical sensitivity and horizontal time base to display between one and two periods of the signal with as large a height as can be set without clipping. Repeat the time domain measurements of steps 4 to 6. Do not bother with doing a Fourier transform on this signal.

11. Measure the length of the probe cables with a ruler. (You will use this to find their capacitance per foot.) Record the values of resistance and capacitance marked on both the 10X and 1X probes and on the input of the oscilloscope. These values are the

equivalent impedance seen at the probe or scope input expressed as a parallel combination of a resistor and capacitor. The value marked on the probes is for the probe and scope together. These equivalent circuits do not necessarily correspond to any actual physical components.

12. Remember to get the magic ID number for your name and Lab 1 from a TA by demonstrating how you have taken data.

Guidelines, Issues, and Questions for Write-Ups:

Please begin your write-up with a short introduction that talks of the features of measurements and spectra that seemed important to you from this lab. Then use the following list as guidance for the rest of the report. (Doing so will make it easier to write and easier for us to grade.)

1. Show the measurements and calculation by which you found the output resistance of the source.

2. Analyze the operation of the 10X probe. The equivalent circuit of the 10X probe is shown below. The components R_1 and C_1 are actual physical elements in the probe body. The capacitor C_{CABLE} represents the cable capacitance. (At 30 KHz the cable is essentially a lumped shunt capacitor.) Let C_T be the total capacitance of cable and scope given by $C_T = C_{CABLE} + C_{SCOPE}$. Please do the following for this circuit:

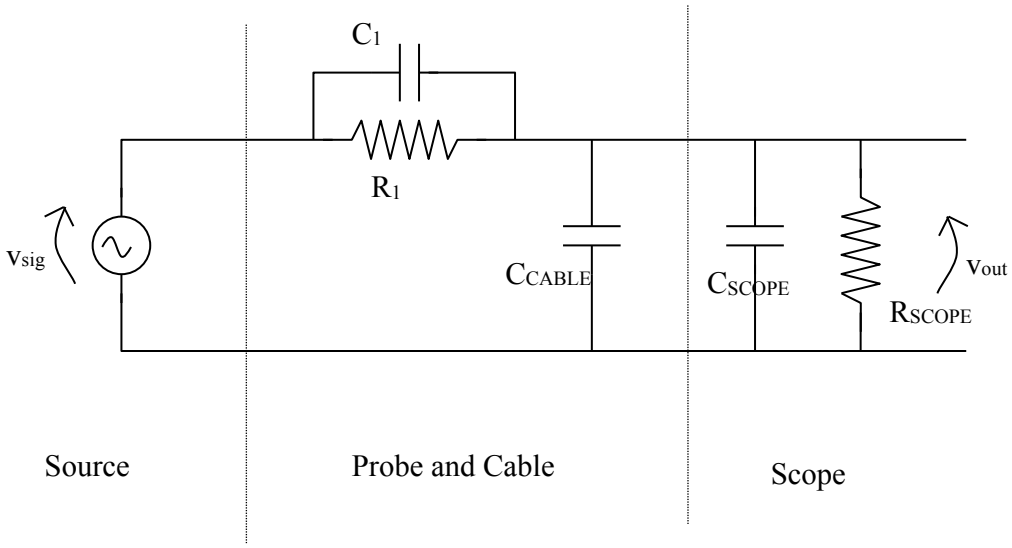
    - Derive the transfer function of this system and show that it is independent of frequency if $C_T/C_1 = R_1/R_{SCOPE}$.

    - The real probe is designed and adjusted to meet this constraint. (There is a screwdriver adjustment of C_{CABLE} in the form of an adjustable lumped capacitor in parallel with the cable, and we try to keep that adjusted to meet this criterion.) Prove that this condition also makes the input impedance equivalent to a single resistor and capacitor in parallel. The probe is marked with **the values of these equivalent components** rather than any of the values of the actual components: R_1, C_1, R_{SCOPE}, C_{SCOPE} or C_{CABLE}. The scope itself is marked with its input resistance (1 megohm) and capacitance (C_{SCOPE}). (You can find C_{SCOPE} for your calculations by reading the front of the instrument.)

    - Find the values of the real components of the probe and scope system (R_1, C_1, C_{SCOPE} and C_{CABLE}) from your theory and measurements.

3. Typical coaxial cable has about 30 pf of capacitance per foot. How does that compare to your estimate of the capacitances per foot of the two probe cables? What is the total capacitance of the 1X probe, including both its cable and the scope connection?

4. Using EXCEL, MATLAB or a similar graphing utility, plot the data you took of the single cycle traces. Do this separately for the square wave and the complex waveform data sets. Overlay the data taken with the 10X probe, the 1X probe, and both probes on the same graph. Distinguish the traces by color, line type or small vertical offset. Try to design the presentation so that the change in signal features is clear as the load capacitance increases. Comment qualitatively as to why the curves change.



Equivalent Circuit for a 10X Probe Connected to an Oscilloscope

5. Look at your raw data and determine what the minimum voltage step is that the scope stored, that is, what is the vertical resolution of the scope on this scale. How many such steps are in your trace? How many fill the screen? The number of such steps is always an integer power of two, the number of digital bits used to represent the data. How many bits per sample does this scope store?

6. Show that output impedance of the generator, R_0, in conjunction with the scope probe forms a low pass filter and compute the cutoff frequencies for the three cases you just plotted. How do those frequencies compare to the fundamental frequency of the waveform?

7. From the measurements you took of the amplitudes of the first five harmonics in sections 4 and 5 of the measurements, what is the lowest harmonic frequency at which the 1X measurements were attenuated by 3 DB (a factor of $1/\sqrt{2}$) or more than the 10X ones? Is this consistent with the calculations of the cutoff frequencies of your probe setups?

8. Prepare frequency spectra of the data from the 10X and 1X probes. You can do this directly on the oscilloscope, within EXCEL using the Fourier Analysis tool that is part of the Data Analysis add-in, or you can import the data into MATLAB. Plot the measured

Fourier spectra of the data from the 10X and 1X probes. Plot using an x-axis with the real linear frequency scaling, not just Fourier coefficient numbers.

9. Because the waveform is known to be perfectly periodic, the proper spectrum is a Fourier series. In general the exact frequencies will not match any components of the Fourier transform exactly. Overlay the 10X probe spectrum along with the ideal frequency spectrum of a square wave. Normalize the ideal spectrum to have the same fundamental amplitude as your data. Where you find harmonic data in the spectrum from your scope, are the data single points or small clusters of components? What is the step size in frequency from one of your Fourier components to the next? Comment on the accuracy of your FFT calculation with respect to both harmonic frequencies and amplitudes. What normalization factor did you have to use?

10. Tabulate your synch pulse measurements. You were told to use external synchronization. What is the advantage of doing so? (Think, for example, of measuring signals in a communication system where data signals change constantly but clock pulses or signals for start and end of data are available just as the synch output of the generator is.) Where on the waveform is the edge of the synchronization pulse? **Show this position by a mark on the waveform plot.**

11. The arbitrary waveform has a narrow positive going pulse superposed on an irregular baseline signal. What is the width of that pulse? What are the time constants of the circuit with the 10X and 1X probes? Is the change in shape of the waveform as measured with the different probes consistent with these two constants?

12. As a final test of your powers of observation, here is a challenge question. There is a small difference between features on the outside of the 10X and 1X probes besides the labels. On our new scopes with the USB ports, you have to set the probe type to have the vertical scale be correct. On our older scopes with the CRT screens, the scope automatically compensates its gain for whether you use a 10X or a 1X probe. (It does not work for any other probe range – there are, for example, 100X probes for high voltage that do not display correctly.) How did those scopes know what probe you are using?

EXPERIMENT NO. 2 - Characterization of a Diode and a Transistor

The object of this experiment is to measure of some of the device characteristics discussed in class for a typical diode and for a typical bipolar transistor. The diode is a 1N4003 diode designed for rectifier service with a nominal breakdown rating of 200 volts and an average forward current rating of 750 ma. The bipolar transistor is the 2N3904 a low power transistor with a V_{CB0} rating of 30 volts, a maximum collector current rating of 150 ma and a power dissipation rating of 0.3 watt maximum. Full data sheets on these devices are on the class website and I have put extracts in an Appendix to this manual.

Current and voltage measurements are done with a Hewlett Packard parameter analyzer for low voltages and currents. We don't have a truly functional instrument for higher voltages or currents so we will limit the diode measurement range. Data from the analyzer can be captured on the PC that controls it and you can put that information into one of the folders on your engineering computing facility account. The software for the analyzer probably still has some bugs but it gets more stable each year. There is a description of how the analyzer works and how to set it up on the class web site under the heading of *Course Materials/Parameter Analyzer Notes.* As much as possible we will try to let you do the measurements yourself. The TAs are willing and able to give you further information on its operation. Remember you have to show a TA that you can do the measurements and ask for a "magic number" to add to your report as a sign you did the work yourself.

1. Measure the capacitance of a reverse biased diode (1N4003) using our Boonton™ capacitance meter. This instrument applies a small 1 MHz signal to one side of the unit under test and senses the current in other lead, while that lead is effectively grounded. Readout is by a panel meter graduated directly in picofarads. Be sure the meter is zeroed before putting in your diode and make use of the mirror scale to minimize parallax. Two terminals on the back of the meter, labeled "bias," allow one to apply a DC voltage to the unit under test while the capacitance is being measured. There is a 120 VDC power supply connected to the meter. A shock from it can be painful, so please be careful. Both you and the meter need protection from this voltage and I have an appropriate network for that purpose connected to the back of the meter already. Please do not disturb it.

There is some loss of potential in the protection network and the power supply meter is not really sufficiently accurate at very low voltages. Therefore, use a separate digital voltmeter to measure the voltage being supplied to the Boonton and to determine the polarity of the bias on the diode. (Remember you are interested in the reverse bias capacitance.) To avoid problems with including the capacitance of the meter with that of the diode, the DVM is connected to the bias terminals on the back of the meter. I try to leave a meter already connected for this purpose and would appreciate your leaving it there. You can use a second meter across the diode terminals to determine polarity before connecting the diode. Measure and plot the reverse bias capacitance of the 1N4003 (or equivalent) diode from zero to 100 volts reverse with enough points to determine whether it approximately follows the expected curve for an abrupt junction:

$$C = C_0 + \frac{C_{J0}}{\sqrt{1 + V_R / V_{BI}}}$$

where C_O is a fixed capacitance due to the case of the diode, C_{J0} is the junction capacitance at zero bias, V_R is the reverse diode voltage, and V_{BI} is the junction built-in potential. Because this equation varies more rapidly near zero volts, you will have to take points more closely spaced near zero than you do for higher voltages. You may even want to take a point or two for forward bias up to 0.1 volts (negative reverse voltage). V_{BI} must be less than the bandgap potential (1.18 volts for silicon) and is likely to be more than .7 volts. Use Excel or a math package to find the best estimates for C_0, C_{J0}, and V_{BI} subject to that constraint. Then overlay your data with a theoretical plot based on these estimates. I suggest not allowing the curve fit to be completely unconstrained – forcing a fit for one or two carefully measured points at zero and 100 volts and adjusting parameters to find the best fit for the remaining points seems to work well.

2. Using the semiconductor parameter analyzer, measure the forward current of the 1N4003 as a function of bias zero volts until the current reaches 100 ma. Does this curve fit a relation of the form:

$$I_D \propto I_S e^{qV/nkT}$$

where *n* is a constant, often called the ideality factor? What value of *n* fits best? Over what range of V and I_D is this fit to within 20 %? (Take this data home as a file for later processing.)

3. Run a SPICE simulation of the 1N4003 for the same conditions. Compare the measured and simulated data.

4. Again using the semiconductor parameter analyzer, make a Gummel plot for your 2N3904 transistor with V_{CE} = 3 volts, keeping I_C under 100 ma. Begin with V_{BE} at zero volts so that any heating effects will affect only the high current measurements. (A Gummel plot has overlaid curves of I_C and I_B as functions of V_{BE} at a fixed, usually low value of V_{CE}. The curves are drawn on a log-linear scale so that a wide range of current can be shown. See the example plot at the end of this write-up.) There is an electronic thermometer on the shelf over the analyzer. Record the temperature at the time you make your measurements. Over what range and with what value of n is I_C proportional to exp(qV/nkT)? Does I_B behave the same way? Is the current gain independent of I_C? From the same data, draw h_{FE} versus I_C.

5. Measure I_C as a function of V_{CE} from 0 to 10 volts using I_B as a parameter, taking enough data to be able to draw one of the sets of curves we use in class to show amplifier operation. Cover the range of I_C up to 10ma with 5 – 10 base current curves. Plot this in your report and derive from it the Early voltage at $I_C \approx 5$ ma and V_{CESAT} at the same current. In the software running the analyzer, pick the option for "matrix" format of output data to make plotting easier.

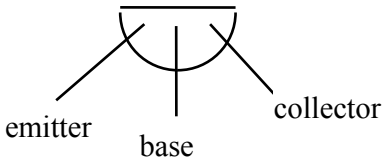
6. In principle and in practice the emitter and collector of a bipolar transistor can be interchanged, and the device will still show appreciable common emitter current gain. In this configuration, the old collector is, of course, the new emitter. This is called "reverse operation" of the transistor, and the current gain is called h_{RE} or β_R. Measure this quantity for I_C = 1 ma and V_{CE} = 2 volts. How does this compare to the forward current gain? Why are the relative magnitudes of h_{FE} and h_{RE} what they are?

7. Do a SPICE simulation of the 2N3904 for the conditions you used for the Gummel plot in forward active operation. Compare that simulation to your measured data.

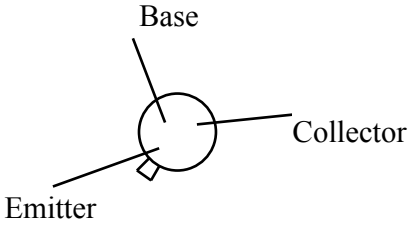
NOTES:

1. Please try to avoid damaging components by limiting reverse, leakage current to 10 μamp. None of these junctions are designed with sufficient thermal dissipation to serve as a zener diode.

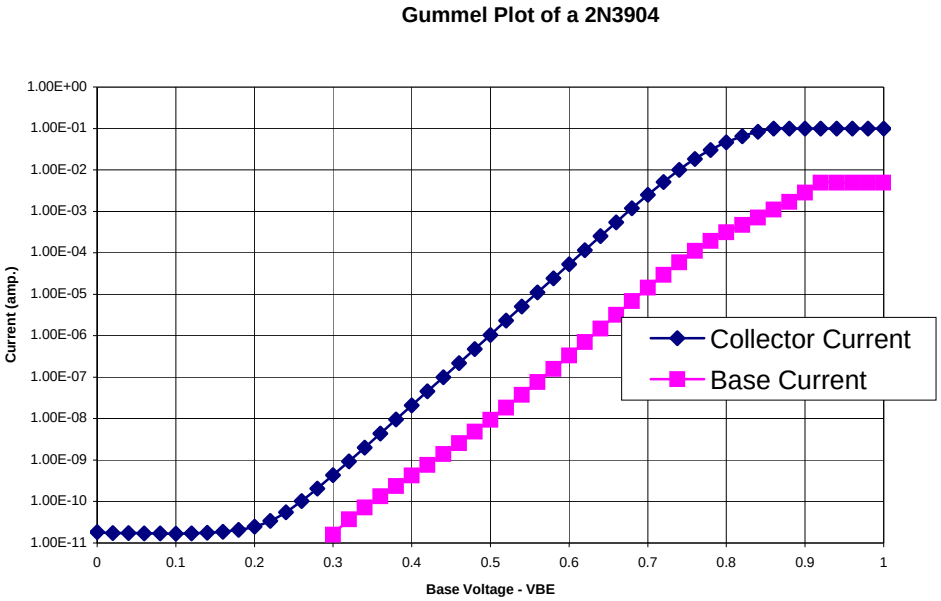
2. Here are the package diagrams for the transistors (bottom view) and the MOSFET arrays (top view).



2N3904 - bottom view



TO-18 2N222A - bottom



Example of a Gummel Plot

EXPERIMENT NO. 3 - Half a Cheap Stereo

This experiment introduces the idea of biasing a circuit for linear amplification. It is intended primarily to introduce the capabilities of MOSFETs (Field Effect Transistors), to remind you of the rules for Q point selection, and to give you a chance to think about simple RC circuits. Build the circuit shown below, designing the required RC network and measuring its performance. The circuit uses a transformer to drive a low-resistance speaker with an amplifier made from a single MOSFET. Using the primary taps marked 2.5 and 5 watts and the C and 8 Ω secondary connections to the speaker will result in a transformer primary with a primary magnetizing inductance of 0.5 H, a turns ratio 4.6:1 from primary to secondary, and a primary wire resistance of 30 ohms. (By comparison, the secondary resistance is negligible.) The speaker acts roughly as an 8 Ω resistance.

There are also a number of power MOSFET field effect transistors in the lab that are already mounted on heat sinks with extension wires on their leads. These wires let you plug the transistor into the rest of the circuit on your protoboard. (The exact type of transistor varies with what is available. The IRF610PbF is typical of what we use and its pinout and characteristics are given below.) Unmounted transistors are intended only as backups. (If one of the transistors on a heat sink is damaged, please give it to me to mount a new one.) The gate bias voltage in operation is usually about 3.5 V but may be up or down by several tenths of a volt. You may have to adjust your circuit to get the correct (optimum!) quiescent current.

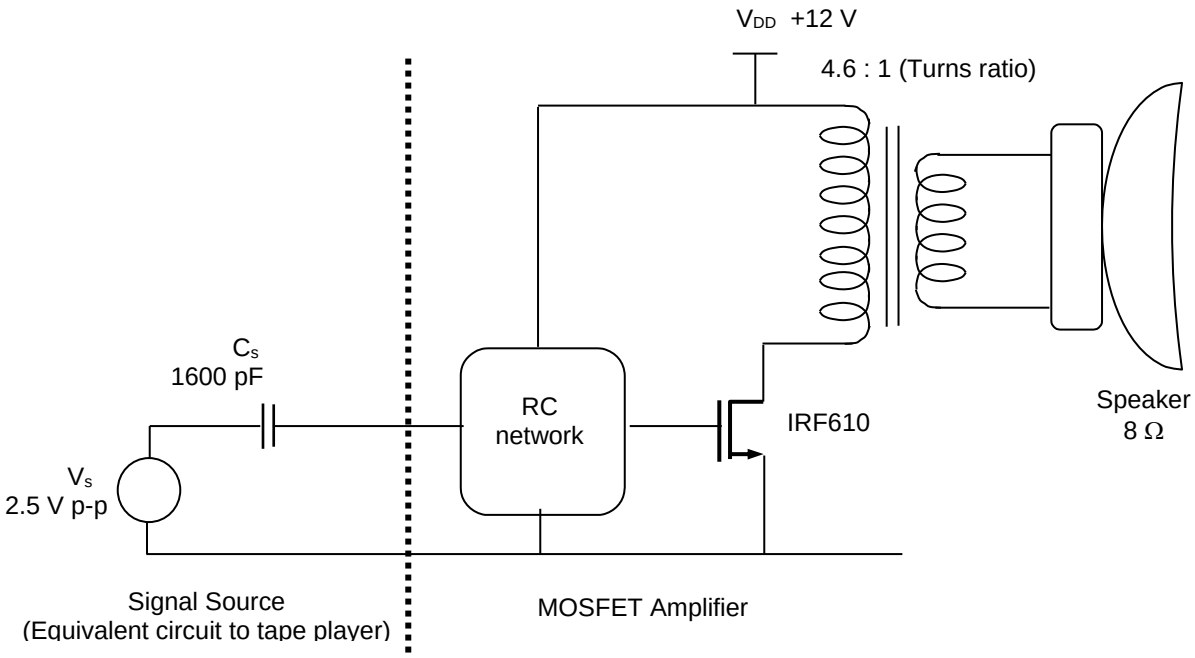
There are two FM/AM radios with cassette tape players in the lab that we have modified for use as a signal sources by adding an output cable and limiting impedance. They are battery operated so be sure to turn them off when done by putting them in tape operation and pressing the STOP button. The output is equivalent to a 2.5 volts peak-to-peak signal with a source impedance of a 1600 pf capacitor. The figure below shows the connection of the MOSFET to the coupling transformer and speaker. Designing an RC network to connect the tape player to the MOSFET and to provide MOSFET bias is part of your job. It should take either three resistors or one capacitor and two resistors. (I rather like the latter circuit for aesthetic reasons. At least, you should know what the two choices are.) The MOSFET gate can be considered an open circuit for this design. The signal voltage from the tape player at full volume is somewhat bigger than the MOSFET can handle without distortion. To fix this problem, your RC network should attenuate the signal by a ratio of 5:1. In your write-up, you are expected to **show this attenuation is realized by design**. The low frequency cutoff associated with the network including the effect of the capacitor in the signal source (1600 pf equivalent source impedance) has to be placed at or somewhat below 50 Hz.

Select the bias from the network to make the quiescent current optimal for maximum possible voltage output. For proper transistor operation, i_D should not go below 10% of the quiescent bias current, and v_{DS} should not go below V_{DSSAT}. Derive the quiescent current $I_{D\text{-}OPT}$ which allows the maximum AC power to be delivered to the speaker. (Hint: Note that $i_D = I_{D\text{-}OPT} + \Delta I_D$; $P_{OUT} = |\Delta I_D \times \Delta V_D|$. ΔI_D and ΔV_D are related through the load impedance.) The transformer specifications are adequate to fill in the parameters of the optimal quiescent current formula. (While I know that we have not talked in class about

MOSFETs, I think one of the points of this experiment is that the device physics is somewhat irrelevant. Amplifiers using three terminal devices operate the same way whether the device is a vacuum tube or one or another transistor type. The differences are largely a matter of scale.) Determining the gate bias voltage that corresponds to the optimum drain current may be done empirically. (The choice of the value itself is theoretical **NOT** empirical.) You may use the curve tracer or parameter analyzer to determine an appropriate value of gate voltage V_{GS} or you may use trial and error to set the right I_D. This is the one lab that allows a cut-and-try approach of adjusting one resistor value while measuring the quiescent drain current I_D. Note that the selection, adjustment, and confirmation of I_D are an important part of the basis on which your report will be graded.

In your report:

1. Show how you calculated the optimal quiescent drain current.
2. Show data for the measured quiescent gate and drain voltages, and the quiescent drain current. You may measure the latter by inserting a 10-ohm resistor in series with the power supply VDD line and measuring the voltage drop across it with a digital voltmeter. If you wish, you may use this same method to measure I_D while setting the current.
3. Show how you designed your RC network, including your calculation of its nominal cutoff frequency.
4. Calculate the expected low frequency cutoff due to the transformer magnetizing inductance. For this you should use and show a reasonable model of the transformer as driven by a signal current source.
5. Give a qualitative evaluation of the functioning of the circuit.
6. Using SPICE, simulate the required voltage to bias the MOSFET and compare it to your empirical determination. (The simplest way to do this is to replace the bias resistors by a Thevinen equivalent and sweep the equivalent voltage with a .DC analysis command line.)
7. Use SPICE to simulate the frequency response of the entire circuit over the range of 20 Hz to 10 KHz. For the transformer you may use the transformed resistance of the speaker in parallel with the primary magnetization inductance. Use 1600 pf in series with a voltage source for the signal.

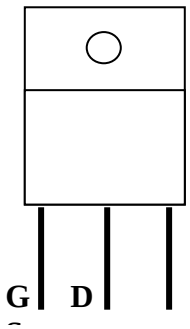


NOTE: MOSFETs are discussed in chapter 6 of Razavi. We will discuss MOSFETs in class near the end of March. You do not need to know much about them to do the lab since the lab is largely independent of the details of the device! Field effect transistors differ from BJTs in a couple of ways that are important here and which make the lab easier. The gate of an FET is its control terminal in the same sense as the base of a BJT is for it. However, the gate draws no steady DC or bias current at all. Superficially the drain current vs. drain voltage curves with V_{GS} as the curve parameter look just like those of a BJT. The main difference besides the lack of gate current is that the gate voltage for a given drain current is larger than V_{BE} for a BJT and tends to be less repeatable from unit to unit. Interestingly nothing in the consideration of the "best" Q-point for a single stage amplifier depends on the differences in the device types.

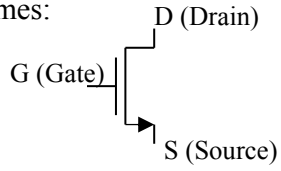
IRF610PbF: *n*-channel enhancement-mode MOSFET made by the DMOS (diffused MOS) process

Maximum V_{DS}	200 V
Maximum I_{DS}	2 A
Maximum P	25 W (on heatsink with ambient temperature 25 °C)
Threshold, V_T	2.0 to 4.0 volts; 3.0 (typical)
Saturation, V_{DSSAT}	1 V (approximate - V_{GS} dependent)

IRF610 MOSFET
Front View



MOSFET Symbol
Terminal Names:



EXPERIMENT NO. 4 - Audio Frequency Amplifier

This lab introduces you to some very common aspects of design through a very simple single transistor amplifier. In this lab you will get your first design experience with the concepts of small signal analysis and will get some further experience with biasing. These concepts are fundamental to circuit design, so make sure you understand them, and the distinction between them. In addition, this lab requires you to use some common measurement techniques. The experiment is quite simple relative to some of the later ones, and should not take you much time in the lab. As your first design, it may require substantial thought beforehand.

The Experiment

Design, build, and characterize an amplifier having the following specifications

Gain: $|A_v| = 15 \pm 20\%$, (23 DB +/- 1.5 DB) from 100Hz to 10kHz
Input Impedance: 10 kΩ ± 2 kΩ @ 1kHz
Output Impedance: <6kΩ @ 1 kHz
Output Voltage Swing: at least ±2.5 volts from quiescent point
Low Frequency Rolloff: -3dB point (relative to midband gain) must be kept below 30Hz

Your amplifier should run from a single 12V power supply, and be based on the 2N2222A (NPN) transistor, which has the following specifications:

$BV_{CEO} = 30V$
$70 < h_{FE} \approx h_{fe} < 230$ @ l mA (typ. 130)
$P_D = 300mW$
$r_O > 150k\Omega$ typical @ 1 mA and 6 volts

Through the proper choice of biasing components, your circuit should meet design criteria for the full range of h_{FE} (70 to 230) and for $0.50V < V_{BE} < 0.70V$. It is <u>not</u> sufficient for you to make your circuit work for one particular set of components - it must be designed to work for any components that meet the appropriate specifications (i.e. $70 < h_{FE} < 230$, resistor values ± 5%, etc.). Gain and output impedance are primarily dependent on the passive components. It is the input impedance and Q-point that vary significantly from one device to another and over temperature. <u>You will be graded stringently on meeting the requirements by design for these circuit parameters</u>.

SPICE can be used to check that a design meets its requirements by simulating with a worst case range of temperature and device models. I only have a typical model for the 2N2222A but temperature is the main reason for variation in V_{BE} so simulate a typical instance of your design for the Q-point and the input impedance at 1 KHz for -20 C, 27 C, at 80 C, the range of operating conditions for some industrial and consumer products. (SPICE simulates the circuit at 27 C by default and the directive to change that is ".OPTIONS TNOM=<Value in deg. C>.)

A common emitter amplifier with a partially bypassed emitter circuit will work. You must choose the passive component values so that your circuit functions as required. Your report should contain:

- Very short introduction
- Schematic
- Description of how you chose your component values, along with calculations of quiescent voltages and currents, gain, input impedance and output impedance; show hand calculations for the limits of (I_C, V_{CE}) over variations in h_{FE} and V_{BE}.
- Measurements of quiescent voltages
- Printout of the Bode plot of the amplifier taken on one of our computerized plotters showing that the amplifier conforms to the design specifications. The printout must show your protoboard number and have the TA's magic number.
- Measurements of input and output impedances at 1kHz. Be explicit about the connections and component values you use to make these measurements.
- SPICE run data as per above to confirm your design goals were met over temperature.

HINTS

1. It is often easier, in this type of design, to satisfy the small-signal design specifications first, and then choose biasing components, which, consistent with small-signal requirements, fulfill the remaining requirements of quiescent point stabilization and large-signal properties such as output voltage swing. Work backwards from the output impedance.

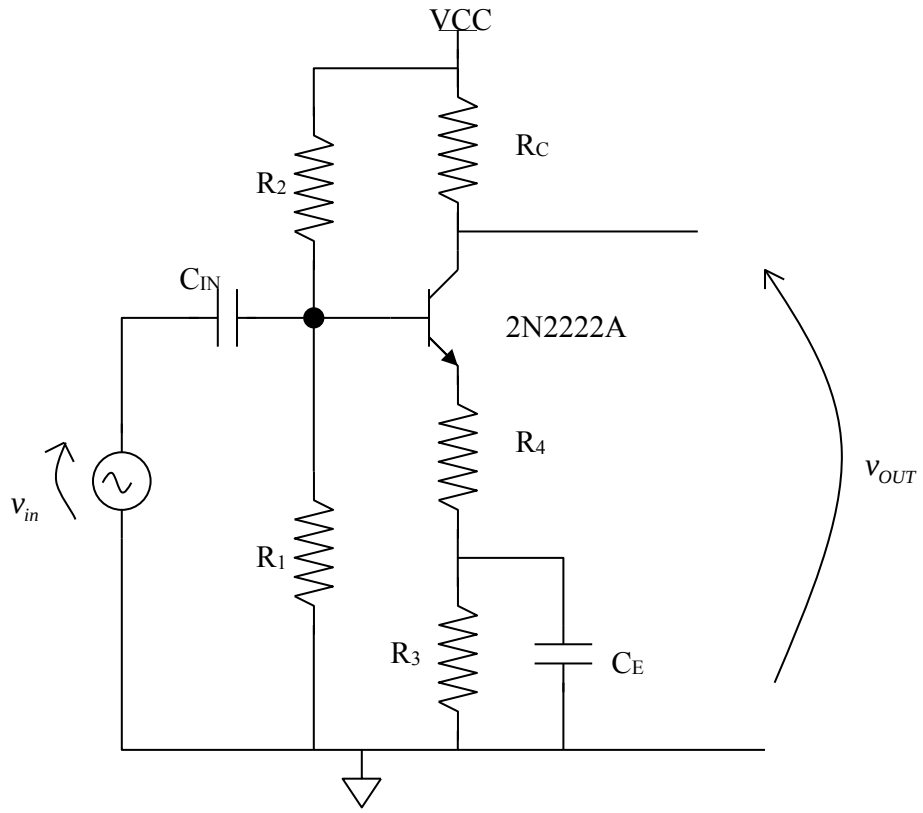
2. The tolerance on the input impedance is a limit; it is not required or desirable that this limit be met exactly for the limits of transistor current gain. Given that the current gain is so variable, it must be necessary to maximize z_{tr} so that R_{BB} is the primary determinant of Z_{IN}. It makes more sense to minimize the effect of beta on the circuit consistent with meeting the other requirements, particularly meeting the output impedance and in-band gain requirements, without worrying about the variability of Z_{IN}.

3. Design the Q-point around the typical device and then check that the input impedance tolerance is met. Choose the total emitter resistance so that you can hope to meet the requirements for variation in V_{BE} over temperature.

4. Use standard resistor values and do not series or parallel connect them to make intermediate values. Resistors have tolerance (+/-5 %) and you cannot realistically count on doing any better than nominal. In the 4 to 7 kilohm range, the standard values are 3.9K, 4.3K, 4.7K, 5.1K, 5.6K 6.2K and 6.8K.

5. Input impedance is most easily measured by placing a resistor comparable to the expected input impedance in series with the signal source. You measure the input current from the voltage across this resistor. Use <u>two</u> oscilloscope probes, one connected to each side of the resistor, and set the scope to measure the difference in the voltages (invert one scope channel and sum them). Be sure both channels are set to the same sensitivity. (This approach to measuring the input current is suggested because it is simple to predict when it will work. Instruments such as bench voltmeters and DVMs usually have too much capacitance and too little frequency response to be used except at quite low frequencies. The differential scope method works well to quite high frequencies.)

6. The output impedance can be measured using a similar technique to what you used in lab #1. You add a load and note the change in output voltage, calculating back to the output resistance that would account for the change. The only trick is to connect the load resistor so that the quiescent point is not disturbed so much that the amplifier ceases to work properly. That means the DC collector voltage must not change as you add the 1 KHz load. Think about how you might introduce a load at 1 KHz without changing the Q-point at all!



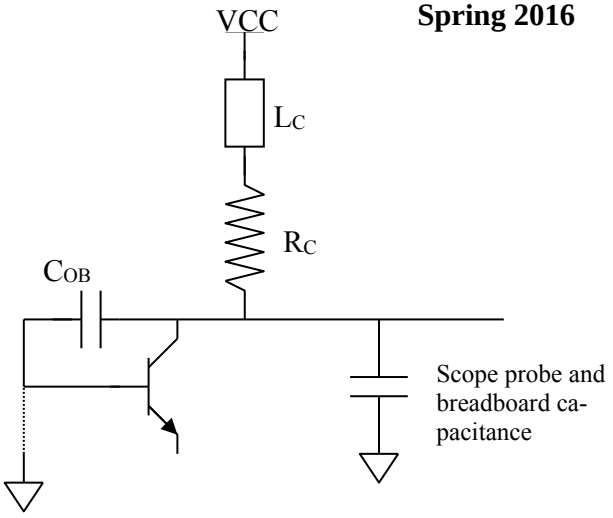
Circuit Topology for a Common Emitter Amplifier Based on the 2N2222A

EXPERIMENT NO. 5 - Video Amplifier

The bandwidth for older television video signals in the United States (the NTSC standard of 1947) was approximately 30 Hz to 4 MHz. The first digital TV standards required a 3 DB video bandwidth of 30 Hz to 6 MHz and this bandwidth was used for the last TVs and displays that used cathode ray tubes (CRTs). There was a common design problem with large-screen, cathode ray tube displays, in which a modest video signal level on the order of 2.2 volts pp drove the grid of a CRT electron gun directly. An amplifier capable of providing the required gain, bandwidth, and output voltage was a standard feature of all TVs and monitors using CRTs. Suppose that our 6 MHz TV required a CRT drive level is from +20 to +65 volts relative to ground and that in addition to the +12V supply (from which to derive base biases), 80 VDC can be obtained from a high voltage supply in the lab. Design and build an amplifier that will give a 30 Hz to 6 MHz bandwidth as defined by its lower and upper 3 DB points. The circuit is to have a minimum input impedance of 1,000 ohms over the entire frequency range. Simulate the capacitive loading of the CRT grid with the 10x oscilloscope probe (about 15 pf capacitance).

You will probably find that these design requirements cannot be met with a simple common emitter amplifier, and that a cascode configuration will be necessary. The cascode connection reduces the Miller effect, which helps keep the input impedance high. Also, it is difficult to combine high cut-off frequency, high breakdown voltage, and high power handling in one transistor. The cascode circuit eases these demands by dividing the requirements between two transistors. Design the circuit around 2N3440 and 2N2222A transistors. The maximum power dissipation for a 2N3440 is 1 watt in an ambient temperature up to 50°C. Design your circuit conservatively to have the 2N3440 dissipate no more than about .65 W. Design around typical values of all transistor parameters. A table of some of the parameters is given below; more complete data is available in the Appendix.

A complication in the problem is that the capacitances shunting the output are substantial. In addition to the scope probe and C_{OB} of the 2N3440 there can be up to 2 pf between terminals of the breadboard. You will probably find that this capacitance limits the upper frequency cut-off from the collector load pole to something under 4 MHz. There is a standard method for increasing the bandwidth by putting a coil in series with the collector resistor as shown below.



For this circuit, the data shown below gives the relation between the inductance L_C and the bandwidth. The frequency f_{max} is the cutoff frequency with no inductor, *i.e.*, $f_{\max} = \frac{1}{(2\pi R_C C_{shunt})}$ where C_{shunt} is the total capacitance to ground from the output node. Use this configuration to move the 3DB cutoff frequency (i.e., the frequency at which the gain decreases by a factor of .707) out as needed. There is a selection of small RF chokes (coils) available from the TA. You may check out and return what you need. (The coils look much like resistors ($ .02 ea.) but cost about a dollar each. You must return these and not treat them as casually as resistors.) The color code on coils is the same as for resistors; the units are microhenries. (The coil color code can be difficult to be sure of because the colors are not well printed. There is an R-L-C meter in the lab to check with.)

Note that 6 MHz is an appreciable fraction of the 250 MHz common base cutoff frequency of the 2N2222A. In calculating input impedance you will have to take account of that fact. Also, the Q-point will have to be stabilized in such a way as to account for the range of h_{FE} of the common emitter transistor and for $.5 < V_{BE} < .7$ volt. I_{CBO} should not be a problem. Be sure to show you have met this requirement by design.

Wiring can cause problems in a circuit like this. You will reduce or avoid such problems if you keep it neat with short leads. One unhappy fact of life at high frequencies is that power supplies may not be high frequency signal grounds unless one puts a small capacitance (typically .1 to .01 μfd.) between the supply and ground physically located right at your circuit. The best kind of capacitor is a ceramic disc type; it is commonly called a bypass capacitor. This observation applies to both the 12-volt supply on the breadboard station and to the 80-volt supply, which will have to come from 0 to 120VDC supply on the back bench. Any electrolytic capacitors should be bypassed as well, because they often have significant series inductance.

Measure the gain over the range from 10 Hz to 10 MHz. This requirement must be met with a plot from the automated Bode plotter. Make a SPICE simulation of the frequency response and use that to calculate the input impedance of the circuit. Measuring the input impedance is tricky so I will let you substitute the SPICE value for a measurement. Also, record the quiescent circuit voltages. Please try to minimize component damage by checking your wiring before applying power. If you have a problem, check the devices on the curve tracer.

Write-up: In your write-up do the following:

I. Indicate how you arrived at component values.

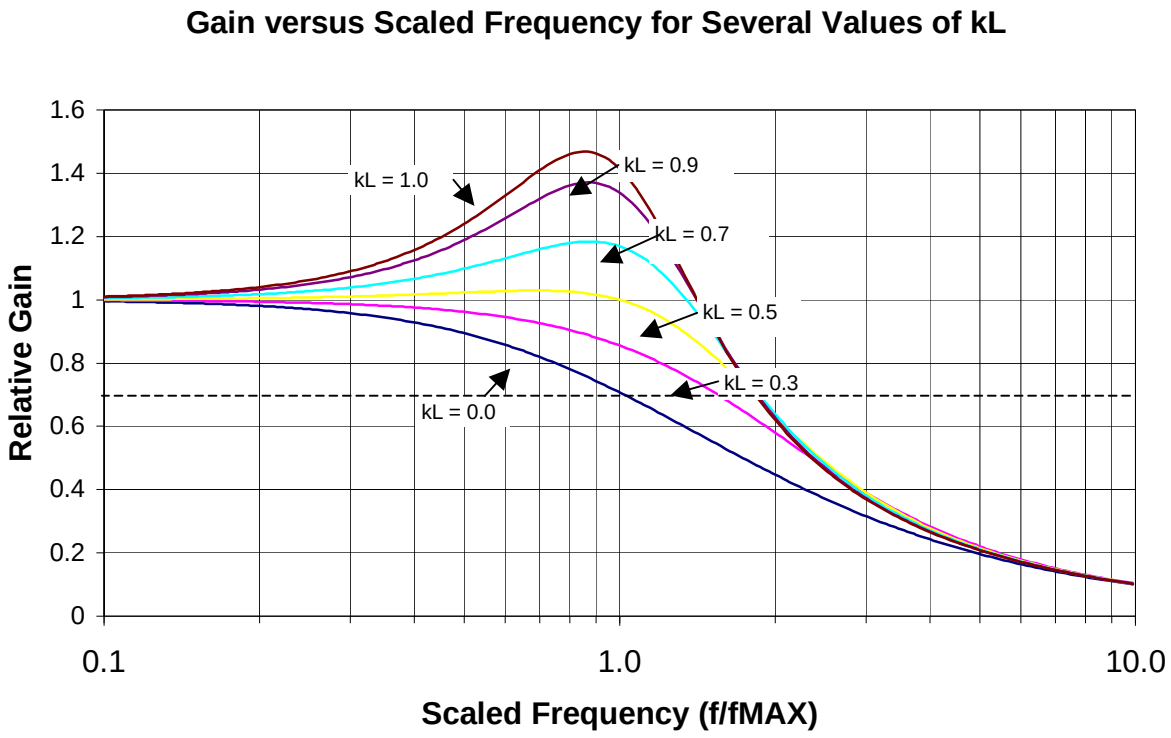
II. Calculate the input impedance of the whole circuit for typical transistor parameters at 6 MHz. Compare this to the value from your SPICE simulation. (Note that if you meet the input impedance requirement at 6 MHz, you do so automatically for all frequencies below that too.)

III. Calculate the limits on the quiescent current due to transistor parameter variations.

IV. Derive the relative gain formula for the circuit including the effects of the inductor. (See discussion below.)

V. Report your measurement results for both the Q-point and the frequency response (Bode plot) with an explanation of any discrepancy with calculation.

VI. Make a SPICE run of the frequency response of the circuit for the same range as your measurements and show how that compares with the measured response.



Relative Gain Calculations: The collector impedance, Z_C, made up of R_C, L_C, and C_{SHUNT}, dominates the high frequency gain of this circuit and its dependence on frequency determines the relative gain of the amplifier. This combination of passive components occurs at various scales in many applications and is best analyzed in dimensionless terms. The relative amplifier gain will be the dimensionless ratio $|Z_C| / R_C$. If the inductor is not present the circuit has sin-

gle pole behavior with a cutoff frequency given by f_{MAX} defined above. Scaling all frequencies by this value makes the frequency scale dimensionless too. Finally, one can express the inductance as the product of a dimensionless coefficient k_L as:

$$L_C = k_L R_C^2 C_{shunt}$$

As **part of your write-up, show** that the relative gain is given by the expression:

$$\frac{|Z_C|}{R_C} = \frac{\sqrt{1+[k_L^2(f/f_{\max})^3+(1-k_L)(f/f_{\max})]^2}}{(f/f_{\max})^2+[k_L(f/f_{\max})^2-1]^2}$$

This formula was used to calculate the family of curves on the graph above. The graph is quite handy for picking L_C based on how much additional frequency response is required.

Selected transistor data. See the data sheets for more details.

Transistor type	Parameters				
	C_{OB} (pF)	f_T (MHz)	BV_{CBO} (V)	BV_{ECO} (V)	P_D (W)
2N2222	7 @ V_{CB}=10 V	250	60	30	0.3
2N3440	4 @ V_{CB}=40 V	25	300	250	1.0

HINTS:

1. The collector resistor is fixed by the maximum power dissipation requirements. Use the maximum power theorem, which states that a voltage source in series with a resistor R and a load will transfer maximum power to that load when half the voltage is across R and half across the load. That power is $V^2/4R$. The trick is to identify the voltage that goes with applying this theorem to your circuit.

2. Pay attention to heat in the collector resistor – it will be too much for the standard quarter watt resistors you use for most of the labs. There is a separate set of 2 watt power resistors among the supplies in the back corner. Please return any resistors to the right drawer when you are done. See also the comments on resistors in the introduction.

3. The quiescent current is set by the midpoint of the output drive levels.

4. V_{CB} for the 2N2222 is set by a compromise between too low a value increasing the value of C_{OB} and too high a value giving an unstable Q point. A reasonable compromise here is $\approx$ 4 to 8 V.

EXPERIMENT NO. 6 - Sine Wave Oscillator

Sinusoids are useful waveforms, because they are convenient basis functions for analyzing the response of (linear) systems. Any sufficiently well-behaved signal can be represented by a linear combination of sinusoids (through Fourier or Laplace transforms) and derivative and integral operations on any of the basis functions yields another basis function of the same frequency. In fact, sinusoids are the only functions that retain their original shape during processing by a linear system, which makes it easy to characterize the effect of the system on a sinusoid by specifying only the amplitude and phase change. In mathematical language, sinusoids, or rather exponentials with pure imaginary arguments, are the eigenfunctions of all linear systems. Consequently, sine wave generators are useful tools for circuit testing and diagnosis (as you have already seen in the previous labs). In this lab, you will design a variable frequency sine wave generator. Although the approach you use cannot yield a sine wave of sufficient purity (*i.e.* low harmonic content) for use in a high quality generator, the quality of its waveform is sufficient for many less demanding applications. This is a fairly inexpensive way of producing a versatile waveform generator (sine, triangle and square waves simultaneously) over a broad frequency range.

The approach you will use involves the generation of a triangle wave followed by converting the triangle wave to a sine wave using a nonlinear circuit. It is relatively easy to generate a high-quality variable frequency triangle wave using an operational amplifier integrator circuit with a variable input resistor. (Alternatively, it is easy to convert a variable frequency square wave to a triangle wave using an integrator). The triangle wave generator will be made using a combination of an integrator and a Schmitt trigger as shown in the figure below. Although in practice the integrator and Schmitt trigger functions can be integrated into a single fairly simple circuit, the approach outlined in this lab will give you exposure to two opamp applications (integrators and Schmitt triggers separately).

A circuit having the block diagram shown on the next page can generate a triangle wave. The Schmitt trigger circuit itself is an operational amplifier wired for positive instead of negative feedback. An inverting amplifier topology in which the opamp's input terminals are swapped will make a non-inverting Schmitt trigger circuit. When the Schmitt trigger output is negative, the integrator output ramps up. When that output reaches the positive-going threshold of the Schmitt trigger, the Schmitt trigger output goes positive. This causes the integrator output to ramp downward until the Schmitt trigger's negative going threshold is reached. This sends the Schmitt trigger output negative, and the cycle repeats.

The symmetry of the triangle wave depends on two things. First the negative and positive outputs of the Schmitt trigger must be equal in magnitude to obtain equal slopes for the positive and negative going parts of the triangle wave. Second, the positive and negative switching points of the Schmitt trigger, which must be equal magnitude, control the positive and negative peaks of the triangle wave. Although an opamp-based Schmitt trigger will not precisely meet these two conditions, the accuracy will be acceptable for the purpose of this experiment. Your task is to determine how to implement the integrator and Schmitt trigger in such a way as to yield a triangle wave generator having a frequency range of at least 100Hz to

10kHz. You will be allowed one 10 kΩ potentiometer for adjusting the oscillator frequency. The input resistor of the integrator (R_I in the figure) must be higher than 3 K so that the load on the square wave amplifier is never less than 2.5 K. The amplitude of the square wave only needs to be greater than 5 volts pp, however, the triangle amplitude should be as near as practicable to 5 volts pp and some grade penalty will be attached to a discrepancy of more than +/- 10 %. You cannot use an electrolytic capacitor in the integrator.

The triangle to sine conversion circuit you will use is an example of a class of nonlinear circuits. It utilizes the nonlinear I-V characteristics of the base-emitter junctions of bipolar transistors. Attached is a copy of the original journal article (R. G. Meyer, W.M.C. Sansen, S. Lui, and S. Peeters, *The Differential Pair as a Triangle-Sine Wave Converter*, IEEE J. Solid-State Circuits, Vol. SC-11, June 1976, pp. 418-420) describing this triangle to sine conversion technique. Using a single CA3083 NPN transistor array chip, design and construct a circuit following the technique outlined by Meyer, et al. It is almost certainly easiest to use the collector output option rather than the emitter option that they also mention. The combination of this circuit with your triangle wave generator will be a variable frequency sine wave generator. You probably have to put something between the triangle output and the sine-converter input to reduce the signal amplitude to an appropriate value. The output sinusoid shall be 5 volts pp too and have a zero mean value. The output source impedance shall not exceed 100 ohms. (This does not mean you could load the circuit with 100 ohms! You may meet this requirement by design.) You very likely need another opamp to do this. It is probably best to use it as a differential amplifier, taking the difference in potential between the two collectors of the sine converter. This reduces distortion and saves a capacitor. As a difference amplifier is a little harder to design, I will reserve points on the lab grade specifically for doing this successfully.

In demonstrating your circuit to the TA, you must show reasonably distortion-free sine wave generation from 100 Hz to 10 kHz. Distortion must be reduced by proper selection of passive components in the triangle wave oscillator. To establish a quantitative measure of the distortion of the sine wave, use an oscilloscope to capture the signal when your generator frequency is about 1 kHz. Use a sampling rate of at least 100 kHz and try to adjust for as near to ten cycles of the waveform on screen as practicable. Fill the vertical scale as fully as possible without clipping. Capture the data on a flash drive and process it in EXCEL and use it or another package to calculate the FFT. From the peaks in that transform calculate the ratios of the second through fourth harmonics to the fundamental. To meet the requirements of the lab, the amplitudes of the second and third harmonics must be at least 23 DB below the fundamental. Also capture the square and triangle outputs of your circuit at 1 KHz. In your report, overlay them with the sine wave data **all on the same time axis**. As in lab 1, the TA will give you an electronic signature to include on your graph when you demonstrate your triangle and square wave outputs to him.

The report should include the usual brief introduction and a section that shows the logic of your component choice. In the section that has the tabulation of measured and designed values, please include at least:

1. Amplitudes of all waveshapes at 100 Hz, 1 kHz, and 10 KHz.

2. Distortion of the sine wave -- FFT printout and the derived ratio of the second and third harmonics to the fundamental amplitude. Make your FFT printout have a DB scale and normalize so that the fundamental is at 0 DB.
3. Waveshapes of all outputs at 1 KHz overlaid on the same time axis.
4. Maximum and minimum frequencies.
5. Quiescent values of the voltages in the sine converter
6. DC or mean value of the sinusoidal output -- i.e. is it really zero mean?

Hints:

1. Bypassing the power supplies with small ceramic capacitors on the breadboard will help avoid spurious oscillations.

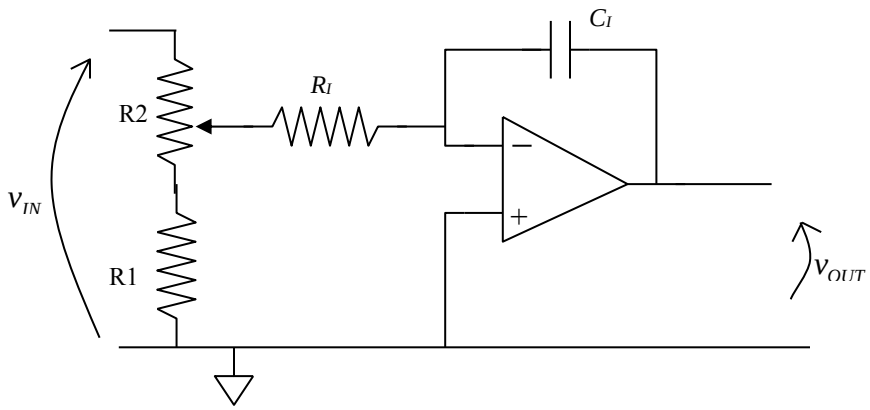
> ***WARNING: Pin 5 (SUBSTRATE) must be connected directly to the*** V_{EE} (-12 volt) supply line in order to isolate one transistor from another. All 5 transistors in the CA3083arrays can be wired freely as needed as long as that substrate connection is made. We don't like wholesale destruction of these devices so please be careful.

2. The transistors in the CA3083 array have their highest gain and best frequency response when biased at just over 10 ma. This would imply that the maximum quiescent current for your circuit should be no more than 5 ma so that performance will remain high as the circuit transfers current preferentially to one side of the differential amplifier. Probably somewhat lower still, somewhere in the range of 0.2 to 2 mA, would result in best performance.

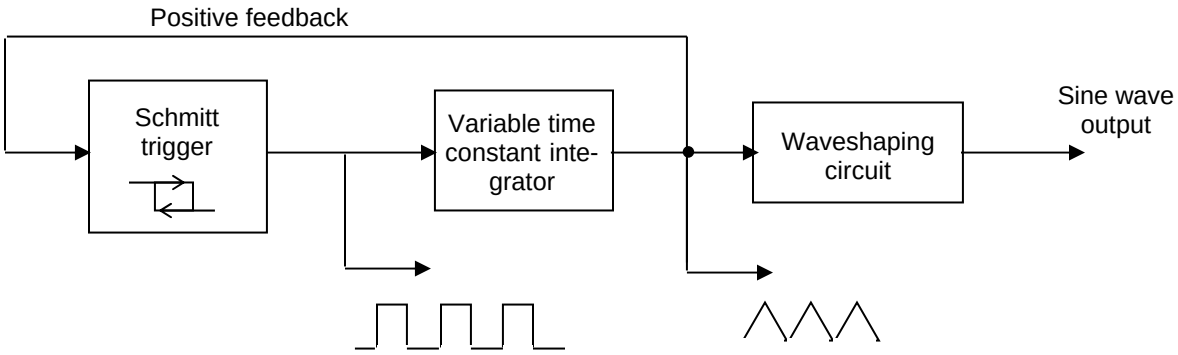
3. One technique for realizing a variable time-constant integrator is shown below. Notice that the potentiometer, R2, is a three terminal device. You **are not just making** the integrator input resistor a variable one. (That will not work satisfactorily.)

4. Some small but annoying anomalies can be avoided by using a 1X buffer between the triangle output of the integrator and the input to the Schmitt trigger. This prevents the latter from adding glitches to the triangle.

5. The amount of distortion is sensitive to any DC offset at the wave-shaper input. That can be caused by the base current of the BJTs if the source impedance of the signal is too high or the resistances of the two bases of the differential pair are unbalanced too much.



Variable Time Constant Integrator



Function Generator Block Diagram: the Schmitt trigger and integrator form a square and triangle generator. The waveshaping circuit uses a differential pair with current source biasing and an emitter resistor. (See attached article.) You should have an opamp buffer in that circuit to minimize distortion and lower the output impedance.

Correspondence

The Differential Pair as a Triangle-Sine Wave Converter

ROBERT G. MEYER, WILLY M. C. SANSEN, SIK LUI, AND STEFAN PEETERS

Abstract—The performance of a differential pair with emitter degeneration as a triangle-sine wave converter is analyzed. Equations describing the circuit operation are derived and solved both analytically and by computer. This allows selection of operating conditions for optimum performance such that total harmonic distortion as low as 0.2 percent has been measured.

I. Introduction

The conversion of triangle waves to sine waves is a function often required in waveshaping circuits. For example, the oscillators used in function generators usually generate triangular output waveforms [1] because of the ease with which such oscillators can operate over a wide frequency range including very low frequencies. This situation is also common in monolithic oscillators [2]. Sinusoidal outputs are commonly desired in such oscillators and can be achieved by use of a nonlinear circuit which produces an output sine wave from an input triangle wave.

The above circuit function has been realized in the past by means of a piecewise linear approximation using diode shaping networks [1]. However, a simpler approach and one well suited to monolithic realization has been suggested by Grebene [3]. This is shown in Fig. 1 and consists simply of a differential pair with an appropriate value of emitter resistance R. In this paper the operation of this circuit is analyzed and relationships for optimum performance are derived.

II. Circuit Analysis

The circuit to be analyzed is shown in Fig. 1(a). The sinusoidal output signal can be taken either across the resistor R or from the collectors of $Q1$ and $Q2$. The current gain of the devices is assumed large so that the waveform is the same in both cases.

The operation of the circuit can be understood by examining the transfer function from V_i to current i flowing in R. This is shown in Fig. 1(b) and has the well-known form for a differential pair. The inclusion of emitter resistance R allows the curvature to be adjusted for optimum output waveform, as will be seen later.

When a triangle wave input of appropriate amplitude is applied as shown in Fig. 1(b), the output waveform is flattened by the curvature of the characteristic and can be made to approach a sine wave very closely. As with all such circuits, the distortion in the output sine wave is dependent on the input amplitude and this must be held within certain limits for acceptable performance.

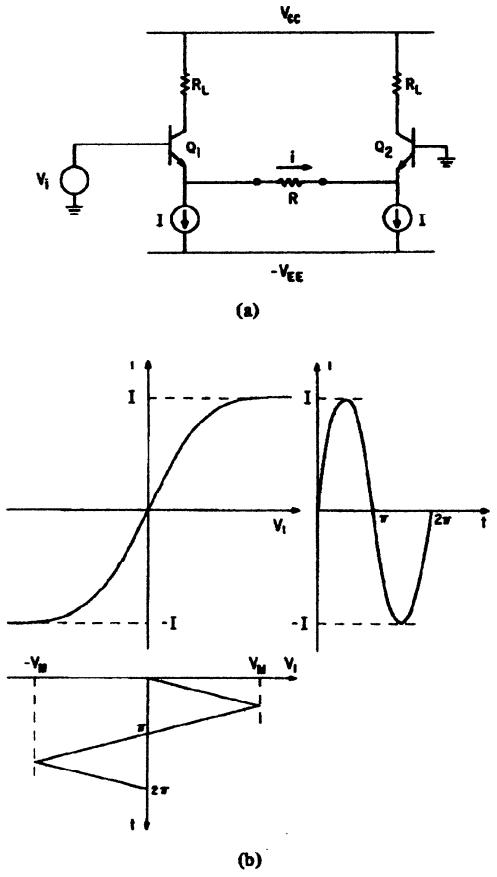


Fig. 1. Triangle-sine wave converter. (a) Circuit schematic. (b) Transfer function.

In the following analysis, $Q1$ and $Q2$ are assumed perfectly matched, although in practice mismatches will occur and give rise to second-order distortion (typically less than 1 percent). However, introduction of an input dc offset voltage has been found to reduce second-order distortion terms to negligible levels and they will be neglected in this analysis. The presence of such an offset does not affect the following analysis. From Fig. 1(a)

$$V_i = V_{BE1} + iR - V_{BE2} \tag{1}$$

but

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_K} \tag{2}$$

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R. G. Meyer and S. Lui are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

W. M. C. Sansen and S. Peeters are with the Laboratorium Fysica en Elektronica van de Halfgeleiders, Katholieke Universiteit, Leuven, Belgium.

$$V_{BE2} = V_T \ln \frac{I_{C2}}{I_K} \tag{3}$$

where

$$V_T = \frac{kT}{q}. \tag{4}$$

Substitution of (2) and (3) in (1) gives

$$V_i = iR + V_T \ln \frac{I_{C1}}{I_{C2}}. \tag{5}$$

If $\alpha \simeq 1$ for $Q1$ and $Q2$ then

$$I_{C1} = I + i \tag{6}$$

$$I_{C2} = I - i. \tag{7}$$

Substitution of (6) and (7) in (5) gives

$$\frac{V_i}{V_T} = \frac{i}{I}\left(\frac{IR}{V_T}\right) + \ln \frac{1 + \frac{i}{I}}{1 - \frac{i}{I}}. \tag{8}$$

Equation (8) is expressed in normalized form and shows that the output signal i/I normalized to I depends only on normalized input voltage V_i/V_T and factor IR/V_T. Because of the small number of parameters in (8), it is readily solved in normalized form by computer to yield a series of curves specifying the circuit performance. Before this is pursued however, it is useful to consider an approximate analytical solution of (8) which gives some insight into the circuit operation.

The log term in (8) can be expanded as a power series

$$\ln \frac{1 + \frac{i}{I}}{1 - \frac{i}{I}} = 2\frac{i}{I} + \frac{2}{3}\left(\frac{i}{I}\right)^3 + \frac{2}{5}\left(\frac{i}{I}\right)^5 + \cdots \tag{9}$$

for

$$\frac{i}{I} < 1. \tag{10}$$

Substitution of (9) in (8) for the circuit transfer function gives

$$\frac{V_i}{V_T} = \left(\frac{IR}{V_T} + 2\right)\frac{i}{I} + \frac{2}{3}\left(\frac{i}{I}\right)^3 + \frac{2}{5}\left(\frac{i}{I}\right)^5 + \cdots. \tag{11}$$

This can be expressed as

$$\frac{1}{\frac{IR}{V_T} + 2}\frac{V_i}{V_T} = \frac{i}{I} + \frac{2}{3}\frac{1}{\frac{IR}{V_T} + 2}\left(\frac{i}{I}\right)^3 + \frac{2}{5}\frac{1}{\frac{IR}{V_T} + 2}\left(\frac{i}{I}\right)^5 + \cdots. \tag{12}$$

The desired transfer function for the circuit is [see Fig. 1(b)]

$$i = K_1 \sin K_2 V_i \tag{13}$$

where K_1 and K_2 are constants, and thus

$$K_2 V_i = \arcsin \frac{i}{K_1}. \tag{14}$$

Expansion of (14) in a power series gives

$$K_2 V_i = \frac{i}{K_1} + \frac{1}{6}\left(\frac{i}{K_1}\right)^3 + \frac{3}{40}\left(\frac{i}{K_1}\right)^5 + \cdots. \tag{15}$$

By comparison of (12) and (15) it is apparent that in order to realize the desired transfer function, it is necessary (but not sufficient) that

$$K_1 = I \tag{16}$$

$$K_2 = \frac{1}{\frac{IR}{V_T} + 2}\frac{1}{V_T}. \tag{17}$$

Equation (16) shows that the peak value of the output current should equal the current source value I. If the input triangle wave has peak value V_M then (13) indicates that for a perfect sine wave output it is necessary that

$$K_2 V_M = \frac{\pi}{2}. \tag{18}$$

Substitution of (17) in (18) gives

$$\frac{V_M}{V_T} = 1.57\frac{IR}{V_T} + 3.14. \tag{19}$$

Equation (19) gives the normalized input triangle wave amplitude for minimum output distortion.

The circuit transfer function given by (12) is to be made as close as possible to the arcsin expansion of (15). If we equate coefficients of third- and fifth-order terms in (12) and (15) we obtain IR/V_T equal to 2 and 3.33, respectively. It is thus expected that the best performance of the circuit will occur for this range of values, and this is borne out by experiment and computer simulation.

III. Computer Simulation and Experimental Results

The solution of (8) was obtained by computer simulation for various values of V_M/V_T (normalized triangle wave amplitude) and factor IR/V_T, and the output signal was analyzed into its Fourier components. Third-harmonic distortion (HD_3) is defined as the ratio of the magnitude of the signal at the third harmonic frequency to the magnitude of the fundamental. Total harmonic distortion (THD) is $\sqrt{HD_3^2 + HD_5^2 + \cdots}$. A typical plot of HD_3 and THD is shown in Fig. 2 for $IR/V_T = 2.5$. It can be seen that the THD null and the HD_3 null occur at about the same value of V_M/V_T, and this is true for any value of IR/V_T. The measured points in Fig. 2 show good agreement with the computed curves and both show a minimum value of THD of about 0.2 percent for $V_M/V_T \simeq 6.6$. This corresponds to $V_M \simeq 175$ mV for $V_T = 26$ mV.

The effect of variations in IR/V_T on the minimum value of THD is illustrated by the computed curve of Fig. 3. At each point on this curve, V_M/V_T was adjusted for minimum distortion. This curve shows that best performance is obtained for $IR/V_T \simeq 2.5$, and this is within the range of 2–3.3 predicted earlier. These results were verified by experimental data.

The effect of temperature variation on circuit performance was investigated by setting $IR/V_T = 2.5$ at room temperature and holding I, R, and V_M constant as T was varied. Measured and computed THD were less than 1 percent from 0° to 55°C. The measured rms output amplitude decreased 5 percent over this temperature range.

The results described above were measured and computed at low frequencies. The measurements were made at frequencies of the order of 100 kHz where the distortion was still frequency independent. Computer simulation neglected all capacitive effects in the transistors. In order to investigate the performance of the circuit at frequencies where charge storage

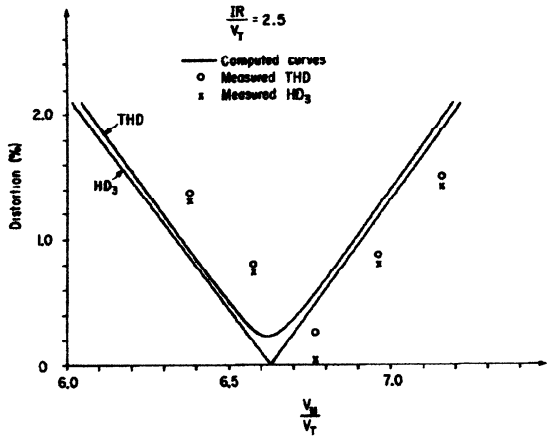

Fig. 2. Computed and measured distortion versus normalized input voltage of the circuit of Fig. 1(a) with $IR/V_T = 2.5$.

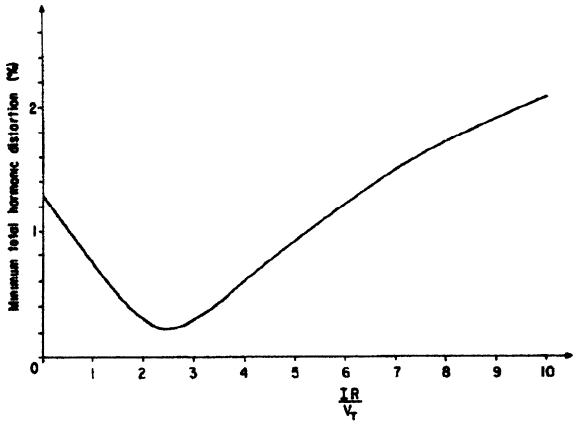

Fig. 3. Computed minimum total harmonic distortion versus IR/V_T for the circuit of Fig. 1.

in the transistors is important, computer simulation was used with input frequencies up to 10 MHz and including a complete, large-signal high-frequency device model. The results showed that THD was independent of frequency up to about 1 MHz. Above this frequency, THD increased rapidly due to irregularities in the peaks of the output sinusoid. This is due to the fact that at the signal peaks, the output current i approaches the current source value I [see (16)], and thus $Q1$ and $Q2$ alternately approach cutoff. The f_T of the transistors in this condition is quite low and they are unable to follow the input signal.

IV. Conclusions

The performance of a differential pair with emitter degeneration as a triangle-sine wave converter has been approached by forming a nonlinear equation in three normalized parameters. The output normalized waveform i/I is a function only of the input amplitude V_M/V_T of the triangle wave, and factor IR/V_T. Computer solution shows that the output sine wave THD has a minimum of about 0.2 percent for $IR/V_T = 2.5$ and $V_M/V_T = 6.6$.

Acknowledgment

The authors wish to thank Dr. A. B. Grebene for suggesting to them the potential of the differential pair as a triangle-sine wave converter.

References

[1] E. H. Heflin, "Compact function generator with enhanced capability–cost ratio," *Hewlett-Packard J.*, pp. 15–20, July 1973.
[2] A. B. Grebene, *Analog Integrated Circuit Design*. New York: Van Nostrand Reinhold, 1972, p. 313.
[3] —, "Monolithic waveform generation," *IEEE Spectrum*, pp. 34–40, Apr. 1972.

Integrated TV Tuning System

W. JOHN WU AND ERIC G. BREEZE

Abstract—**This paper presents a frequency synthesized digital tuning system for UHF/VHF TV receivers and the integrated circuits developed to implement this scheme. The design and performance of the GHz ÷ 248/256 programmable prescaler is described in detail.**

Recent trends in the consumer and communication industry toward more cost effective and more reliable systems place the following requirements on advanced TV tuning systems: meet new FCC regulations; tune all channels (VHF and UHF) individually without complex alignment; be capable of interfacing with digital displays and remote control circuits; have keyboard entry for channel selection; and allow provisions for fine tuning. This correspondence presents a frequency synthesizer which meets all the above requirements and is highly accurate as the phase-locked loop is self-compensating for parameter drifts and component tolerance.

Fig. 1 gives the block diagram of the frequency synthesizer. The dotted block represents a standard VHF or UHF varactor tuner. An amplifier is connected to the VCO output of the tuner to increase the voltage to the acceptable level to drive the digital prescaler. The purpose of the prescaler is to divide down the local oscillator high frequencies to a range that can be processed and counted by TTL or MOS logic circuits. Output of the prescaler is then fed to the programmable counter programmed by the keyboard entry. The output is then compared with a crystal controlled reference frequency. The phase/frequency comparator drives an integrator which in turn provides voltage control to the varactor tuner input [1]. Physical implementation of this scheme requires 5 integrated circuits and will precisely tune 99 channels, the air channels (2 through 83), and the cable channels (84 through 99). The fine tuning provides ±1 MHz in 128 steps. It also has the capability of keyboard entry, channel searching, and channel number display.

The 1 GHz ÷ 248/256 prescaler is designed for this specific

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The authors are with Fairchild Semiconductor, Mountain View, CA 94042.

EXPERIMENT NO. 7 - Telephone Anti-Aliasing Filter

It is now standard practice to send telephone voice service over digital links by filtering the analog signal and sampling this bandwidth-limited signal with an ADC. The standard service uses an 8 Ksps sampling rate, which requires that the signal bandwidth be restricted to below 4 kHz. (All systems which use analog to digital conversion must be careful to limit the high frequency content of the original signal. Nyquist's sampling theorem says that the original signal can only be recovered from the digital samples if the signal had no components beyond one-half the sampling frequency. If this condition is not met, then not only is data lost, but false information may be folded into the real data. If you played around with the FFT settings on the scope in Experiment 1, you may have seen this effect.) Voice service requires that frequency components in the original signal be maintained as well as possible out to beyond 3 kHz. Usually the 3 DB down point is placed at around 3.1 to 3.3 KHz. In this lab you are to design and build a filter which might be used for this purpose using active circuits based on operational amplifiers.

The main difficulty in realizing such a filter is the need for out of band suppression. The minimum suppression I will consider acceptable is 9 DB at 4 kHz. and 30 DB at 8 kHz. The midband gain of the filter subsystem at 1 kHz. should be 20 DB (or 10X) +/- 1.5 DB. At the low frequency end, there should be at least a single pole high pass response so the DC components are removed from the signal. The low frequency response should be down by no more than 6 DB at 100 Hz. You are free to choose any standard transfer function that will be reasonably smooth. If you choose one which exhibits passband ripple (the Chebycheff response, for example) then that ripple should not exceed 1 DB. Probably the simplest acceptable solution is a Butterworth filter of odd order. (Odd order because most of the complication of construction goes into the quadratic pole pairs, and extra rolloff comes with minimal effort with one more simple pole.) You are free to make that filter from cascaded sections of any of the designs that are discussed in your text or in class. There is an automated response measurement available as with labs 4 and 5.

To meet the requirements for response with the tolerances of the components in the lab may require adjusting some resistor values. (You should use mostly film capacitors, as their tolerance of +/- 10 % is the best we can manage. Resistor values come in roughly 10 % increments.)

While I set the rolloff requirement fairly leniently, you should be aware that real systems require more suppression near 4 kHz. This extra attenuation can come at some increase in the transfer function at higher frequencies. The way this is usually done is to use a filter that has one or more zeros on the imaginary axis. A zero of this kind means the filter has no response to sinusoids at the zero frequency. The figure below shows two transfer functions overlaid. The first curve drops very rapidly past 3.1 kHz, going to zero transmission at 4.05 kHz before rising to -37 DB at a little over 5 kHz. This is the transfer function:

$$H(s) = \frac{1}{1 + s\tau_1} \cdot \frac{(s\tau_z)^2 + 1}{(s\tau_2)^2 + \frac{s\tau_2}{Q_2} + 1} \cdot \frac{1}{(s\tau_3)^2 + \frac{s\tau_3}{Q_3} + 1}$$

where

$\tau_1 = 1.51 \cdot 10^{-4}$ sec [1053 Hz]

$\tau_2 = 7.05 \cdot 10^{-5}$ sec [2256 Hz]

$Q_2 = 1.57$

$\tau_z = 3.88 \cdot 10^{-5}$ sec [4100 Hz]

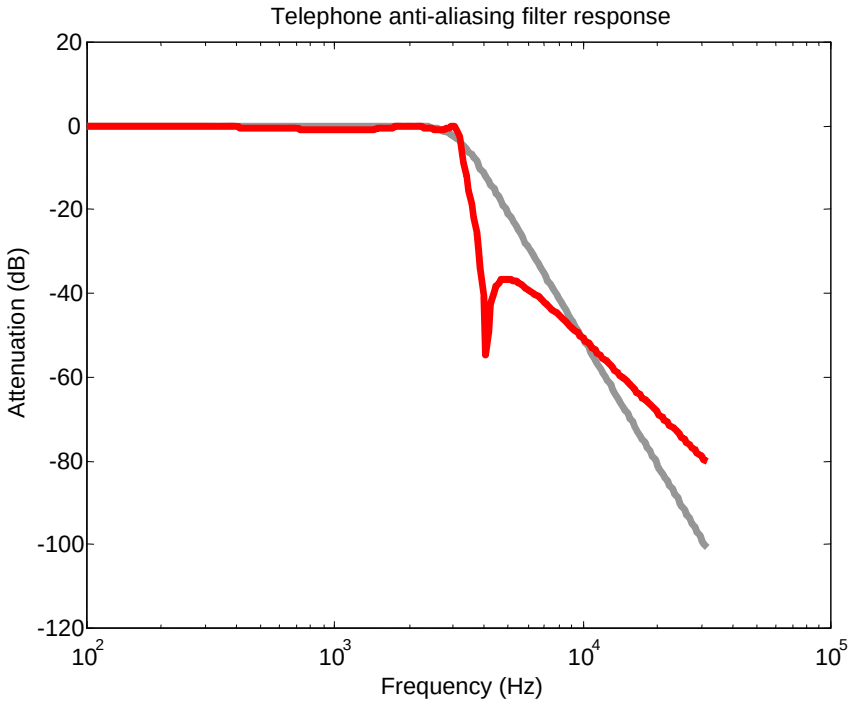
$\tau_3 = 5.14 \cdot 10^{-5}$ sec [3096 Hz]

$Q_3 = 8.07$

The second curve is a 5th order Butterworth filter with its cutoff at 3.1 kHz. Notice that eventually the Butterworth will attenuate more than the first curve, but the filter with a zero does better up to 10 kHz. I am including a reprint from *Principles of Active Network Synthesis and Design* by Gobind Daryananni (John Wiley, NY, 1976) on how to build the section of the filter with the zeros using three or four opamps. If you are feeling adventurous, I would encourage you to try this circuit. It actually is only two or three more opamps than the least complicated acceptable solution. Please feel free to take or ask for more opamps as you need them. You can make the two factors of H(s) that have no zeros in any of the usual low pass topologies – they are not particularly high Q. The section with zeros can be done by following the discussion below.

Writeup: Your lab report should include:

1. Frequency response as measured with one of the Bode plotters.
2. A SPICE simulation of the response as a comparison.
3. Your calculations of component values
4. Full schematic; I would encourage you to use xDxDesigner for the schematic as that gives a neat well document output. The opamps and passive components are in the en162 library.
5. Magic number for this lab.



Realization procedure for zeros on the $j\omega$ axis from Daryannani, *op. cit.*:

10.2 REALIZATION OF THE GENERAL BIQUADRATIC FUNCTION

In this section we describe two methods for the realization of the general biquadratic function of Equation 10.1. The first is based on the summation of the voltages already available in the basic circuit developed in the last section. This

summation requires an extra summing amplifier. The resulting circuit will be referred to as the **summing four amplifier biquad**. The second method uses the feedforward scheme, developed in Chapters 8 and 9, in which the zeros are formed by introducing the input signal at appropriate nodes in the basic three amplifier circuit. This circuit will be called the **feedforward three amplifier biquad**.

10.2.1 THE SUMMING FOUR AMPLIFIER BIQUAD

In the last section it was shown that the voltage at node 1 of the basic three amplifier circuit (Figure 10.4) yields the band-pass function:

$$V_1 = V_{BP} = \frac{-\frac{1}{R_4C_1}s}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}} V_{IN} \tag{10.18}$$

while node 3 exhibits the low-pass function:

$$V_3 = V_{LP} = \frac{-\frac{1}{R_2R_4C_1C_2}}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}} V_{IN} \tag{10.19}$$

The voltage at node 2 is the same as that at node 3 with the sign reversed, that is,

$$V_2 = -V_{LP} \tag{10.20}$$

The band-pass, low-pass, and input voltages may be summed, using a fourth amplifier, as shown in Figure 10.5. The output of the summing amplifier is

$$V_O = -\frac{R_{10}}{R_8}V_{LP} - \frac{R_{10}}{R_7}V_{BP} - \frac{R_{10}}{R_9}V_{IN} \tag{10.21}$$

and the resulting transfer function, obtained by substituting Equation 10.18 and 10.19 for V_{BP} and V_{LP}, respectively, is

$$\frac{V_O}{V_{IN}} = \frac{\frac{R_{10}}{R_8}\frac{1}{R_2R_4C_1C_2} + \frac{R_{10}}{R_7}\frac{s}{R_4C_1} - \frac{R_{10}}{R_9}\left(s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}\right)}{s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}} \tag{10.22}$$

Comparing this with the general biquadratic (for $m = 1, n = 1$):

$$T(s) = -K\frac{s^2 + cs + d}{s^2 + as + b} \tag{10.23}$$

346 THE THREE AMPLIFIER BIQUAD

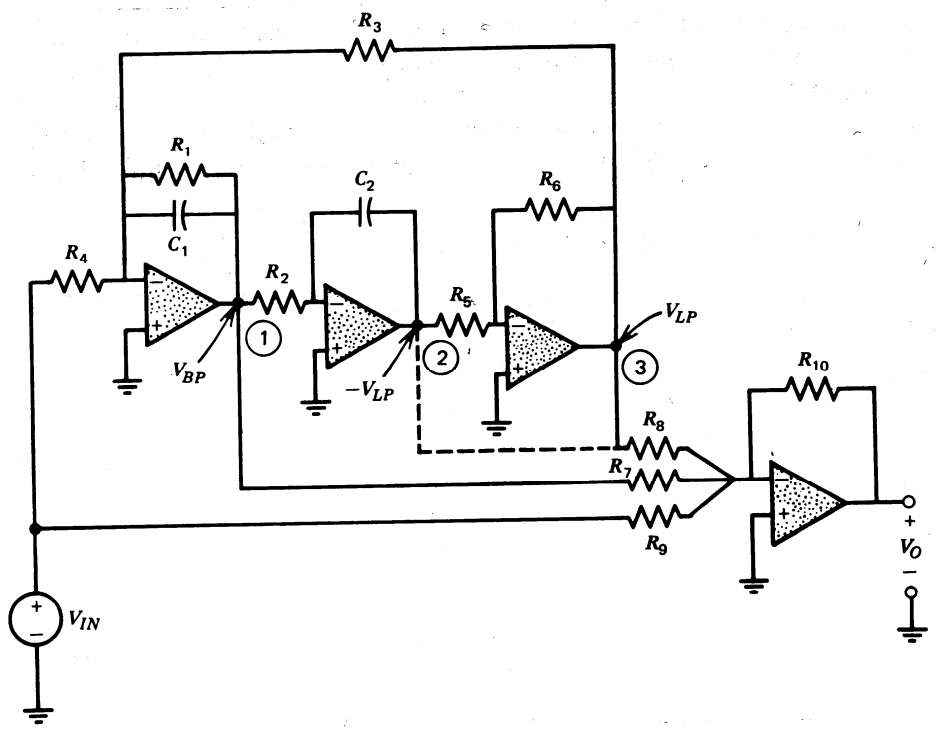


Figure 10.5 Summing four amplifier biquad.

the following relationships are obtained:

$$a = \frac{1}{R_1 C_1} \tag{10.24a}$$

$$b = \frac{1}{R_2 R_3 C_1 C_2} \tag{10.24b}$$

$$K = \frac{R_{10}}{R_9} \tag{10.24c}$$

$$c = \frac{1}{R_1 C_1} - \frac{R_9}{R_7}\frac{1}{R_4 C_1} = a - \frac{R_9}{R_7}\frac{1}{R_4 C_1} \tag{10.24d}$$

$$d = \frac{1}{R_2 R_3 C_1 C_2} - \frac{R_9}{R_8}\frac{1}{R_2 R_4 C_1 C_2} = b - \frac{R_9}{R_8}\frac{1}{R_2 R_4 C_1 C_2} \tag{10.24e}$$

We have five equations and ten elements. Therefore, five of the elements can be fixed. One choice for the fixed elements is

$$C_1 = 1 \qquad C_2 = 1 \qquad R_2 = R_3 = R \qquad R_7 = R_{10} = R \tag{10.25a}$$

Then the remaining elements are given by

$$R_1 = \frac{1}{a} \qquad R_2 = R_3 = \frac{1}{\sqrt{b}} \qquad R_4 = \frac{1}{K(a-c)}$$
$$R_7 = R_{10} = \frac{1}{\sqrt{b}} \qquad R_8 = \frac{a-c}{b-d} \qquad R_9 = \frac{1}{K\sqrt{b}} \tag{10.25b}$$

These synthesis equations yield nonegative element values for

$$a \geq c \qquad \text{and} \qquad b \geq d \tag{10.26}$$

The first inequality requires the zero to have a smaller real part than the pole. This condition is satisfied for all the approximation functions described in Chapter 4, since their zeros were constrained to lie on the $j\omega$ axis.* The second inequality requires that the magnitude of the pole frequency be larger than that of the zero frequency. This restriction can be removed by using V_2 instead of V_3 as the input to the summing amplifier (dotted lines in Figure 10.5). Then the output of the summer is

$$+\frac{R_{10}}{R_8} V_{LP} - \frac{R_{10}}{R_7} V_{BP} - \frac{R_{10}}{R_9} V_{IN} \tag{10.27}$$

It can easily be seen that the resulting synthesis equations will be the same as Equation 10.25, except in this case

$$R_8 = \frac{a-c}{d-b} \tag{10.28}$$

Thus, we see that the summing four amplifier biquad can be used to realize the general biquadratic function of Equation 10.1.

EXPERIMENT NO. 8 - Design of a Bipolar OTA Circuit

When early (ca. 1965) integrated circuits were being designed, it was customary to breadboard them using standard chips with transistors similar to those expected to be made by the ultimate production technology. Now it is usually done by computer simulation alone, but you can still try one the old way. The point of breadboarding is to be sure that there are no undesirable operating modes for the device. It also gives the designer a chance to try the device in practical applications and to revise the specifications if necessary to make them more useful without having to commit to the large costs involved in a set of masks. Although some of the techniques for such breadboarding are not readily available to us, we do have two types of transistor arrays available. You met the CA3083 (5 NPN's) in lab 6 and the other is the CA3096 (3 NPN's and 2 PNP's on one chip).

Design and breadboard an IC circuit which is a voltage input to current output amplifier. (This type of amplifier is called an operational transconductance amplifier or OTA.) If v_1 and v_2 are two input voltages relative to ground and i_0 is an output current running through an arbitrary impedance to ground, then your circuit should realize the function $i_0 = A(v_1 - v_2)$ where A is a constant with units of conductance. If the amplifier output voltage is v_0 and the power supply is ± 12 V then this formula shall hold for $|\ v_0\ | \leq 10$ V and $|\ i_0\ | \leq 1.5$ ma. The common mode rejection ratio is to be ≥ 200 at 100 Hz. The input offset voltage is to be ≤ 10 mvolts; the common mode voltage ≥ ±7 volts; the maximum differential input voltage 5 volts; the minimum value of A = 0.4 amp/V and the minimum differential input impedance 30 kohms.

<u>WARNING: DO NOT USE</u> A
MILLIAMMETER OR A VOLTMETER
ON A MILLIAMPERE RANGE
TO MEASURE CURRENT IN THIS
CIRCUIT

Milliammeters have very low input resistance. Connected between the wrong points in this circuit they can blow out an IC instantaneously. These integrated circuits are expensive so use them with care. Check wiring before applying power and ask a TA to check your circuit configuration for safety. (He will not tell you if it is right, only if he thinks it would destroy an IC.) For current measurements use a voltmeter across a 1.5 K ohm resistor.

In class, in the discussion of operational amplifiers, we cover circuit configurations for all but the current amplifier. The creative part of the experiment is devising a **current output** stage that can both source and sink current. (**<u>Hint:</u>** The output can be the difference between a constant current and a unidirectional, variable current amplifier.)

A block diagram of the circuit is given below. A simple version of the circuit can be built with 8 transistors from 2 chips. The super fanciest version might take as many as 20 tran-

sistors. Build the circuit according to the rules of the next paragraph and test all the above parameters except the maximum input voltage. We expect to have an automated arrangement for measuring the differential gain and input offset. A circuit is given below for measuring the CMRR. It may give you ideas for testing other parameters.

Since this is an IC design, there are certain restrictions on the components that lead to the following rules:

1. No capacitors bigger than 40 pf may be used.

2. Resistors fall into two classes according to the voltage across them. Class 1 resistors may have any voltage across them, but no individual resistor may exceed 39 K and the sum of all Class 1 resistors in the circuit may not exceed 70 K. Class 2 resistors may only have ≤ 3 volts across them, but may have any value from 2 K to 100 K with essentially no restriction on the total number.

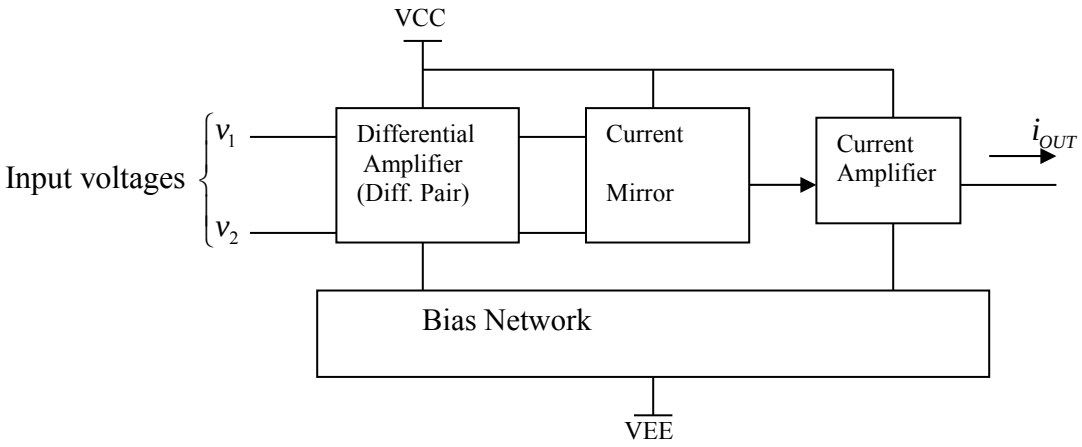
Also, in using the CA3096 transistor arrays, **you must connect the substrate (pin 16) to the most negative voltage** in the circuit in order to keep the transistors isolated. Those of you who find the problem interesting might optionally consider how to add the following features to the circuit:

1. Two nearly identical outputs instead of one, so that one might be a true current output while the other is used for feedback. Alternatively, some OTAs have two differential outputs, that is, one output is the negative of the other.

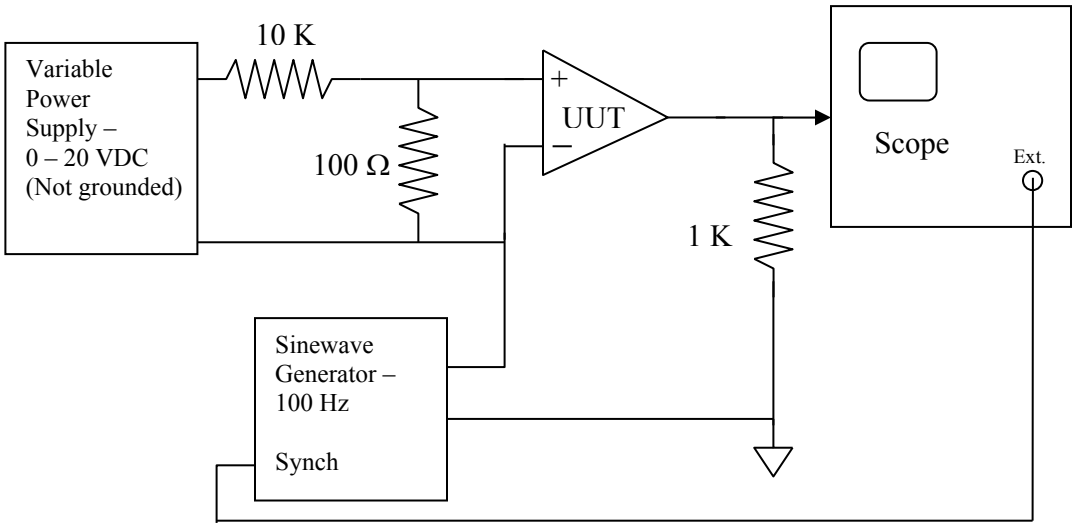
2. Ten times as much input impedance with three times the overall gain.

3. Provision for external adjustment of the input offset voltage.

4. Higher output current and lower power dissipation with two more current mirrors instead of the current amplifier.



Block Diagram



Common Mode Rejection Test Circuit

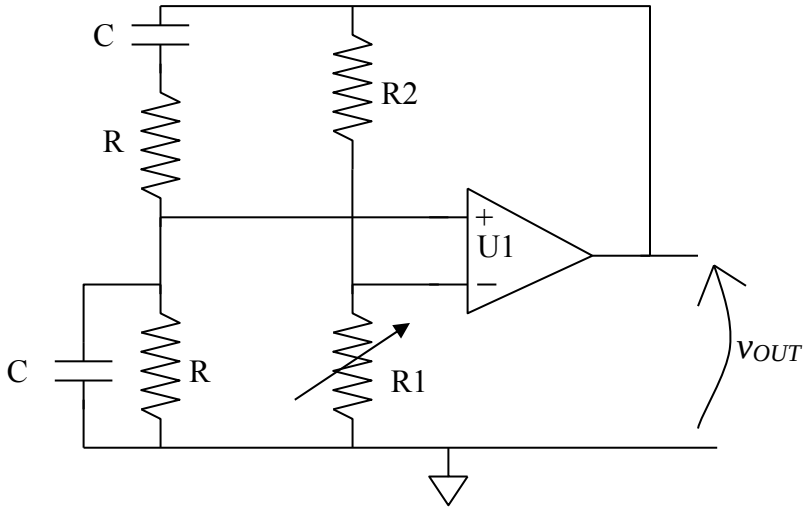
WARNING: At this time (4/18/16) I have not tested this lab myself.

EXPERIMENT NO. 9 – 1 KHz Wien Bridge Oscillator with Low Distortion

Silicon Valley has two famous garages, one in Los Altos where the two Steves are popularly credited with building the first Apple-I computers and the second in Palo Alto where Bill Hewlett and David Packard started Hewlett Packard. The HP garage is now on the National Register of Historic Landmarks and is CHISL # 976 (California State Historical Landmark). In this lab you build the circuit that was the basis for HP's very first product, the Model 200A (10 Hz to 300 KHz) audio frequency sinewave oscillator with very low distortion that was assembled in that garage. (Disney bought some of the first ones to support the production and distribution of *Fantasia*.) You will update Mr. Hewlett's design with a more complicated replacement for his Christmas tree bulb.

Requirements: Build a Wien bridge oscillator with a MOSFET used as a voltage variable resistor to stabilize the output voltage of your oscillator. The oscillator should have 1 KHz +/- 100 Hz frequency and a stable amplitude of 5 volts peak. Measure the harmonic distortion crudely with the Fourier transform built into our oscilloscopes. If you need an extra LF353N or 1N4448, the TA's have a stock of them in the cabinet in room 196.

The Wien bridge oscillator uses an operational amplifier for its basic active element and has two separate feedback paths. One path with two identical resistors (R) and two of the same capacitor (C) is wired for positive feedback. (Notice that this RC network connects to the POSITIVE input terminal of the opamp.) It is a property of this series-parallel circuit that at $f = \frac{1}{2\pi RC}$ there is no phase shift and the amplitude is reduced by a factor of one third.



The second feedback path provides negative feedback through a simple voltage divider formed by R1 and R2. The circuit oscillates when the positive feedback exceeds the negative and stops oscillating when the negative feedback dominates. The problem with this circuit is that

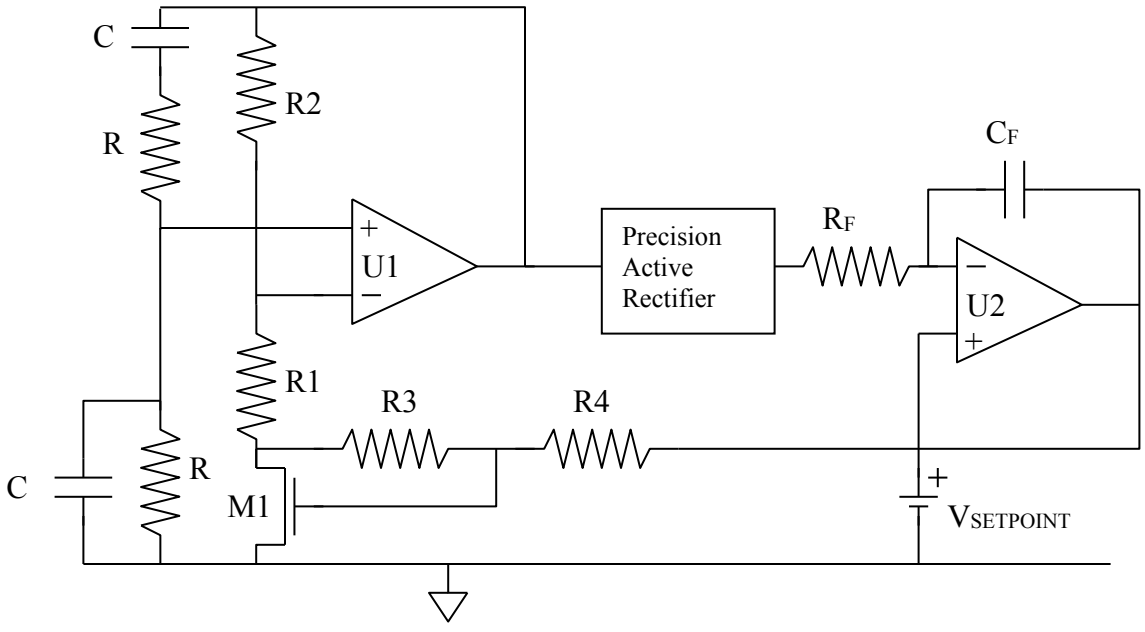
when it oscillates the amplitude is usually limited by the amplifier clipping, that is, the output goes to a peak value determined by the maximum possible output of the amplifier. This generally means very high distortion because the amplifier devices reach saturation or cutoff.

In principle the trick is to adjust R1 so that the circuit oscillates stably with about half the possible output of the amplifier. This requires continuous small adjustment of R1 to compensate for the effects of temperature, aging, and supply voltage variation.

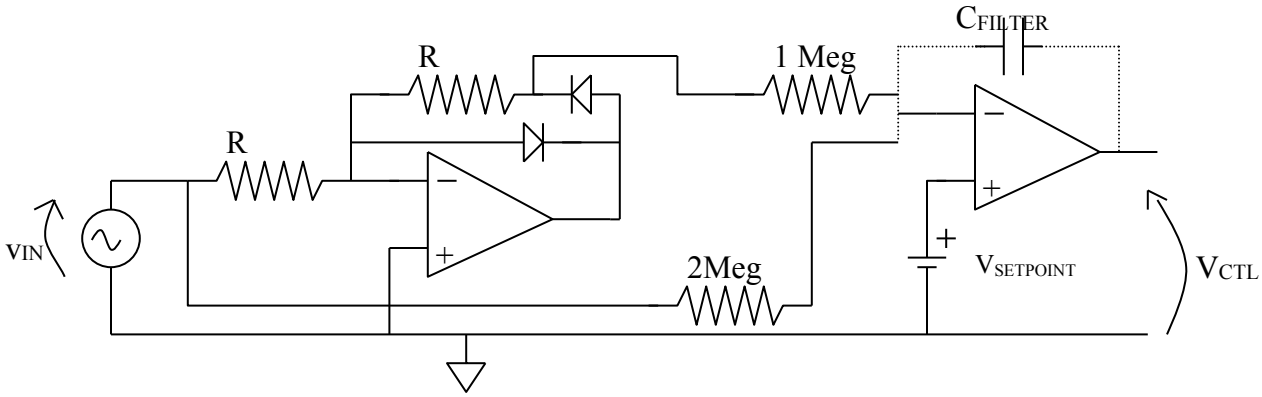
Hewlett solved the problem by replacing R1 with a small incandescent light bulb. (Actually a clear Christmas tree bulb.) Tungsten has a high thermal coefficient of resistance and as the amplitude of oscillation increases, the resistance of the bulb increases because the filament is warmed by the current through it. Increasing R1 increases the negative feedback until it is just enough to sustain the oscillation at the level to keep the bulb warm enough.

You will build the same oscillator but will replace part of R1 with a MOSFET transistor run as voltage variable resistor. A MOSFET with VDS << VGS – VTH acts like a resistor between source and drain that is inversely proportional to the gate overvoltage, VGS – VTH. A lower gate voltage increases the resistance and hence increases the negative feedback in the oscillator. A precision active rectifier measures the amplitude of the oscillation and drives the gate of the MOSFET to reach the desired equilibrium output of the oscillator.

Here is the block diagram of the system. U1 is the Wien bridge oscillator. U2 filters the output of the rectifier and compares that value to a reference voltage that is the level of output you want from the oscillator. You will use a MOSFET from an ALD1106 quad matched MOSFET IC. R3 and R4 compensate the non-linearity of the MOSFET as a voltage variable resistor so that it does not introduce significant distortion to the output.



There is an example of how to build a precision rectifier in the handout on opamp applications that I gave in class. (It is also on the class website.) That rectifier circuit has two stages, one that produces a half-wave rectified output and a second that sums the half wave with the original signal to give a current proportional to the instantaneous absolute magnitude of its input. One can combine the integrator U2 with that summing circuit. The overall rectifier-integrator scheme then looks like this circuit with $V_{SETPOINT}$ being the reference voltage that controls the amplitude of the oscillator output. Here v_{IN} is the output of the Wien bridge oscillator and v_{OUT} is the signal to the gate of the MOSFET in the bridge itself.



A long-channel MOSFT operated with $V_{DS} << V_{GS} - V_{TH}$ has the drain current

$$I_D = K_N \left(V_{GS} - V_{TH} - \tfrac{1}{2}V_{DS}\right)V_{DS}$$

If you set R3 and R4 so that $V_{GS} = \tfrac{1}{2}\left(V_{DS} + V_{CTL}\right)$ then the MOSFET drain-source terminals become a resistor with value $r_{DS} = \dfrac{2}{K_N\left(V_{CTL} - 2V_{TH}\right)}$. The datasheet for the ALD1106 is on the class website and is available by Google. **NOTE: for the ALD1106 to operate properly, you HAVE TO CONNECT ITS SUBSTRATE PIN (Pin 4) TO GROUND.**

The datasheet says that the typical value of V_{TH} is 0.7 volts and it gives a graph of the drain-source resistance at low VDS that can be used for your design. To keep distortion low, make r_{ds} between 3 and 5 % of the total value of R1. As a second rule of thumb, keep the total DC current from the V_{CTL} control voltage below 10 microamperes.

Analysis Discussion: Intuitively one knows the circuit will oscillate when there is a single frequency such that a signal at that frequency coming out of the opamp will return to the input and will again go through the amplifier exactly in phase with the original output but it will be bigger because of the overall loop gain. This is what happens when a microphone picks up a signal from a speaker to which it is connected and the system squeals from the feedback. Unfortunately this intuitive idea does not help much in quantifying the action. For example, it gives little insight into what the frequency of oscillation will be, how the circuit will start up or

how phase shift in U1 might affect startup or oscillation frequency. For any such questions, a more sophisticated analysis is necessary.

One way to analyze the circuit is to break the connection from the output of U1 to the Wien bridge and replace the Wien bridge drive with an input signal as shown below. Then one calculates the transfer function and converts that function into a standard linear differential equation. Replace the input voltage with the output voltage and the LDE gives you the condition for oscillating at all, the time response on startup, the frequency of oscillation, etc.

To simplify an initial analysis, assume that the opamp has a finite gain, A_O, but no phase shift. Define the voltage divider constant for R1 and R2 as $\beta \equiv \frac{R1}{R1+R2}$ and define the product RC as $\tau = RC$. With those definitions the transfer function of this circuit becomes:

$$v_{out} = A_O\left[\frac{s\tau}{s^2\tau^2+3s\tau+1} - \beta\right]v_{in}$$

With some manipulation this becomes:

$$\left(1+\beta A_O\right)\left(s^2\tau^2+3s\tau+1\right)v_{out} = A_O s\tau v_{in}$$

We were able to write this algebraic equation because we assumed implicitly that the voltages were linear combination of complex exponentials. In that case the derivative operator became the algebraic operator *s*. Now reverse that substitution to form a differential equation while at the same time assuming that $\beta A_O \gg 1$. Then we get

$$\beta\left(\tau^2\frac{d^2v_{out}}{dt^2}+3\tau\frac{dv_{out}}{dt}+v_{out}\right)-\tau\frac{dv_{in}}{dt}=0$$

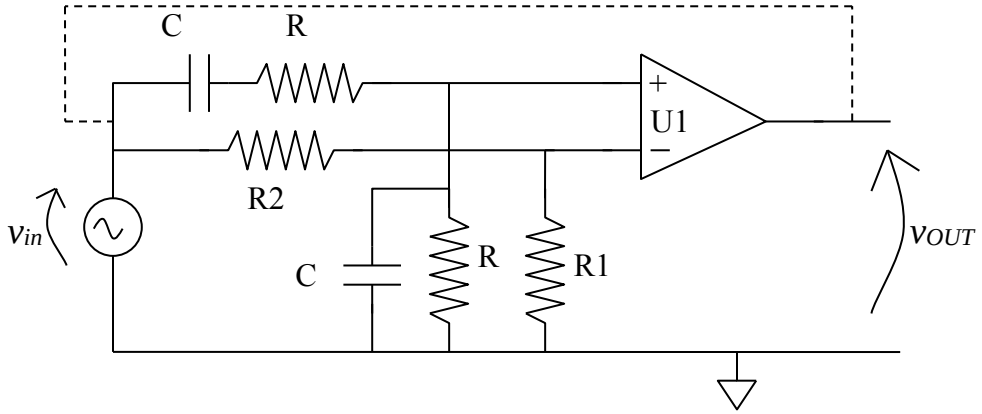
If at some moment when the two voltages are zero, we replace the input source with a connection to the output of U1, we get the differential equation that describes the closed loop response.

$$\tau^2\frac{d^2v}{dt^2}+\tau\left(3-\frac{1}{\beta}\right)\frac{dv}{dt}+v=0$$

This is the well-known equation for damped or underdamped sine waves. Whether the amplitude grows or decays depends on the sign of the first derivative. If that is negative, *i.e.* $\beta < \frac{1}{3}$, then the sinusoid will grow proportionally to $\exp\left(\frac{(1-3\beta)}{2\beta\tau}t\right)$. The real system will have a little noise in the amplifier that will excite some combination of the solutions to this equation. If β is adjusted to exactly 1/3, which is the function of the rectifier-integrator circuitry, then the amplitude of the sinewave will be constant and its frequency will be $f_{osc} = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC}$.

It is straightforward to show by the same procedure that the effect of an opamp with a single dominant pole is to change both the condition for oscillation and the frequency of oscillation by small amounts. If f_{GBW} is the gain-bandwidth product of the amplifier, then

the condition for oscillation is $\frac{1}{\beta} \geq 3 + \frac{6 f_{osc}}{f_{GBW}}$ and the frequency of oscillation becomes $f_{osc} = \frac{1}{2\pi\tau\sqrt{1 + \frac{6 f_{osc}}{f_{gbw}}}}$. (As a reminder, the gain-bandwidth product of the LF353 is 4 MHz.)



The lab report should include:

1. Your calculation of component values
2. Full schematic; xDxDesigner preferred but not mandatory.
3. Derivation of the relation between the $V_{SETPOINT}$ at the control integrator and the amplitude of the output of U1.
4. Measurement of the frequency and amplitude of the oscillator and the values of V_{CTL} and $V_{SETPOINT}$.
5. Magic number for lab 9.

APPENDIX: DEVICE DATA SHEETS

1N4154
2N2222A
2N3440
2N3904
ALD1106
ALD1107
CA3083
CA3096
IRF610PbF
LF353N

Note: these are abbreviated datasheets. Complete datasheets are on the class website.

FAIRCHILD SEMICONDUCTOR™

1N4154

DISCRETE POWER AND SIGNAL TECHNOLOGIES

General Description:

The high breakdown voltage, fast switching speed and high forward conductance of this diode packaged in a DO-35 miniature Glass Axial leaded package makes it desirable also as a general purpose diode.

High Conductance Fast Diode

Features:

- 500 milliwatt Power Dissipation package.
- Fast Switching Speed,
- Typical capacitance less than 1.0 picofarad.

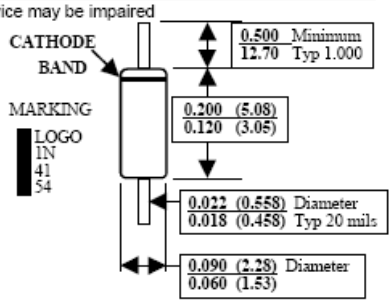
Ordering:

- 13 inch reel, 50 mm (T50R) & 26 mm (T26R) Tape; 10,000 units per reel.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

Sym	Parameter	Value	Units
T_{stg}	Storage Temperature	-65 to +200	°C
T_J	Operating Junction Temperature	175	°C
P_D	Total Power Dissipation at T_A = 25°C	500	mW
	Linear Derating Factor from T_A = 25°C	3.33	mW/°C
$R_{\Theta JA}$	Thermal Resistance Junction-to-Ambient	300	°C/W
W_{IV}	Working Inverse Voltage	35	V
I_O	Average Rectified Current	100	mA
I_F	DC Forward Current (IF)	300	mA
i_f	Recurrent Peak Forward Current (IF)	400	mA
$i_{F(surge)}$	Peak Forward Surge Current (IFSM) Pulse Width = 1.0 second	1.0	Amp
	Pulse Width = 1.0 microsecond	4.0	Amp

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired



Electrical Characteristics TA = 25°C unless otherwise noted

SYM	CHARACTERISTICS	MIN	MAX	UNITS	TEST CONDITIONS
B_V	Breakdown Voltage	35		V	I_R = 5.0 uA
I_R	Reverse Leakage		100	nA	V_R = 25 V
			100	uA	V_R = 25 V, T_A = 150°C
V_F	Forward Voltage		1.0	V	I_F = 30 mA
C_T	Capacitance		4.0	pF	V_R = 0.0 V, f = 1.0 MHz
T_{RR}	Reverse Recovery Time		4.0	ns	I_F = 10 mA V_R = 6.0 V I_{RR} = 1.0 mA, R_L = 100 ohms

Revision A - September 21, 1998

NPN switching transistors 2N2222; 2N2222A

FEATURES

- High current (max. 800 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

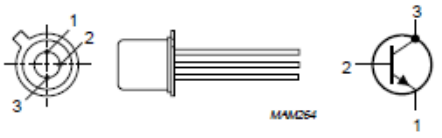


Fig.1 Simplified outline (TO-18) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V	75	–	
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = −15 mA	–	250	ns

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current				
	2N2222	I_E = 0; V_{CB} = 50 V	–	10	nA
		I_E = 0; V_{CB} = 50 V; T_{amb} = 150 °C	–	10	µA
I_{CBO}	collector cut-off current				
	2N2222A	I_E = 0; V_{CB} = 60 V	–	10	nA
		I_E = 0; V_{CB} = 60 V; T_{amb} = 150 °C	–	10	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 3 V	–	10	nA
h_{FE}	DC current gain	I_C = 0.1 mA; V_{CE} = 10 V	35	–	
		I_C = 1 mA; V_{CE} = 10 V	50	–	
		I_C = 10 mA; V_{CE} = 10 V	75	–	
		I_C = 150 mA; V_{CE} = 1 V; note 1	50	–	
		I_C = 150 mA; V_{CE} = 10 V; note 1	100	300	
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V; T_{amb} = −55 °C			
	2N2222A		35	–	
h_{FE}	DC current gain	I_C = 500 mA; V_{CE} = 10 V; note 1			
	2N2222		30	–	
	2N2222A		40	–	
V_{CEsat}	collector-emitter saturation voltage				
	2N2222	I_C = 150 mA; I_B = 15 mA; note 1	–	400	mV
		I_C = 500 mA; I_B = 50 mA; note 1	–	1.6	V
V_{CEsat}	collector-emitter saturation voltage				
	2N2222A	I_C = 150 mA; I_B = 15 mA; note 1	–	300	mV
		I_C = 500 mA; I_B = 50 mA; note 1	–	1	V
V_{BEsat}	base-emitter saturation voltage				
	2N2222	I_C = 150 mA; I_B = 15 mA; note 1	–	1.3	V
		I_C = 500 mA; I_B = 50 mA; note 1	–	2.6	V
V_{BEsat}	base-emitter saturation voltage				
	2N2222A	I_C = 150 mA; I_B = 15 mA; note 1	0.6	1.2	V
		I_C = 500 mA; I_B = 50 mA; note 1	–	2	V
C_c	collector capacitance	I_E = i_e = 0; V_{CB} = 10 V; f = 1 MHz	–	8	pF
C_e	emitter capacitance	I_C = i_c = 0; V_{EB} = 500 mV; f = 1 MHz			
	2N2222A		–	25	pF
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
F	noise figure	I_C = 200 µA; V_{CE} = 5 V; R_S = 2 kΩ;			
	2N2222A	f = 1 kHz; B = 200 Hz	–	4	dB

2N3439
2N3440

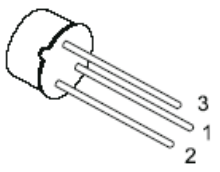
SILICON NPN TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES
- NPN TRANSISTOR

DESCRIPTION

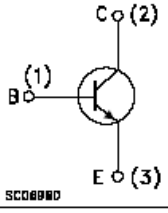
The 2N3439 and 2N3440 are silicon epitaxial planar NPN transistors in jedec TO-39 metal case designed for use in consumer and industrial line-operated applications.

These devices are particularly suited as drivers in high-voltage low current inverters, switching and series regulators.



TO-39

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		2N3439	2N3440	
V_{CBO}	Collector-Base Voltage (I_E = 0)	450	300	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	350	250	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	7		V
I_C	Collector Current	1		A
I_B	Base Current	0.5		A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	10		W
P_{tot}	Total Dissipation at $T_{amb} \leq 50$ °C	1		W
T_{stg}	Storage Temperature	-65 to 200		°C
T_j	Max. Operating Junction Temperature	200		°C

2N3903, 2N3904

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 2) (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	–	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{BL}	–	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{CEX}	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	
Collector–Emitter Saturation Voltage (Note 2)		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc			–	0.3	
Base–Emitter Saturation Voltage (Note 2)		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903		250	–	
	2N3904		300	–	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		1.0	8.0	
	2N3904		1.0	10	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		0.1	5.0	
	2N3904		0.5	8.0	
Small–Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		50	200	
	2N3904		100	400	
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903		–	6.0	
	2N3904		–	5.0	
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc,	t_d	–	35	ns
Rise Time	I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	t_r	–	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, 2N3903	t_s	–	175	ns
	I_{B1} = I_{B2} = 1.0 mAdc) 2N3904		–	200	
Fall Time		t_f	–	50	ns

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

ADVANCED LINEAR DEVICES, INC.

ALD1106/ALD1116

QUAD/DUAL N-CHANNEL MATCHED PAIR MOSFET ARRAY

GENERAL DESCRIPTION

The ALD1106/ALD1116 are monolithic quad/dual N-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1106/ALD1116 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. The ALD1106/ALD1116 are building blocks for differential amplifier input stages, transmission gates, and multiplexer applications, current sources and many precision analog circuits.

FEATURES

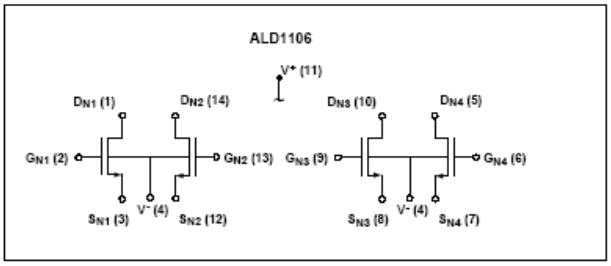
- Low threshold voltage of 0.7V
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- $10^{14}\Omega$ typical
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 109
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1116 DA	ALD1116 PA	ALD1116 SA
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1106 DB	ALD1106 PB	ALD1106 SB

* Contact factory for industrial temperature range.

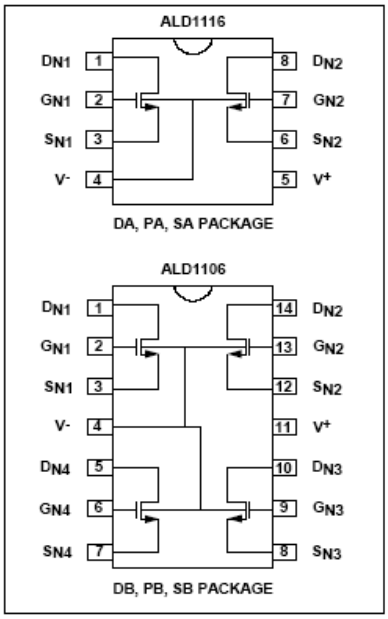
BLOCK DIAGRAM



APPLICATIONS

- Precision current mirrors
- Precision current sources
- Voltage choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog signal processing

PIN CONFIGURATION



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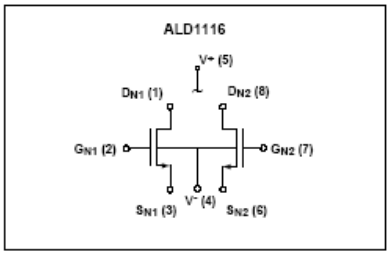

ADVANCED LINEAR DEVICES, INC.

ALD1107/ALD1117

QUAD/DUAL P-CHANNEL MATCHED PAIR MOSFET ARRAY

GENERAL DESCRIPTION

The ALD1107/ALD1117 are monolithic quad/dual P-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1107/ALD1117 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for precision analog switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC operating environment. The ALD1107/ALD1117 are builiding blocks for differential amplifier input stages, transmission gates, multiplexer applications, current sources, current mirrors and other precision analog circuits.

FEATURES

- Low threshold voltage of -0.7
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- $10^{14}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10^9
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1117 DA	ALD1117PA	ALD1117 SA
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1107 DB	ALD1107 PB	ALD1107 SB

* Contact factory for industrial temperature range.

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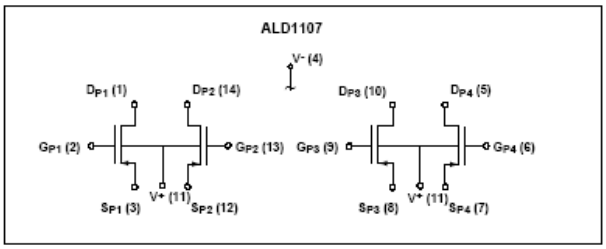
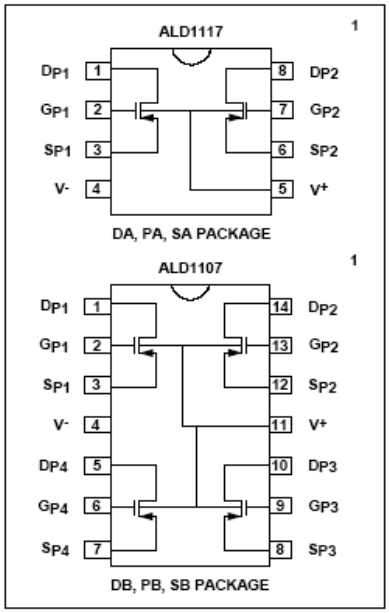


APPLICATIONS

- Precision current sources
- Precision current mirrors
- Voltage Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Precision analog signal processing

PIN CONFIGURATION



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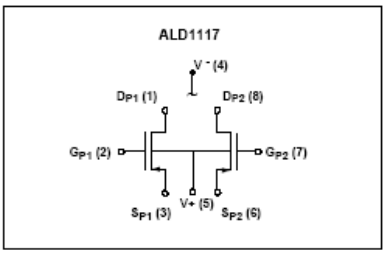


General Purpose High Current NPN Transistor Array

The CA3083 is a versatile array of five high current (to 100mA) NPN transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CA3083	CA3083	-55 to 125	16 Ld PDIP	E16.3
CA3083Z (Note)	CA3083Z	-55 to 125	16 Ld PDIP* (Pb-free)	E16.3
CA3083M96	3083	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3083MZ (Note)	3083MZ	-55 to 125	16 Ld SOIC (Pb-Free)	M16.15
CA3083MZ96 (Note)	3083MZ	-55 to 125	16 Ld SOIC (Pb-Free) Tape and Reel	M16.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

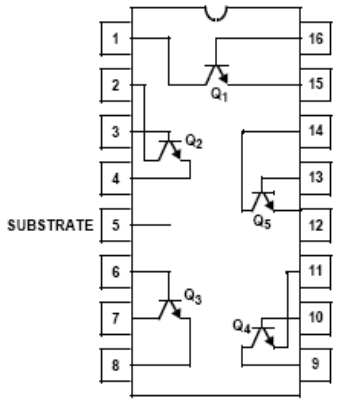
- High I_C . . . . . 100mA (Max)
- Low $V_{CE\ sat}$ (at 50mA) . . . . . 0.7V (Max)
- Matched Pair (Q_1 and Q_2)
  - V_{IO} (V_{BE} Match) . . . . . ±5mV (Max)
  - I_{IO} (at 1mA) . . . . . 2.5µA (Max)
- 5 Independent Transistors Plus Separate Substrate Connection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing
- See Application Note AN5296 "Applications of the CA3018 Circuit Transistor Array" for Suggested Applications

Pinout

CA3083
(PDIP, SOIC)
TOP VIEW



NOTES:

1. The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate Terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications For Equipment Design, $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu A$, $I_E = 0$		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\mu A$, $I_B = 0$, $I_E = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu A$, $I_C = 0$		5	6.9	-	V
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$		-	-	10	µA
Collector-Cutoff-Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$		-	-	1	µA
DC Forward-Current Transfer Ratio (Note 3) (Figure 1)	h_{FE}	$V_{CE} = 3V$	$I_C = 10mA$	40	76	-	
			$I_C = 50mA$	40	75	-	
Base-to-Emitter Voltage (Figure 2)	V_{BE}	$V_{CE} = 3V$, $I_C = 10mA$		0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage (Figures 3, 4)	$V_{CE\ SAT}$	$I_C = 50mA$, $I_B = 5mA$		-	0.40	0.70	V
Gain Bandwidth Product	f_T	$V_{CE} = 3V$, $I_C = 10mA$		-	450	-	MHz
FOR TRANSISTORS Q_1 AND Q_2 (As a Differential Amplifier)							
Absolute Input Offset Voltage (Figure 6)	$\lvert V_{IO} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$		-	1.2	5	mV
Absolute Input Offset Current (Figure 7)	$\lvert I_{IO} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$		-	0.7	2.5	µA

NOTE:

3. Actual forcing current is via the emitter for this test.

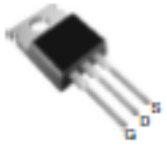
IRF610, SiHF610

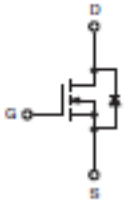
Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1.5
Q_g (Max.) (nC)	8.2	
Q_{gs} (nC)	1.8	
Q_{gd} (nC)	4.5	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF610PbF
	SiHF610-E3
SnPb	IRF610
	SiHF610

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	3.3	A
		T_C = 100 °C		2.1	
Pulsed Drain Current[a]			I_{DM}	10	
Linear Derating Factor				0.29	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	64	mJ
Repetitive Avalanche Current[a]			I_{AR}	3.3	A
Repetitive Avalanche Energy[a]			E_{AR}	3.6	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	36	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 8.8 mH, R_G = 25 Ω, I_{AS} = 3.3 A (see fig. 12).
c. I_{SD} ≤ 3.3 A, dI/dt ≤ 70 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

National Semiconductor

December 2003

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

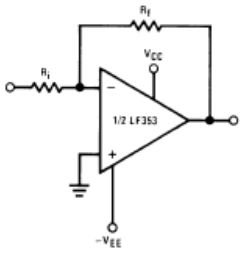
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage:	10 mV
■ Low input bias current:	50pA
■ Low input noise voltage:	25 nV/√Hz
■ Low input noise current:	0.01 pA/√Hz
■ Wide gain bandwidth:	4 MHz
■ High slew rate:	13 V/μs
■ Low supply current:	3.6 mA
■ High input impedance:	$10^{12}\Omega$
■ Low total harmonic distortion :	≤0.02%
■ Low 1/f noise corner:	50 Hz
■ Fast settling time to 0.01%:	2 μs

Typical Connection



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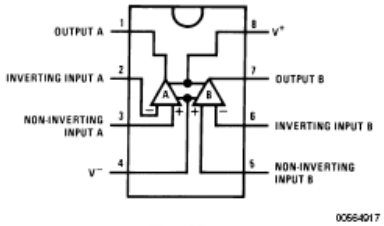
Connection Diagram

Dual-In-Line Package



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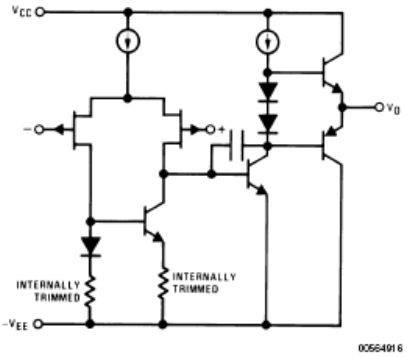
Top View
Order Number LF353M, LF353MX or LF353N
See NS Package Number M08A or N08E

Simplified Schematic

1/2 Dual



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BI-FET II™ is a trademark of National Semiconductor Corporation.

 DS005649 www.national.com

LF353

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1000V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 5, 6)		25	100	pA
		$T_j \leq$70°C			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 5, 6)		50	200	pA
		$T_j \leq$70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω,		16		nV/$\sqrt{Hz}$
		f=1000 Hz				
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/$\sqrt{Hz}$