Hints and Comments - 2011

1. **Sources of Information:** The definitive data on the characteristics of any device is its data sheet. Do not rely on random pull-ups from Wikipedia or the like. There is a packet of data sheets for all the devices in your kit on the class web site as a zip file you can download. Do it and use them!

2. **Displaying results for Lab 1:** We have programmed a few CPLD boards to use as displays for Lab 1 on error correction. You connect a display board to your protoboard with the ribbon cable in your kit. The pinout that is listed for those boards here refers to the 24-pin DIP plug on the protoboard end of that cable. Pin numbers are stamped on the top of the DIP plug. The pin assignments for the display are:

Pin Function
24 VDD = + 5 volts (be sure this connection is made before turning on the power.)
10 GND = 0 volts
23 Q3 - MSB of hex display (Use pullup resistors for high – **do NOT connect directly to VDD**.)
22 Q2
21 Q1
20 Q0 - LSB of hex display
11 Cathode of display - MUST CONNECT TO GND

The XC9572XL's are easily destroyed, so please be careful. Read the lab manual (sec. 10) on how to handle these boards. Do NOT connect or disconnect the display board with the power on!! I have posted copies of the precautions in the lab too.

3. **Capturing Oscilloscope Data for Labs 2 and 6:** There is now one new scope in the lab and two more on order. These have the ability to capture screen data as any of sever file formats on a USB flash drive. To use this capability after you have the measurement displayed on the screen:

    - Insert a flash drive into the USB connector at the bottom center of the front panel.
    - Hit the File/Save button at the bottom of the "Measure" group of controls.
    - The screen will show new labels above the buttons at the bottom of the screen. Hit the "Save" button that will open some additional softbutton choices.
        - Select the "CSV" (Comma Separated Values) data format
        - Select "Filename" and enter the name you want to use to store the image.
        - Hit "Save" to store the screen data to the drive.

4. **NE555 Used as an Oscillator:** Look at its data sheet! It has the circuit for the free-running oscillator and a graph that helps picking component values. In the table of Electrical Characteristics (pg. 4) are a number of guidelines for how to use it. One thing is that the two resistors are each shown as always being in the range of 1K to 100K for operation with limited drift or temperature effects. The available discharge current for +5 volt operation is suggested as 4.5 mA in the entry under device saturation voltage. This sets a limit of 1K for the resistor R1 in the schematic of Figure 15. Do not make R1 smaller than 1 K or the circuit may not work. Making it 2 K or higher is probably better. While the total resistance of R1 + R2 can be as high as 3.5 Meg (Note 2 Table 3), that is not recommended for stable accurate operation. Keep it down to under six hundred K ohms.

5. **Preparing Files for Programming a CPLD or FPGA:** When you have completed making your .jed file and before you try to download, it is a good idea to check that you got the pinout for the device right. You do that when the Project Navigator has completed its work. In the "Hierarchy" tab of the left pane, click on your Verilog file to select it. In the "Design" tab, expand the "User Constraints" branch and click on "Floorplan IO". This will open a tool with a table of the pin names and numbers. Recheck them.

6. **Xilinx Software Access:** There is a minor change to the instructions in the first version of the lab manual regarding how to set up for and start the Xilinx programming software. I have fixed the on-line version of the manual. The basics are:

    - Create a U:\Xilinx_Projects directory to keep all Xilinx related files

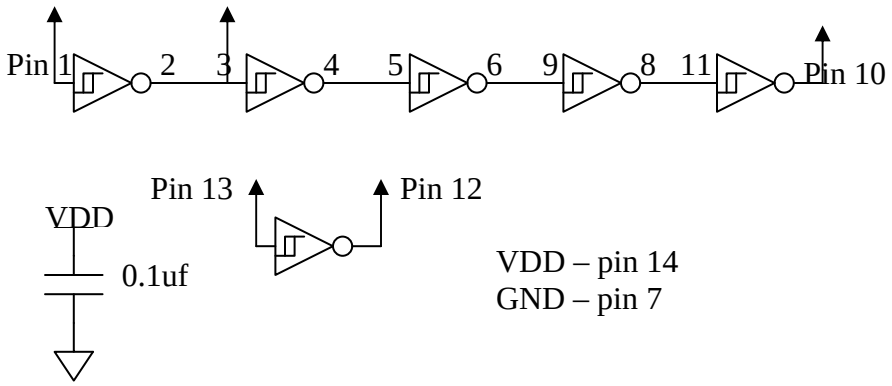
    - Start the software from the Win 7 start menu as: "All Programs/Xilinx ISE…./ISE Design Tools/62-Bit Project Navigator".

7. **CPLD-Board Connections:** Getting the correct connection from a signal in the CPLD to its terminus on your breadboard is tricky. There are three different numbers for pins on the same signal net depending on whether the connection is at the CPLD, the ribbon cable connector or the DIP plug on your breadboard. To make the situation even more complicated, there is the additional consideration that the plug for the logic analyzer on the CPLD board is pre-connected to a subset of the nets. (If you use the logic analyzer on a bus, you want those connections to be ordered so the values on the bus show correctly in hexadecimal notation.) There is a table correlating these sets of numbers in the lab manual section 10, table 10.1 on page 107. The same table is posted in the lab. Section 10 has other information on downloading and on the care and feeding of the CPLD itself.

8. **Required Schematics:** Please note that as the lab manual states, the required schematic must be done in DxDesigner and must include all the incidental com-

ponents and annotation laid out in section 9.5. Section 11.3 has instructions on how to use the DxDesigner tool itself. You might find that learning the tool can be helpful in drawing better schematics for all the more complicated labs, particularly 5, 7, 8, and A.

9. **Lab 6: Measuring the properties of the SN74LVC04 as a ring oscillator:** The following is the wiring of the pre-mounted chips in the lab. Use the isolated gate (pins 12 and 13) with pin 1 grounded for the single-gate measurements. Wire together the ends of the string to make the oscillator. Lines terminating in arrowheads are connections available for your protoboards.



Prewired SN74LVC04A Connections: The bypass capacitor is on the socket and arrowheads mark available wires for your connections.

10. **Turning on the FPGA test stations:** There will be four setups for the FPGA labs B through D. Please do not move the setups. Each station has a Spartan 3E evaluation board from Digilent Inc. and a custom pcb that I built. There needs to be both a power supply connection and a USB connection to each unit. The eval board has a power switch that should be left turned off between uses and turned on before you download your bit-file. The switch is in the upper left corner of the board near where the power cable attaches to the board.