BROWN
School of Engineering

DIGITAL ELECTRONICS SYSTEM DESIGN

FALL 2019

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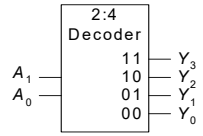
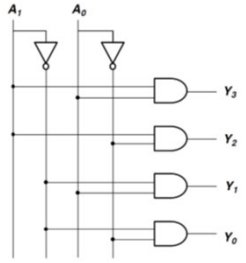
LECTURE 6: COMBINATIONAL LOGIC BLOCKS

DECODER: DEFINITION

- N inputs, 2^N outputs
- One-hot outputs: only one output HIGH at once



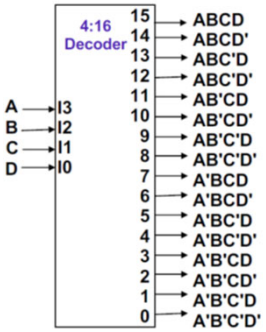
A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



LOGIC FUNCTIONS USING DECODERS

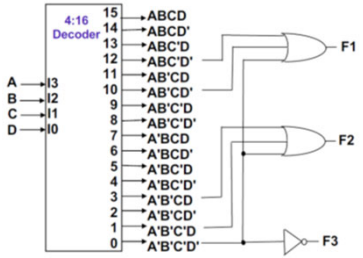
- N:2^N decoder can be used to implement any function of N variables

  How?
  - Connect variables to inputs
  - Represent function using minterm canonical form

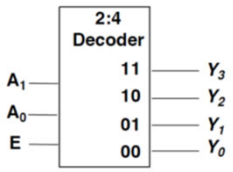


LOGIC FUNCTIONS USING DECODERS

- F1 = A'B'C'D' + AB'CD' + ABC'D'
- F2 = A'B'C' + A'B'CD
- F3 = A+B+C+D



DECODER WITH ENABLE

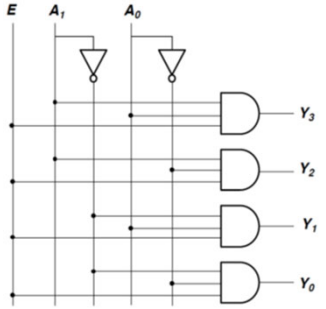


E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

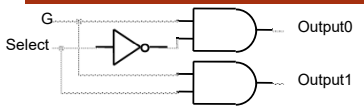
- X: don't care input
- Note that E, A_0, A_1 = 0XX covers 000, 001, 010, 011

DECODER WITH ENABLE

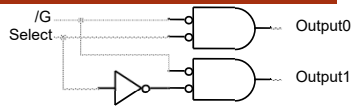
$Y_3 = A_1 \bullet A_0 \bullet E$
$Y_2 = A_1 \bullet A_0' \bullet E$
$Y_1 = A_1' \bullet A_0 \bullet E$
$Y_0 = A_1' \bullet A_0' \bullet E$



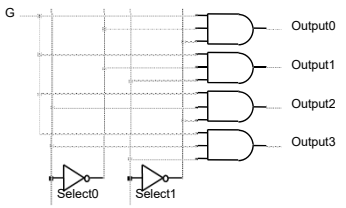
ALTERNATIVE IMPLEMENTATIONS



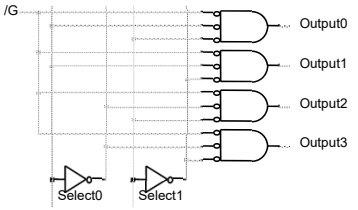
1:2 Decoder, Active High Enable



1:2 Decoder, Active Low Enable



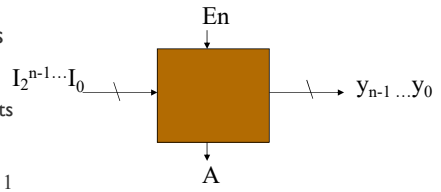
2:4 Decoder, Active High Enable



2:4 Decoder, Active Low Enable

ENCODERS

- Opposite of decoders
- Binary encoders:
  - 2^N inputs and N outputs
- Description:
  - At most one input $I_i = 1$
  - $(y_{n-1}, \ldots, y_0) = 1$ (according to the encoding for *i*) if $I_i = 1$ & En = 1
  - $(y_{n-1}, \ldots, y_0) = 0$ otherwise
  - A=1 if En = 1 & one 1 s.t. $I_i = 1$
  - A=0 otherwise

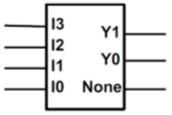


What happens if more than one input $I_i = 1$?

PRIORITY ENCODER

- Highest numbered inputs have priority when multiple inputs are asserted at the same time
- Example: 4-to-2 priority encoder

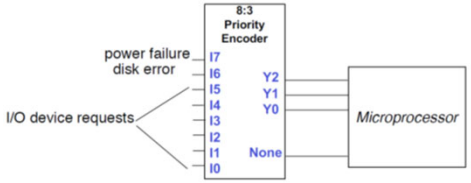
I3	I2	I1	I0	Y1	Y0	None
1	X	X	X	1	1	0
0	1	X	X	1	0	0
0	0	1	X	0	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	1



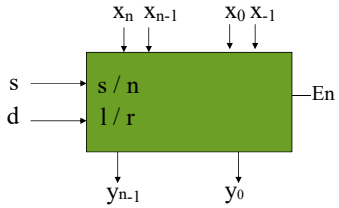
Y1=I3+I3'I2=I3+I2
Y0=I3+I3'I2'I1=I3+I2'I1
None=I3'I2'I1'I0'

EXAMPLE: MICROPROCESOR INTERRUPTS

- In order for devices to get service, they interrupt the microprocessor
- Most important requests are given priority

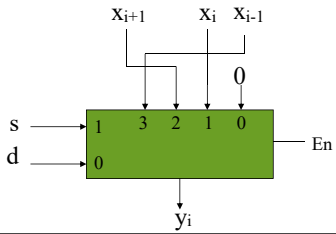


SHIFTER



$y_i = x_{i-1}$ if En = 1, s = 1, and d = L
$= x_{i+1}$ if En = 1, s = 1, and d = R
$= x_i$ if En = 1, s = 0
$= 0$ if En = 0

Can be implemented with a mux



COMBINATIONAL BLOCK IN LABS

- Check your kits for chips that implement these combinational blocks
  - Decoder/demultiplexer
  - Multiplexor
  - Shift register
  - Comparator
- Use to your advantage

TRANSISTORS AND BUILDING LOGIC GATES WITH CMOS TRANSISTORS

FEATURE SIZE (Λ VS. ABSOLUTE DIMENSIONS)

- Feature size: minimum distance between source and drain of transistor
- λ rules:
  - If λ=45nm and L = 2λ, feature size 90nm
- Absolute dimensions:
  - e.g, 45nm library
  - Min. feature size = 50nm
    - $L_{effective} \approx 45nm$
- λ rules can be more convenient than absolute dimensions since we don't need to update sizes for new technologies

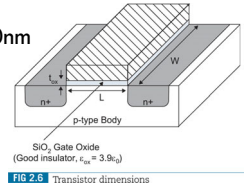
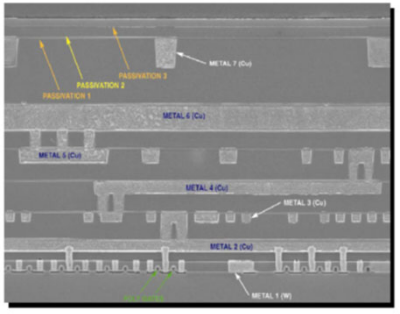
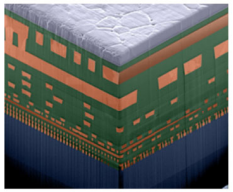


FIG 2.6 Transistor dimensions

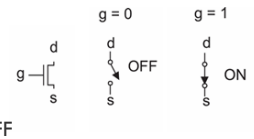
THE INSIDE OF AN INTEGRATED CIRCUIT

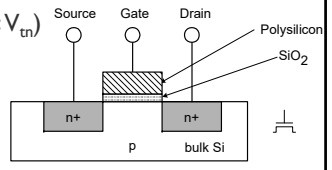




NMOS TRANSISTOR

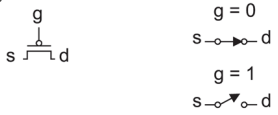
- g=0: gate is at low voltage ($V_{gs}<V_{tn}$)
  - p-type body is at low voltage
  - source and drain junction diodes are OFF
  - transistor is OFF (no current flows)
- g=1: gate is at a high voltage ($V_{gs} \geq V_{tn}$)
  - negative charge attracted to body
  - inverts a channel under gate to n-type
  - transistor is ON (current flows)
  - transistor acts as resistor

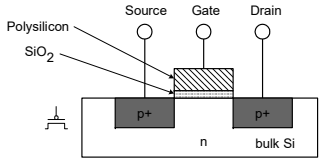




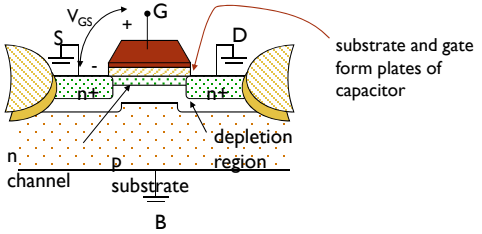
PMOS TRANSISTOR

- g=0: gate is at low voltage ($|V_{gs}| > |V_{tp}|$)
  - positive charge attracted to body
  - inverts channel under gate to p-type
  - transistor is ON (current flows)
- g=1: gate is at a high voltage ($|V_{gs}| \leq |V_{tp}|$)
  - n-type body is at high voltage
  - Source and drain junctions are OFF
  - transistor is OFF (no current flows)





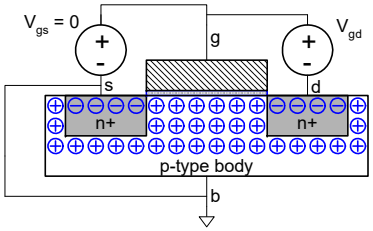
THRESHOLD VOLTAGE CONCEPT



- Depletion region: area devoid of mobile carriers (holes)
- Inversion layer: n-channel region under oxide
- The value of V_{GS} where strong inversion occurs is called the threshold voltage, V_T

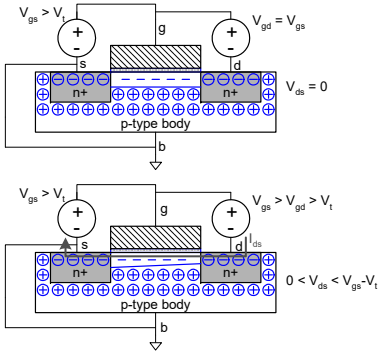
NMOS CUTOFF

- No channel
- $I_{ds} = 0$



NMOS LINEAR

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}, V_{gs}
- Similar to linear resistor



NMOS SATURATION

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source