BROWN
School of Engineering

DIGITAL ELECTRONICS SYSTEM DESIGN

FALL 2019

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SEPTEMBER 25, 2019

LECTURE 7: CMOS TRANSISTORS

CLARIFICATION ABOUT DEADLINES

- Labs are due in groups:
  - Group 1: labs 0-3 due by **Sunday, October 6**
  - Group 2: labs 4-9 due by **Sunday, November 17**
  - Group 3: labs A and B due by **Friday, December 6**
- The last week before the final exam can be used as a grace period:
  - *Up to one additional lab from each group can be checked off between Dec. 7-13*
  - Labs may be checked off earlier, but if completed after the group deadline, they will count as being checked off during exam week
  - *Only one lab a day credited in exam week*
- Labs C and D may be checked off up until **Thursday, Dec. 13**
- **Plan ahead! Don't wait until exam week to finish all your labs!**

STORAGE SPACE IN LAB

- Unfortunately, there is no secure storage space available in B&H 196
- However, we do have open shelves and drawers in the back end of the room
- You are free to leave your kits there, but it is at your own risk
  - Put all parts in an enclosed bin (e.g., Tupperware with lid)
  - Write your name clearly on bin
  - Do no leave valuables in the bin

IBM STUDENT DESIGN WORKSHOP

WHEN: October 12, 2019

TIME: 9:00am-5:00pm

- **Open to all students, but geared mostly toward engineering students in their junior year.**
- **IBM facilitators will guide students through design for tackling a current pressing problem (e.g., within the or for a course)**

- Advanced registration is required. Please reserve your spot by *Friday, Sept. 27* at https://forms.gle/ynUg4rixsJbTy8Qj6
- Some intial problem evaluation is required before the workshop takes place

WHAT IS DESIGN THINKING?

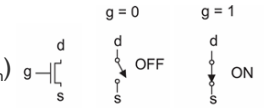
- Design thinking is a methodology for creative problem solving that enables collaboration across disciplines.
- It can be applied to many different kinds of problems
- It can help many different people (including engineers) think about problem solving in new ways

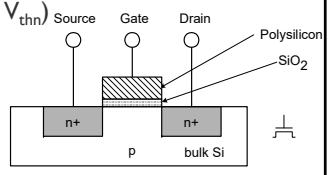
STUDENT WORKSHOP BRIEF

- Learn how to use an enhanced form of design thinking to creatively solve problems collaboratively with fellow students.
- We'll tackle a real-world problem, and bring potential solutions from problem discovery through to prototyping using an agile and user-centered approach.
- Join us and learn a set of methods that you can use to solve almost any kind of design challenge.

NMOS TRANSISTOR

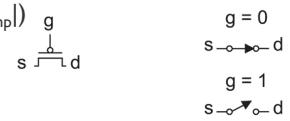
- g=0: gate is at low voltage ($V_{gs}<V_{thn}$)
  - p-type body is at low voltage
  - transistor is OFF (no current flows)
- g=1: gate is at a high voltage ($V_{gs} \geq V_{thn}$)
  - negative charge attracted to body
  - inverts a channel under gate to n-type
  - transistor is ON (current flows)
  - transistor acts as resistor

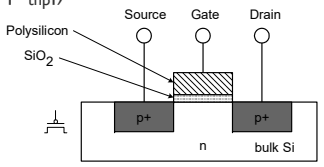




PMOS TRANSISTOR

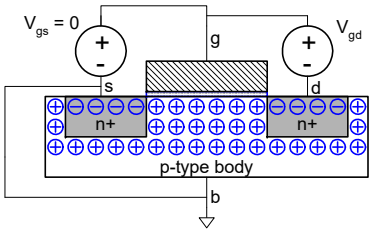
- g=0: gate is at low voltage ($|V_{gs}| > |V_{thp}|$)
  - positive charge attracted to body
  - inverts channel under gate to p-type
  - transistor is ON (current flows)
- g=1: gate is at a high voltage ($|V_{gs}| \leq |V_{thp}|$)
  - n-type body is at high voltage
  - transistor is OFF (no current flows)





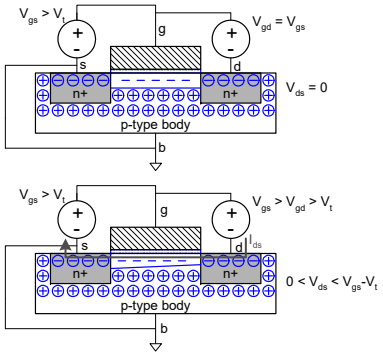
NMOS CUTOFF

- No channel
- $I_{ds} = 0$



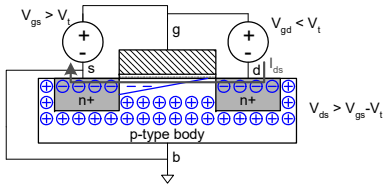
NMOS LINEAR

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds} and V_{gs}
- Similar to linear resistor



NMOS SATURATION

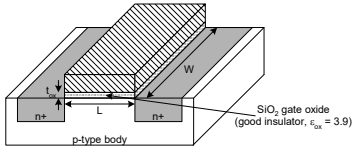
- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source

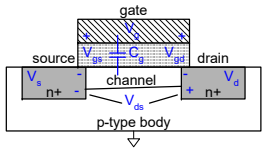


CHANNEL CHARGE

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$
- $V = V_{gc} - V_{th} = (V_{gs} - V_{ds}/2) - V_{th}$

$C_{ox} = \varepsilon_{ox} / t_{ox}$





CROSSING THE CHANNEL

- Now we know
  - How much charge $Q_{channel}$ is in the channel
- How much time, *t*, does it take to cross channel?
  - $t = \frac{L}{v} = \frac{L}{\mu E}$, where μ is mobility, E is electric field across the channel, or $E = V_{ds}/L$
  - So now, $t = \frac{L}{\mu \frac{V_{ds}}{L}} = \frac{L^2}{\mu V_{ds}}$
  - Typical values for mobility:
    - for NFETs: μ_n = 1400 cm²/V-sec
    - for PFETs: μ_p = 450 cm²/V-sec
    - More of a function of doping than technology node size

NMOS LINEAR I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time, *t*, each carrier takes to cross channel

$$I_{ds} = \frac{Q_{channel}}{t}$$
$$= \mu C_{ox} \frac{W}{L}\left(V_{gs} - V_{th} - {}^{V_{ds}}/_{2}\right)V_{ds}$$
$$= \beta\left(V_{gs} - V_{th} - {}^{V_{ds}}/_{2}\right)V_{ds} \qquad \beta = \mu C_{ox}\frac{W}{L}$$

NMOS SATURATION I-V

- When $V_{ds} > V_{dsat}$, where $V_{dsat} = V_{gs} - Vt$
  - channel is no longer inverted around the drain;
  - channel pinches off near drain
- Increasing V_{ds} has no further effect on current

$$I_{ds} = \beta\left(V_{gs} - V_{th} - {}^{V_{ds}}/_{2}\right)V_{ds}$$
$$= \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2$$

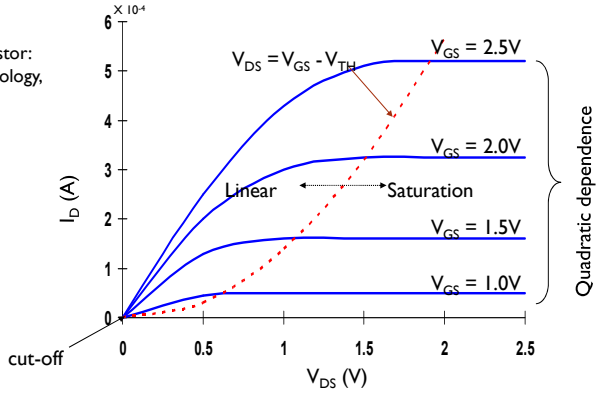
NMOS I-V SUMMARY

- *Shockley* 1st order transistor models

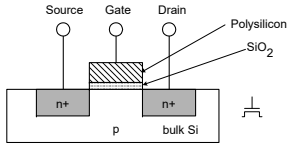
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_{th} \quad \text{cutoff} \\ \beta\left(V_{gs} - V_{th} - {}^{V_{ds}}/_{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

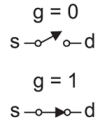
LONG CHANNEL I-V PLOT (NMOS)

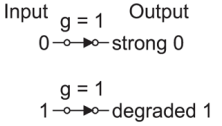
NMOS transistor:
0.25um technology,
L_d = 10um,
W/L = 1.5,
V_{DD} = 2.5V,
V_{TH} = 0.4V



WHY IS NMOS A POOR LOGIC "1" DEVICE?

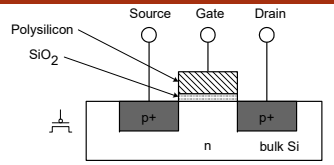


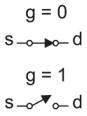


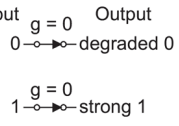


• Why does '1' pass degraded?

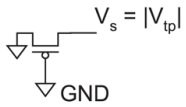
PMOS PASSES LOGIC "0" POORLY



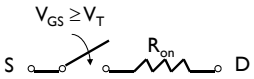


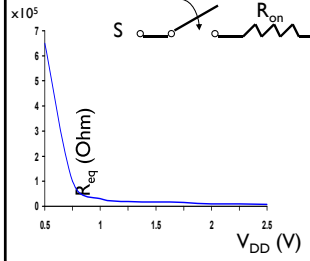


• Why does '0' pass degraded?



TRANSISTOR MODELED AS A SWITCH





(for $V_{GS} = V_{DD}$, $V_{DS} = V_{DD} \rightarrow V_{DD}/2$)

Model as a switch with infinite off resistance and a finite on resistance, R_{on}

- Resistance inversely proportional to W/L (doubling W halves R_{on})
- Once V_{DD} approaches V_T, R_{on} increases dramatically

CMOS INVERTER: STEADY STATE RESPONSE