BROWN
School of Engineering

DIGITAL ELECTRONICS SYSTEM DESIGN

FALL 2019

PROF. IRIS BAHAR

OCTOBER 7, 2019

LECTURE 10: CMOS TRANSIENT BEHAVIOR

SCHEDULE THIS WEEK

- Jiwon Choe will be covering my lecture this Wednesday
  - Introduction to sequential logic
- McKenna Cisler will be holding a ***Verilog tutorial*** this THURSDAY from 5-7pm in the fishbowl
  - He will be swapping his usual Wednesday hours with Andrew

NMOS I-V SUMMARY

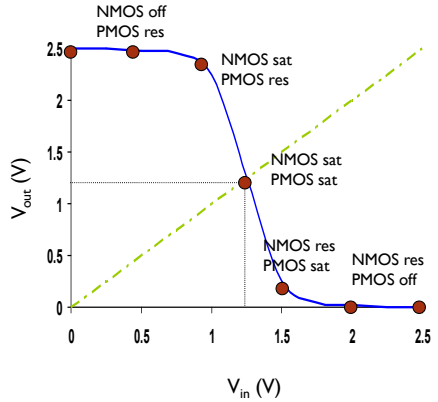
- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_{th} \quad \text{cutoff} \\ \beta\left(V_{gs} - V_{th} - {}^{V_{ds}}/_{2}\right)V_{ds} & V_{gs} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$\beta = \mu C_{ox}\frac{W}{L}$$

where C_{ox} is the capacitance per unit area of SiO_2

CMOS INVERTER VTC



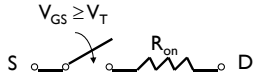
Taking those intersection points from the load curves, we obtain the voltage-transfer characteristic

SWITCHING THRESHOLD

- Define V_M to be the point where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)
- If $V_M = V_{DD}/2$, then this implies *symmetric rise/fall* behavior for the CMOS gate
- Recall at saturation, $I_D = (k'/2)(W/L)\,(V_{GS}-V_{th})^2$,
  - where $k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$
- Setting $I_{Dp} = -I_{Dn}$ $\quad \frac{k'_n}{2}\frac{W_n}{L_n}(V_M - V_{thn})^2 = \frac{k'_p}{2}\frac{W_p}{L_p}(V_M - V_{thp})^2$
- Assuming $V_{thn} = -V_{thp}$ $\quad \frac{W_p/L_p}{W_n/L_n} = \frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p}, \quad$ if $L_p = L_n, \quad W_p = W_n \cdot \frac{\mu_n}{\mu_p}$

MOS STRUCTURE RESISTANCE

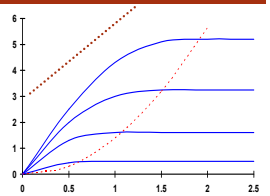
- The simplest model assumes the transistor is a switch with an infinite "off" resistance and a finite "on" resistance R_{on}



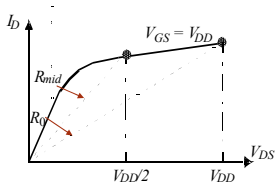
- However R_{on} is nonlinear, time-varying, and dependent on the operation point of the transistor
- *How can we determine an equivalent (constant and linear) resistance to use instead?*

MOS STRUCTURE RESISTANCE

- Approximate R_{on} as the resistance found during linear operation
  - Simple to calculate but limited accuracy
- Instead use the average value of the resistances, R_{eq}, at the end-points of the transition (i.e., V_{DD} and $V_{DD}/2$)



$$R_{eq} \approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$
$$\approx \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}} + \frac{V_{DD}/2}{I_{DSAT}}\right)$$
$$\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}$$



EQUIVALENT MOS STRUCTURE RESISTANCE

$$R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}$$

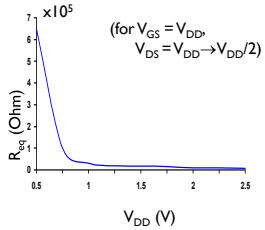
where

$$I_{DSAT} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left((V_{DD} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$$

so,

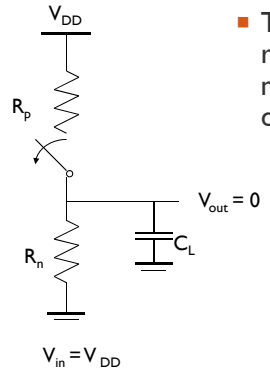
$$R_{eq} = \frac{3}{2\mu C_{ox}}\frac{L}{W}\frac{V_{DD}}{(V_{DD} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}}$$

$$R_{eq_{NMOS}} \propto \frac{L}{\mu_n W}, \qquad R_{eq_{PMOS}} \propto \frac{L}{\mu_p W}$$



R_{eq} is essentially independent of V_{DD} as long as $V_{DD} >> V_T + V_{DSAT}/2$

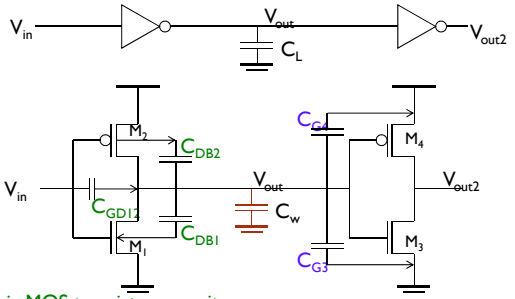
CMOS INVERTER: DYNAMIC BEHAVIOR



- Transient, or dynamic, response determines the maximum speed at which a device can be operated.

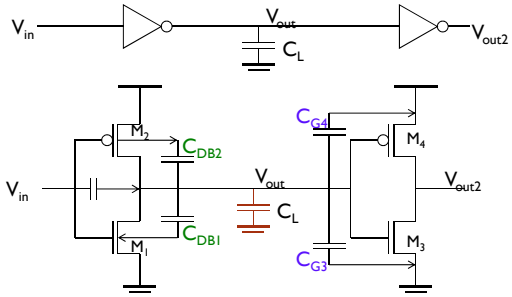
$t_{pHL} = f(R_n, C_L)$

SOURCES OF CAPACITANCE



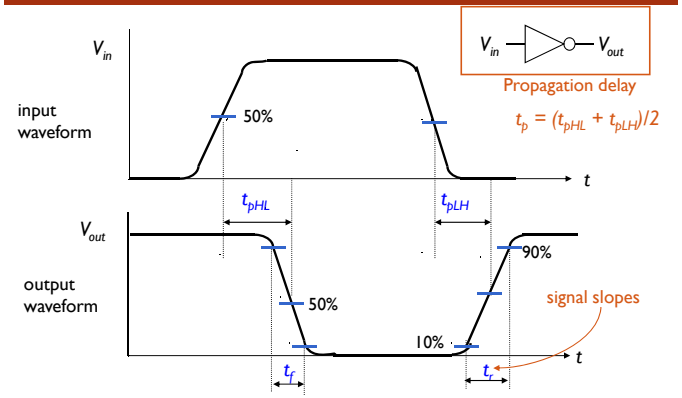
- intrinsic MOS transistor capacitances
- extrinsic MOS transistor (fanout) capacitances
- wiring (interconnect) capacitance

SOURCES OF CAPACITANCE



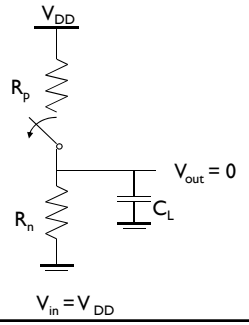
- $C_L \approx C_{DB2}+C_{DB1}+C_{G4}+C_{G3}$

DELAY DEFINITIONS



INVERTER PROPAGATION DELAY

- Propagation delay proportional to time-constant of network formed by ON resistor and the load capacitance.



$t_{pHL} = f(R_n, C_L)$

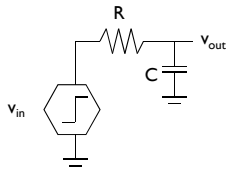
$$R_n = R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}$$

$$C_L = C_{int} + C_{ext}$$

Want to have equal rise/fall delays
make $R_n = R_p$

MODELING PROPAGATION DELAY

- Model circuit as first-order RC network



$v_{out}(t) = (1 - e^{-t/\tau})V_{in}$

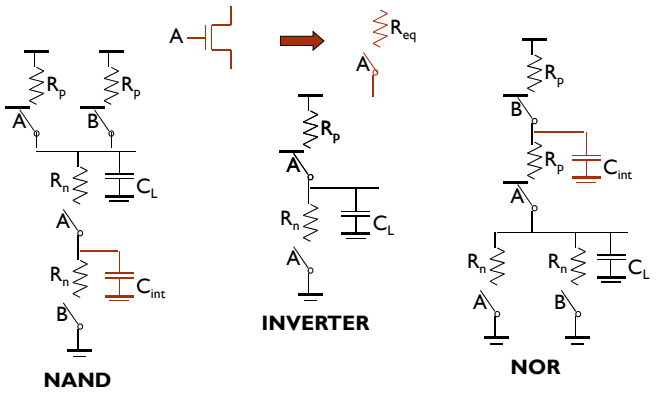
where $\tau = RC$

Time to reach 50% point is
$t = \ln(2)\ \tau = 0.69\ \tau$

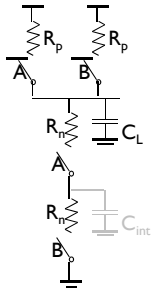
Time to reach 90% point is
$t = \ln(9)\ \tau = 2.2\ \tau$

$$t_p = (t_{pHL} + t_{pLH})/2 = 0.69 C_L (R_n + R_p)/2$$

SWITCH DELAY MODEL



INPUT PATTERN EFFECTS ON DELAY

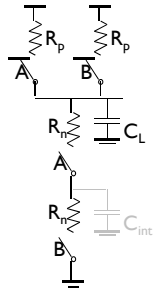


- Delay is dependent on the pattern of inputs
- 1st order approximation of delay:

  $t_p \approx 0.69\ R_{eff}\ C_L$

- R_{eff} depends on the input pattern

INPUT PATTERN EFFECTS ON DELAY

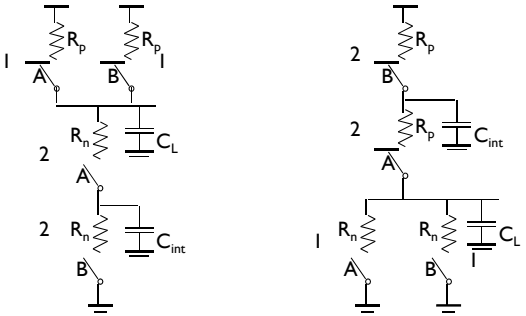


$t_p \approx 0.69\ R_{eff}\ C_L$

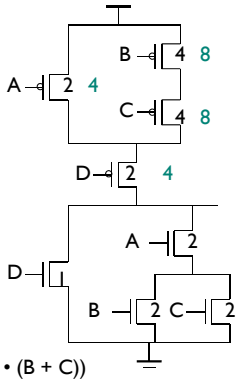
- 0→1 transition on output: 2 possibilities
  - one input goes low: what is R_{eff}?
    - delay is $0.69\ R_p\ C_L$
  - both inputs go low: what is R_{eff}?
    - delay is $0.69\ R_p/2\ C_L$ since 2 p-resistors on in parallel
- 1→0 transition on output: 1 possibility
  - both inputs go high
    - delay is $0.69\ 2R_n\ C_L$
- Adding transistors in series (without sizing) slows down the circuit

TRANSISTOR SIZING

- How should NMOS and PMOS devices be sized relative to an inverter with equal rise/fall times?



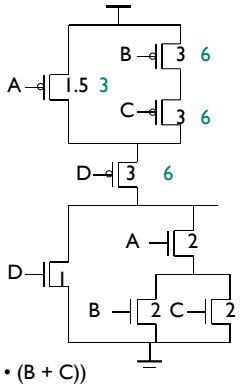
TRANSISTOR SIZING A COMPLEX GATE



OUT = !(D + A • (B + C))

- *Size the shortest path first*
- Numbers in **black** are relative to an inverter
- Numbers in **green** are relative to a minimum width device

TRANSISTOR SIZING A COMPLEX GATE



OUT = !(D + A • (B + C))

- ***Alternate sizing:*** *size the longest path first*