BROWN
School of Engineering

DIGITAL ELECTRONICS SYSTEM DESIGN

FALL 2019

PROF. IRIS BAHAR

OCTOBER 16, 2019

LECTURE 12: CMOS TRANSIENT BEHAVIOR (CONTINUED)

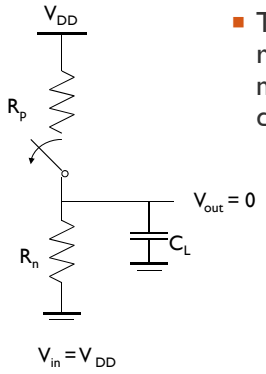
ENGINEERING DESIGN THINKING SPEAKER YVONNE LIN

- Yvonne Lin (AB ENGN '00)
  - Founder, 4B Collective and the Femme Den
  - **Thursday, Oct. 17, 12-1pm**
  - B&H 190
  - Title: Design Engineering: Making Actual Stuff. Taking a product idea from inception to fruition
- Yvonne will speak about her path from Brown to the design world and what it took to get there
- **How design works:** from idea to real life
- **What is design engineering?** How is it different from traditional engineering
- **Putting together a design portfolio** (to land a great job)

HOMEWORK PROBLEMS

- To give you practice on some of the concepts covered in class (and the labs), Jiwon has prepared a practice homework set
- You can find it on the course webpage
  - Look under *Handouts* and "Exam related materials from 2019"
- I am also including homework sets from past years prepared by Prof. Patterson.

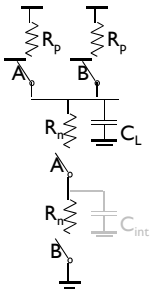
CMOS INVERTER: DYNAMIC BEHAVIOR



- Transient, or dynamic, response determines the maximum speed at which a device can be operated.

$t_{pHL} = f(R_n, C_L)$

INPUT PATTERN EFFECTS ON DELAY



- Delay is dependent on the pattern of inputs
- 1st order approximation of delay:

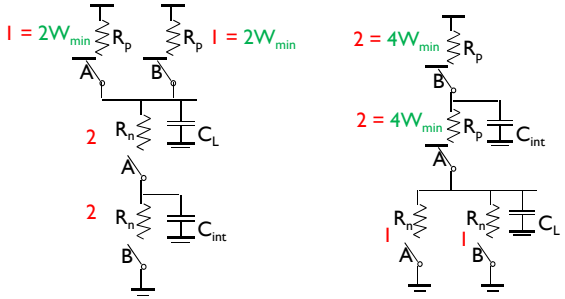
  $t_p \approx 0.69\ R_{eff}\ C_L$

- R_{eff} depends on the input pattern

➡ To get (more equal) rise/fall delays, we need to size transistors not just to compensate for differences in mobility, but also for differences in the topology.

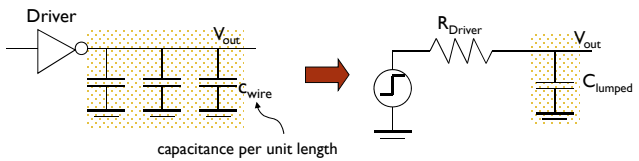
TRANSISTOR SIZING

- How should NMOS and PMOS devices be sized relative to an inverter with equal rise/fall times?
- Size for the worst case series path



WIRE DELAY MODELS

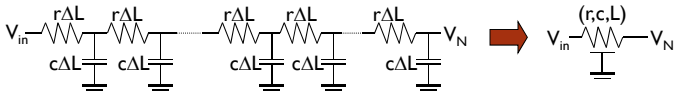
- Lumped C model
  - when only a single parasitic component (C, R, or L) is dominant the different fractions are lumped into a single circuit element



- good for short wires; pessimistic and inaccurate for long wires

WIRE DELAY MODELS, CON'T

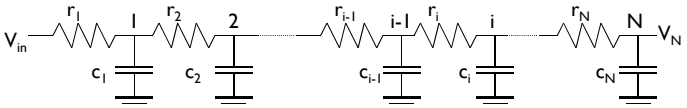
- Lumped RC model
  - total resistance and capacitance are lumped into a single R, C respectively
  - good for short wires; pessimistic and inaccurate for long wires
- Distributed RC model
  - circuit parasitics are distributed along the length, L, of the wire
    - c and r are the capacitance and resistance per unit length



- Delay is determined using the Elmore delay equation:

$$\tau_{Di} = \sum_{k=1}^{N} c_k r_{ik}$$

CHAIN NETWORK ELMORE DELAY

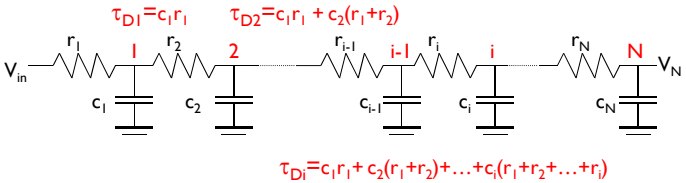


- A typical wire is a chain network with (simplified) Elmore delay of

$$\tau_{DN} = \sum c_i r_{ij} = \sum_{}^{N} c_i \sum_{}^{i} r_j$$

- Where $\sum_{}^{i} r_j = r_1 + r_2 + \ldots + r_i$

CHAIN NETWORK ELMORE DELAY

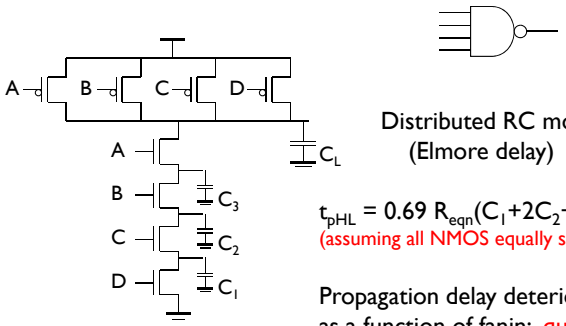


Elmore delay equation $\tau_{DN} = \sum c_i r_{ii} = \sum_{}^{N} c_i \sum_{}^{i} r_j$

If all resistors are equal size,

$$\tau_{Di}=c_1r_{eq}+2c_2r_{eq}+3c_3r_{eq}+\ldots+ic_ir_{eq}$$

FANIN CONSIDERATIONS

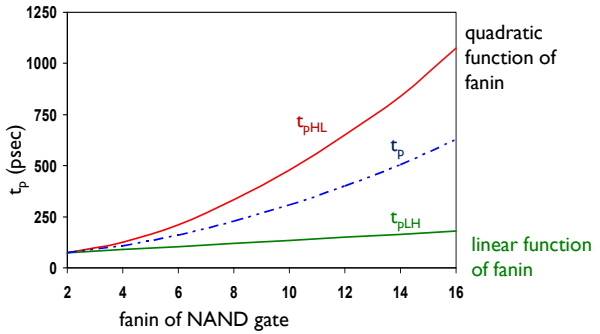


Distributed RC model (Elmore delay)

$t_{pHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$
(assuming all NMOS equally sized)

Propagation delay deteriorates rapidly as a function of fanin: quadratically in the worst case.

T_P AS A FUNCTION OF FANIN

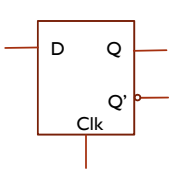


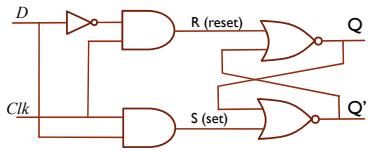
- Gates with a fan-in greater than 4 should be avoided.

SEQUENTIAL LOGIC

D LATCH

Clk	D	R	S	Q	Q'
1	1	0	1	1	0
1	0	1	0	0	1
0	X	0	0	Q_{prev}	Q'_{prev}

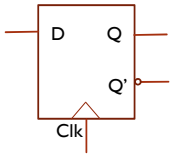




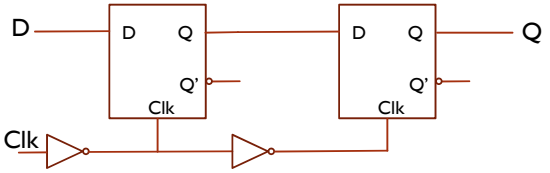
- Circuit guarantees R=S=1 will never occur

FLIP-FLOP

- Flip-flop: Samples input on triggering edge of clock
  - Rising edge → *positive edge-triggered* flip-flop
  - Falling edge → *negative edge-triggered* flip-flop
- D flip-flop: Two D latches back-to-back



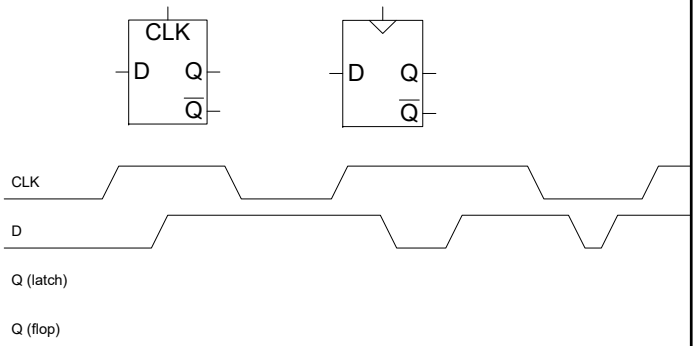
FLIP-FLOP MADE FROM D-LATCHES



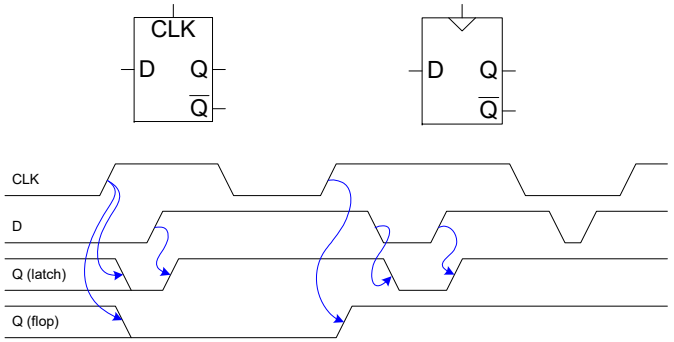
D	Clk	Q
0	↑	0
1	↑	1
X	0	Q_{prev}
X	1	Q_{prev}

- Copies D to Q on the *rising edge* of the clock

D FLIP-FLOP VS. D LATCH



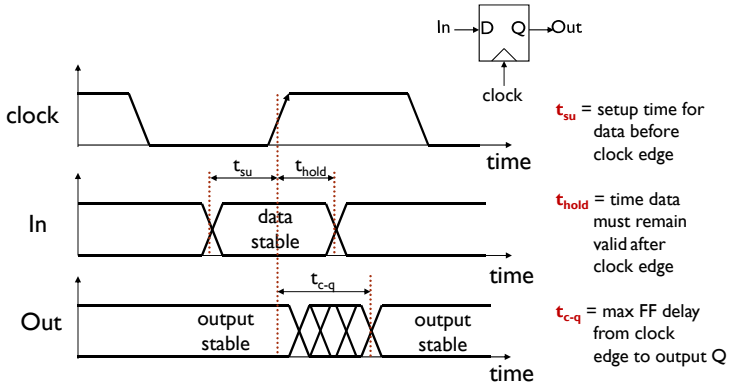
D FLIP-FLOP VS. D LATCH



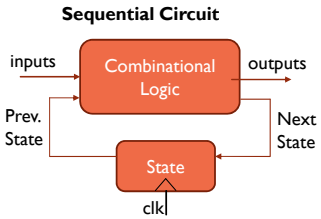
FLIP-FLOPS VS. LATCHES

- Why use a flip flop when it just takes twice as much logic?
- When would you want to use a flip-flop instead of a latch?

TIMING METRICS



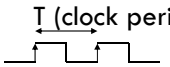
SYSTEM TIMING CONSTRAINTS



t_{plogic} = worst case delay through combinational logic

$t_{cdlogic}$ = min. delay through combinational logic

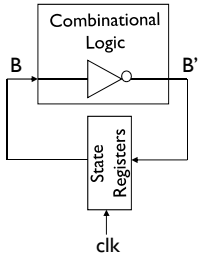
t_{cdreg} = min. delay through register logic

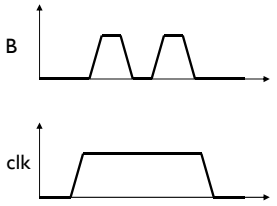


$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$

$t_{cdreg} + t_{cdlogic} \geq t_{hold}$

LATCH RACE PROBLEM





Which value of B is stored?

Two-sided clock constraint

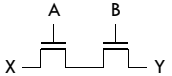
$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$

$T_{high} < t_{c\text{-}q} + t_{cdlogic}$

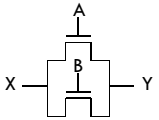
PASS TRANSISTOR LOGIC

NMOS TRANSISTORS IN SERIES/PARALLEL

- So far we have assumed that primary inputs are only allowed to drive gate terminals of MOS transistors.
- Now assume primary inputs can drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



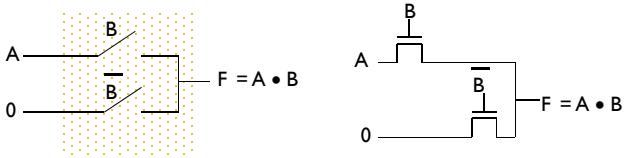
X = Y if A and B



X = Y if A or B

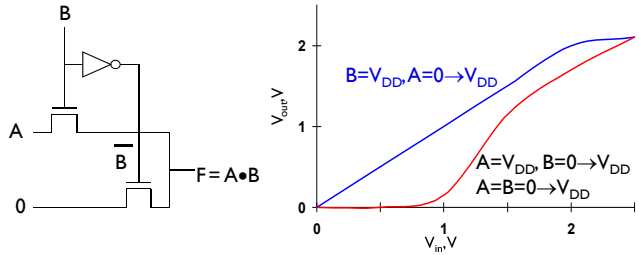
- Remember - NMOS transistors pass a strong 0 but a weak 1

PASS TRANSISTOR (PT) LOGIC



- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Bidirectional (versus non-directional)

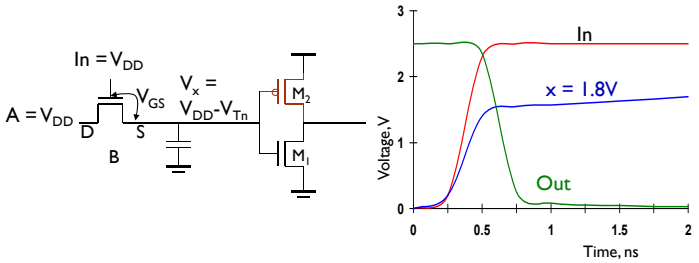
VTC OF PASS TRANSISTOR AND GATE



- Pure PT logic is not regenerative: signal gradually degrades after passing through a number of PTs

➡ fix with static CMOS inverter insertion

NMOS ONLY PT DRIVING AN INVERTER



- V_x does not pull up to V_{DD}, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power dissipation (M_2 may be weakly conducting forming a path from V_{DD} to GND)