BROWN
School of Engineering

DIGITAL ELECTRONICS SYSTEM DESIGN

FALL 2019

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NOVEMBER 4, 2019

LECTURE 16: A/D CONVERTERS AND OP AMPS

1

ANNOUNCEMENTS

- McKenna is changing his Friday lab hours to 11am-1pm

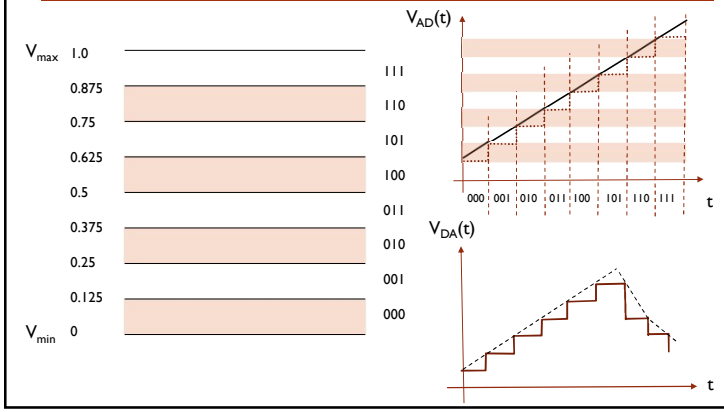
2

ENGN 1630 LABS 7, 8:
ANALOG TO DIGITAL CONVERTERS

- Interface to the "real" world involves analog signals,
  - Inputs derived from sensors (temperature, flow, position, velocity, acceleration, magnetic field,….)
  - Outputs generated to control devices (motors, engines, valves, heaters, lights,…..)
- Wide range of voltage and current values and their variations in time → specialized analog circuit techniques (not the domain of this course!)
- A/D and D/A conversion: Translate between a limited voltage range contained within the $[0, V_{DD}]$ range of the digital circuit, and the set of all 2^n n-bit binary numbers (for some value of n)

3

A/D AND D/A CONVERSION



4

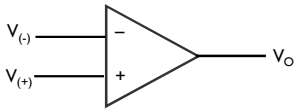
IDEAL OP-AMP (OPERATIONAL AMPLIFIER)

Model for a general-purpose component that solves the loading problem (among other things!)

Has a very large input resistance, small output resistance, and amplifies any difference between the voltages at the two input terminals

Power supply connections generally NOT shown on circuit schematics

Analysis *with negative feedback*: assume $V_{(+)} = V_{(-)}$ and no current flow into or out of the input terminals. Output sources or sinks any current necessary to achieve these conditions.

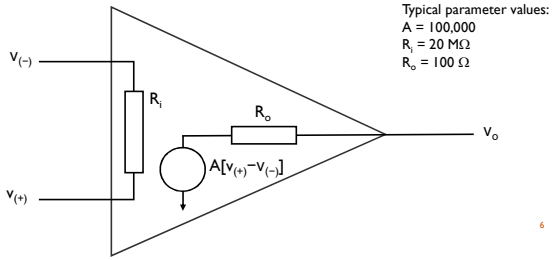


5

5

REAL OP-AMP

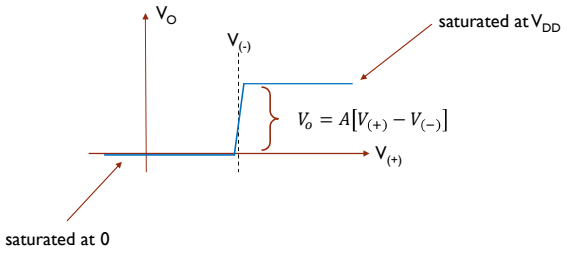
- First attempt to model the non-ideal behavior of actual op-amps
- Incorporates a dependent voltage source and two resistors
- Enables a more detailed analysis of op-amp circuits, such as the voltage follower



6

6

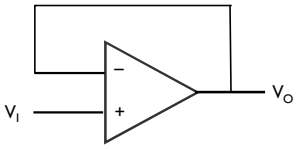
OP-AMP OPEN LOOP (= COMPARATOR)



7

UNITY-GAIN BUFFER (VOLTAGE FOLLOWER)

- Output voltage follows the input voltage (gain = 1)
- Very high input resistance
- Very low output resistance
- Effectively isolates the behavior of the "upstream" and "downstream" circuit functions

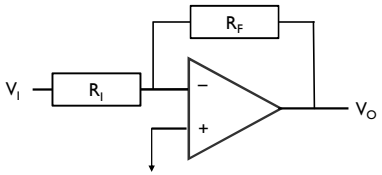


8

8

ANALOG INVERTER

- Output voltage follows the input voltage but with the opposite sign (gain = -1)



$$V_{(-)} \cong V_{(+)} = 0$$

$$\frac{V_I}{R_I} = \frac{0 - V_o}{R_F}$$

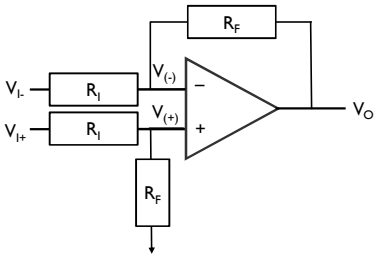
$$V_o = -\left(\frac{R_F}{R_I}\right) V_I$$

9

9

SUMMING AMPLIFIER

- Output voltage follows the sum of two input voltages, one taken with the opposite sign



$$V_{(-)} \cong V_{(+)} = \frac{R_F}{R_I + R_F} V_{I+}$$

$$\frac{V_{I-} - V_{(-)}}{R_I} = \frac{V_{(-)} - V_o}{R_F}$$

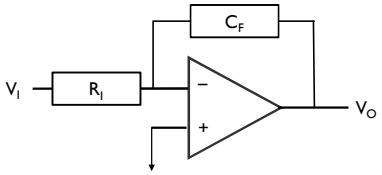
$$V_o = ?$$

10

10

INTEGRATOR

- Output voltage is the time integral of the input voltage, with the opposite sign, and with a scale factor



$$V_{(-)} \cong V_{(+)} = 0$$

$$\frac{V_I}{R_I} = C_F \frac{d}{dt}(0 - V_o)$$

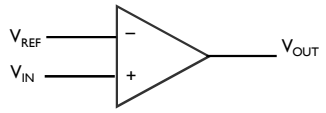
$$V_o = -\left(\frac{1}{R_I C_F}\right) \int V_I dt$$

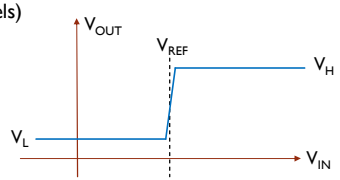
11

11

COMPARATOR

- Fundamental interface between the analog and digital domains
- Component with analog inputs (arbitrary voltages) and a digital output (two defined levels, "low" and "high").
- In your kits, LM 311
- Basically a high-gain amplifier intended to be used in saturation (its output driven all the way to the V_H or V_L levels)

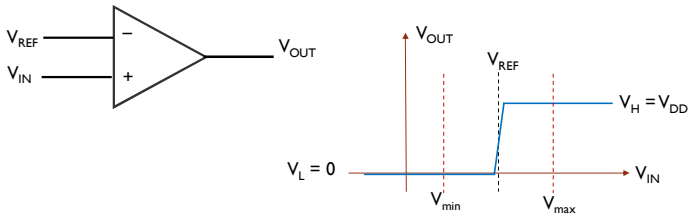




12

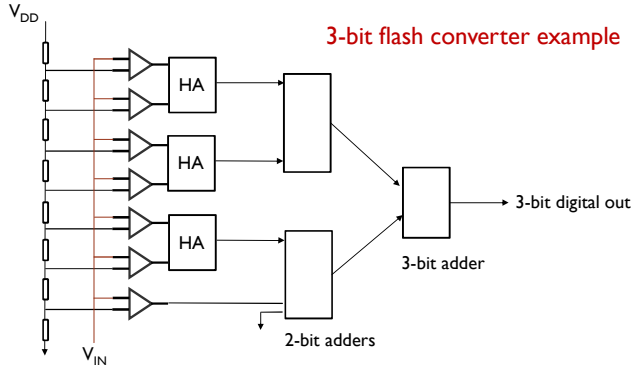
COMPARATOR: 1-BIT A/D CONVERTER

- Set the reference voltage at ½ of the analog signal range
- Operate the comparator with the same voltage supply as the digital logic
- Output is 0 for voltage below threshold, 1 for voltage above threshold



13

N-BIT PARALLEL (FLASH) A/D CONVERTER (2^N – 1 COMPARATORS)



14

FLASH CONVERTER TRADE-OFFS

- Large number of comparators plus adder network or other logic stages (chip area increasing with 2^N)
- Comparator offset voltage must be less than ½ the LSB interval, which becomes challenging for 1 mV level and less
- Comparator offset matching
- Resolution up to 10 bits
- Highest speed (one clock cycle)

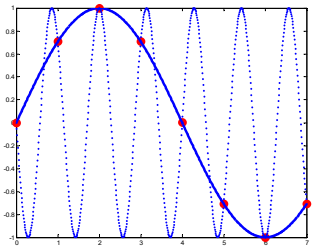
15

SAMPLING

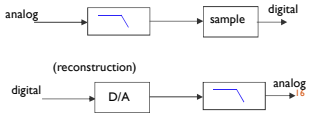
Voltage or current signals, which are continuous functions of time, have to be sampled in order to be represented digitally.

Sampling introduces ambiguity: what happens in between sample points?

If the maximum frequency present in the signal is f, the sample rate F_s must be greater than $2f$.

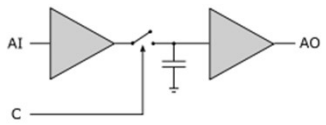


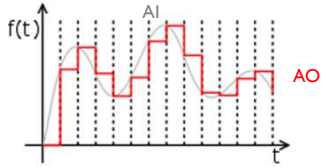
All frequencies greater than $F_s/2$ appear aliased in the interval $[0, F_s/2]$. To get rid of the confusion, signals must be band-limited (by low-pass filtering) to less than $F_s/2$ before the sampling operation.



16

SAMPLE AND HOLD (S/H)



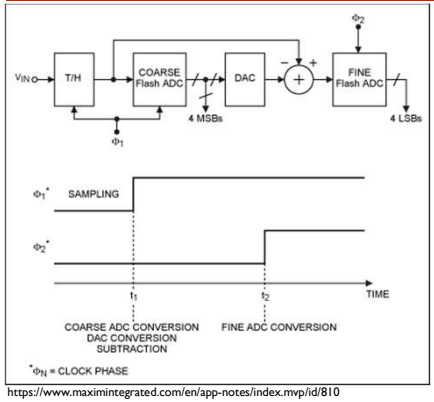


https://en.wikipedia.org/wiki/Sample_and_hold

- Clock signal C determines sampling instants
- Capacitor stores the sampled voltage between C pulses
- Unity-gain amplifiers buffer the sampling capacitor from input and output circuits
- Input side (or prior circuits) must band-limit the signal to less than half the sampling frequency
- Output presents a piece-wise constant signal to the A/D converter

17

SUB-RANGING A/D CONVERTER

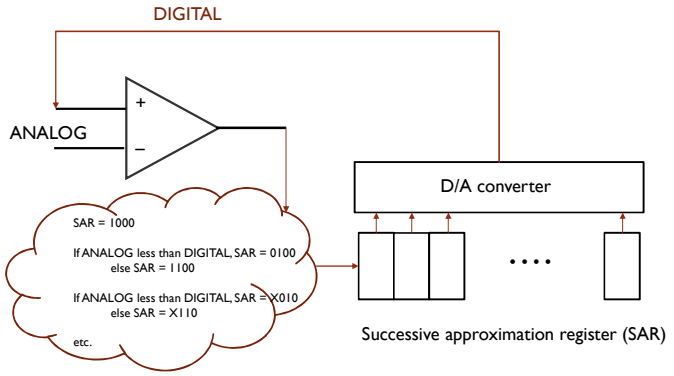


https://www.maximintegrated.com/en/app-notes/index.mvp/id/810

- One of many techniques for trading off conversion time and circuit cost
- 2 lower resolution flash A/D converters operating at half the rate
- D/A converter requires 8-bit accuracy in this example

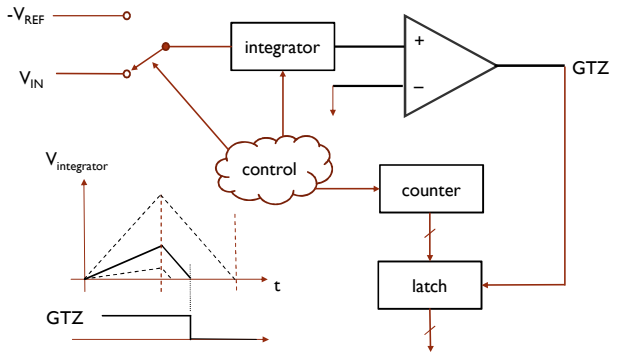
18

SUCCESSIVE APPROXIMATION A/D CONVERTER



19

DUAL-SLOPE A/D CONVERTER



20