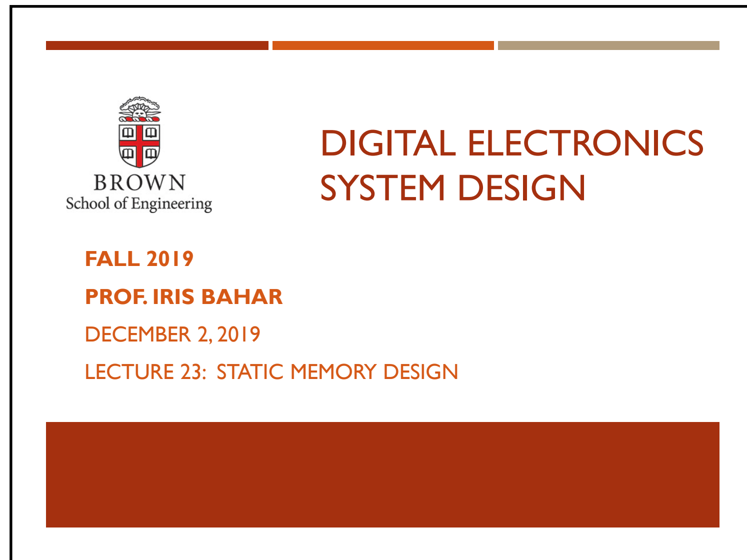
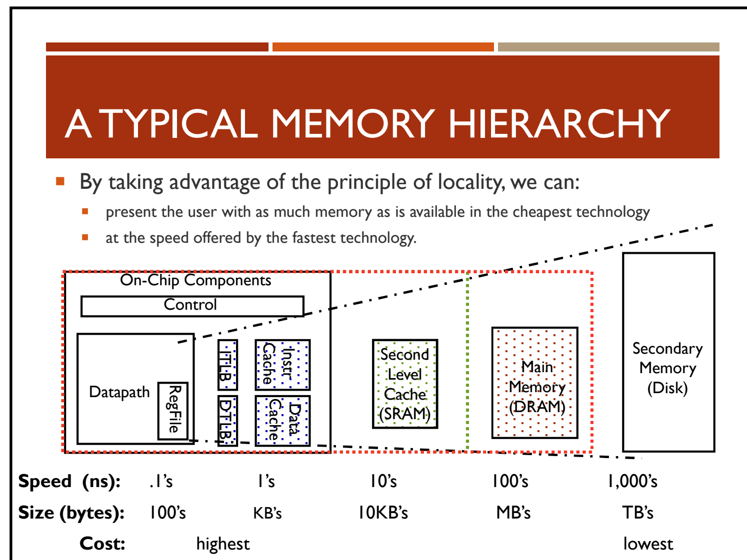


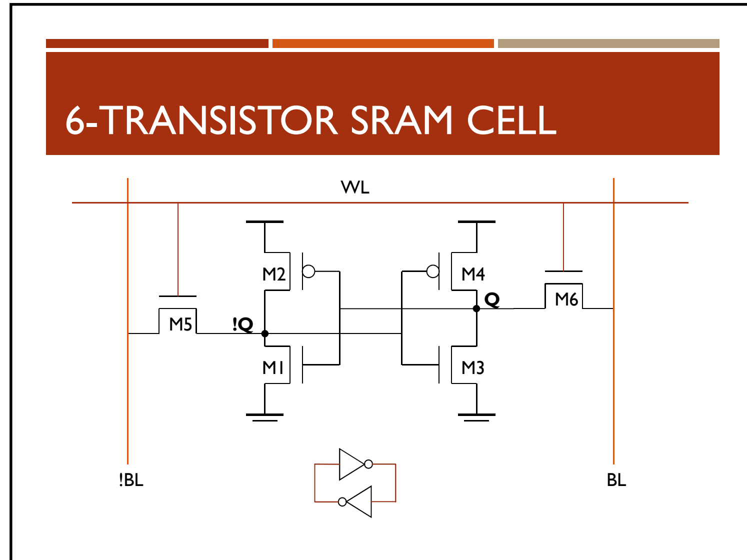
COURSE EVALUATIONS

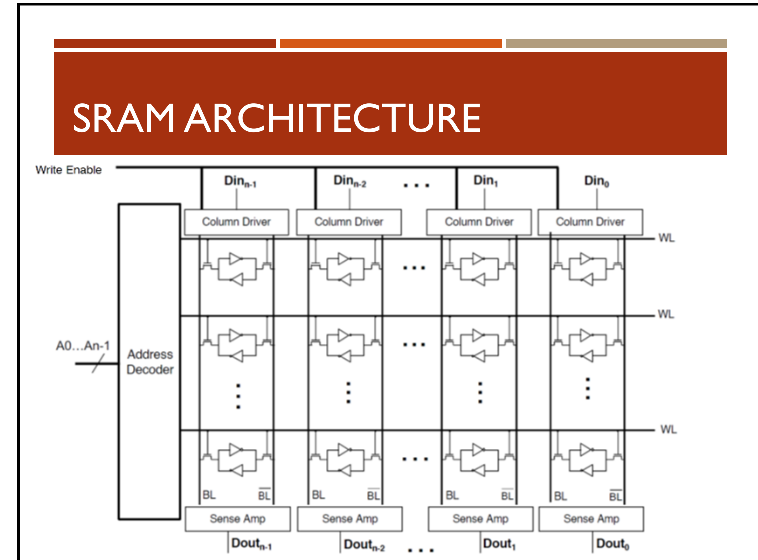
- Course evaluation forms are now available
- Please access using Banner self service
- Filling out this form provides me with important feedback about your experience with this course.
- Comments are confidential
- Available to me only after grades have been submitted.
- Thanks!

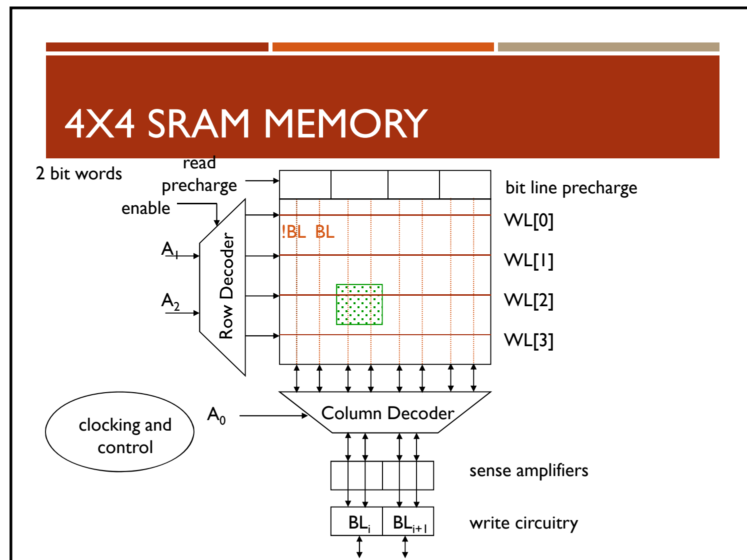


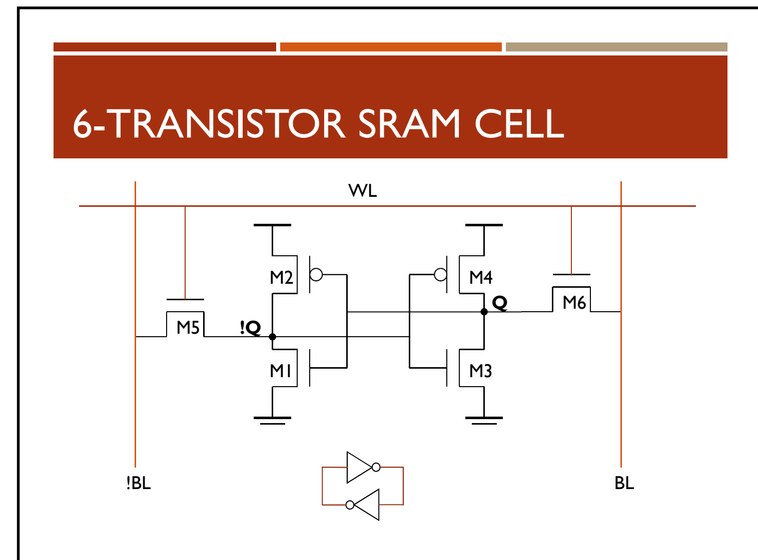
READ/WRITE MEMORIES (RAMS)

- Static – SRAM
  - data is stored as long as voltage supply is enabled
  - large cells (6 FETs/cell) → fewer bits/chip
  - fast → used where speed is important (e.g., caches)
- Dynamic – DRAM
  - periodic refresh required (every 1 to 4 ms)
  - small cells (1 to 3 FETs/cell) → more bits/chip
  - slower → used for main memories


6-TRANSISTOR SRAM CELL
WL
M2
M4
Q
M6
M5
!Q
M1
M3
!BL
BL

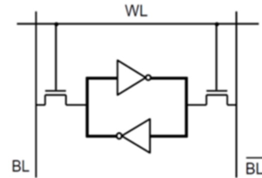

SRAM ARCHITECTURE
Write Enable
A0…An-1
Address Decoder
Column Driver
WL
Sense Amp


4X4 SRAM MEMORY
2 bit words
read precharge
enable
bit line precharge
WL[0]
WL[1]
WL[2]
WL[3]
!BL BL
Row Decoder
clocking and control
Column Decoder
sense amplifiers
write circuitry


6-TRANSISTOR SRAM CELL
WL
M2
M4
Q
M6
M5
!Q
M1
M3
!BL
BL

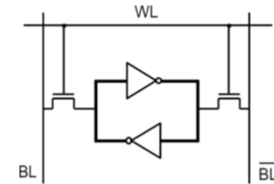
SRAM WRITE

- Drive on bit line high, the other low (depending on the desired write value)
- Then enable the word line (WL)
- Bit lines overpower cell with new value



SRAM READ

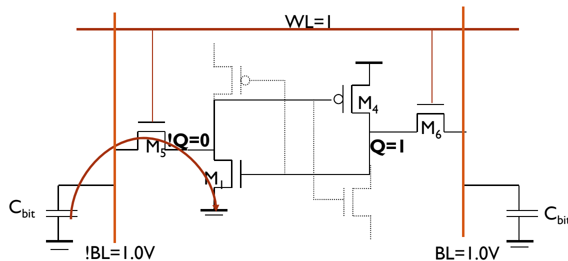
- Precharge both bit lines high
- Then enable word line (WL)
- One of the two bit lines will be pulled down by the cell
  - Change detected by sensor amplifier



How does the SRAM distinguish between reading or writing a cell?

How do you make sure you don't accidentally overwrite a cell value when you are trying to read?

SRAM CELL ANALYSIS (READ)

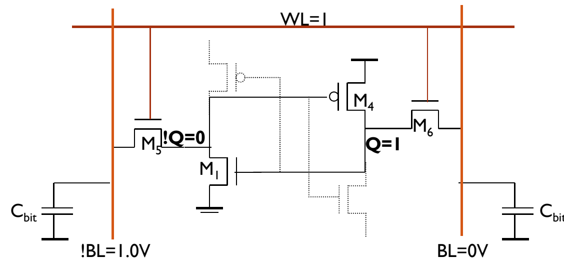


Read-disturb (read-upset): must carefully limit the allowed voltage rise on !Q to a value that prevents the read-upset condition from occurring while simultaneously maintaining acceptable circuit speed and area constraints

READ VOLTAGE RATIOS

- Keep cell size minimal while maintaining read stability
  - Make M_1 minimum size and increase the L of M_5 (to make it weaker)
    - Increases load on BL
  - Make M_5 minimum size and increase the W of M_1

SRAM CELL ANALYSIS (WRITE)



The !Q side of the cell cannot be pulled high enough to ensure writing of 1 (because of the on state of M_1). So, the new value of the cell has to be written through M_6.

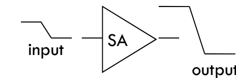
WRITE VOLTAGE RATIOS

- Need to pull Q below V_{thn} to turn off M_1
- Keep cell size minimal while allowing writes
  - Make M_4 and M_6 minimum size
- Be sure to consider worst case process corners

CELL SIZING AND PERFORMANCE

- Keeping cell size minimal is critical for large caches
  - Minimum sized pull down devices (M1 and M3)
    - Requires longer than minimum channel length pass transistors (M5 and M6) to ensure proper Cell Ratio
    - But up-sizing of the pass transistors increases capacitive load on the word lines and limits the current discharged on the bit lines both of which can adversely affect the speed of the read cycle
  - Minimum width and length pass transistors
    - Boost the width of the pull downs (M1 and M3)
    - Reduces the loading on the word lines and increases the storage capacitance in the cell – both are good! – but cell size may be slightly larger
- Performance is determined by the read operation
  - To accelerate the read time, SRAMs use sense amplifiers (so that the bit line doesn't have to make a full swing)

SENSE AMPLIFIERS



- Amplification: resolves data with small bit line swings
- Delay reduction: compensates for the limited drive capability of the memory cell

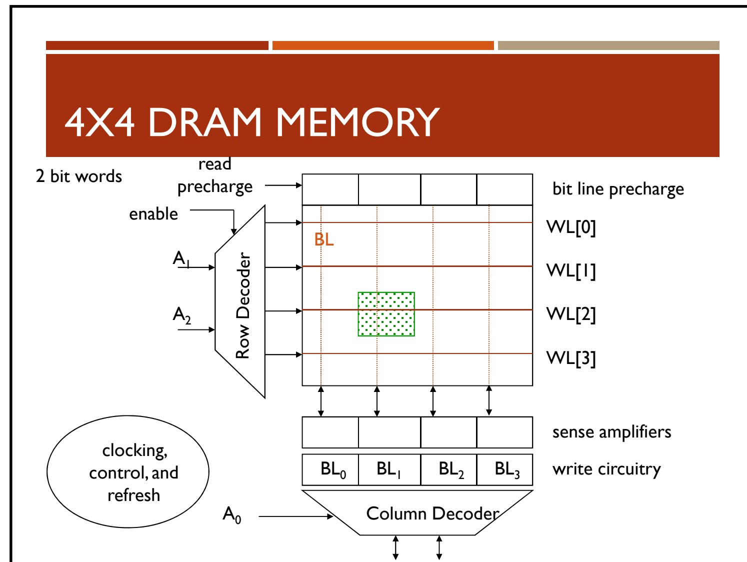
$$t_p = (C * \Delta V) / I_{av}$$

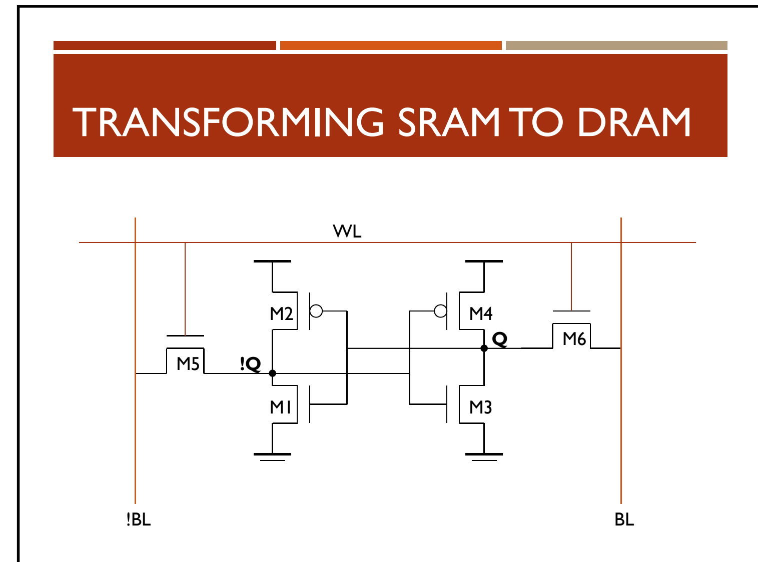
large (t_p); make Δ V as small as possible; small (I_{av})

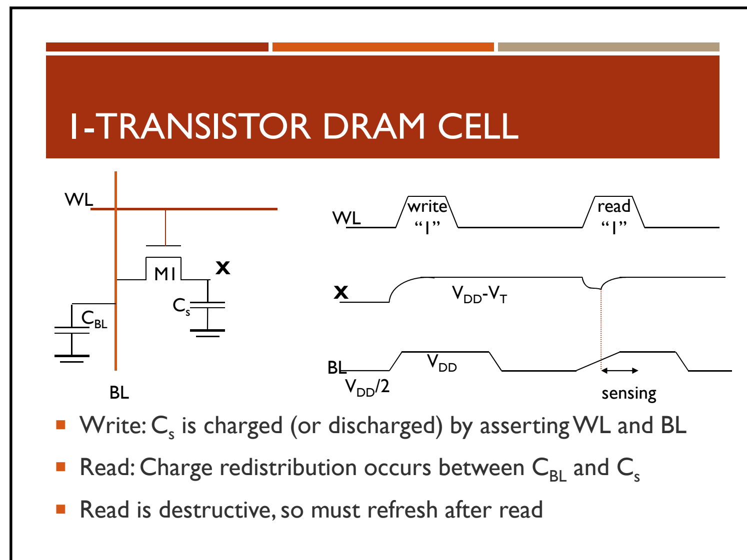
- Power reduction: eliminates a large part of the power dissipation

$$P = ½ C * V_{DD} * \Delta V * f$$

make Δ V as small as possible







- Write: C_s is charged (or discharged) by asserting WL and BL
- Read: Charge redistribution occurs between C_{BL} and C_s
- Read is destructive, so must refresh after read

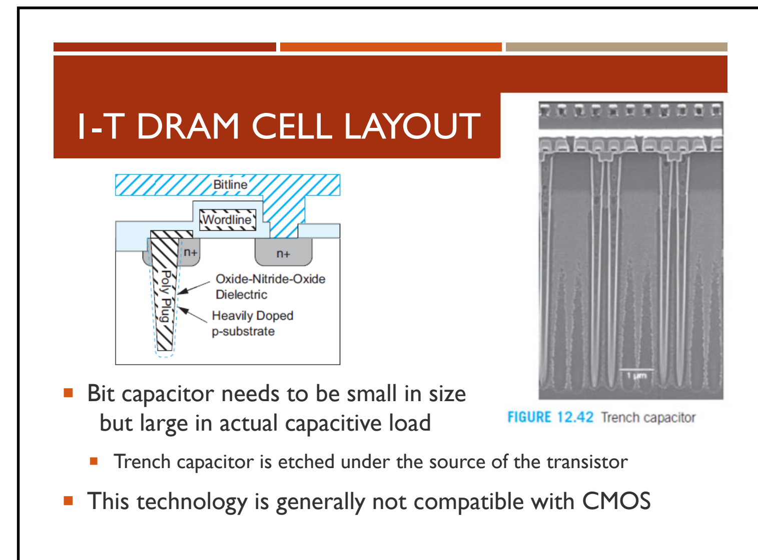


FIGURE 12.42 Trench capacitor

- Bit capacitor needs to be small in size but large in actual capacitive load
  - Trench capacitor is etched under the source of the transistor
- This technology is generally not compatible with CMOS

1-T DRAM CELL OBSERVATIONS

- Cell is single ended (complicates the design of the sense amp)
- Cell *requires* a sense amp for each bit line due to charge redistribution based read
  - all previous designs used SAs for speed, not functionality
- Cell read is destructive; refresh must follow to restore data
- Cell requires an extra capacitor (CS) that must be explicitly included in the design
  - not always compatible with logic CMOS process
- A threshold voltage is lost when writing a 1 (can be circumvented by bootstrapping the word lines to a higher value than VDD)