BROWN
School of Engineering

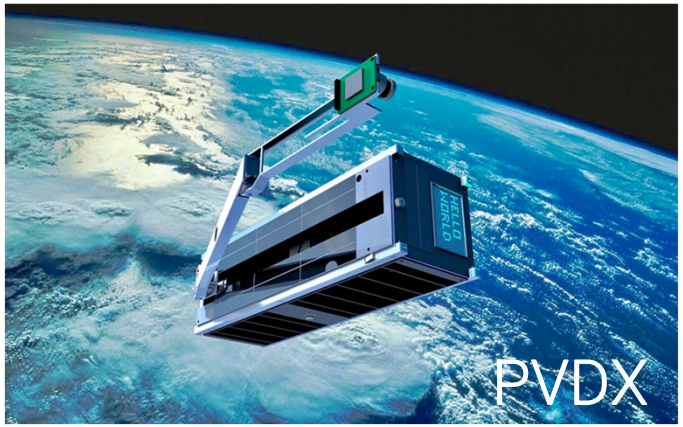
DIGITAL ELECTRONICS SYSTEM DESIGN

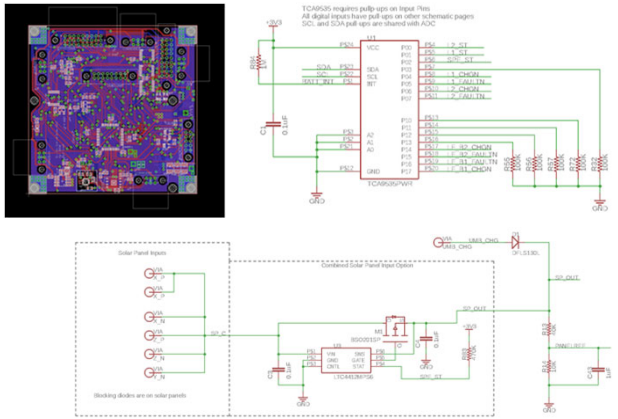
FALL 2019

PROF. IRIS BAHAR

DECEMBER 4, 2019

LECTURE 24: DYNAMIC MEMORY DESIGN





Sundays 1PM
Barus and Holley 190*
bse@brown.edu

LAB PRINTOUT AND RETURN

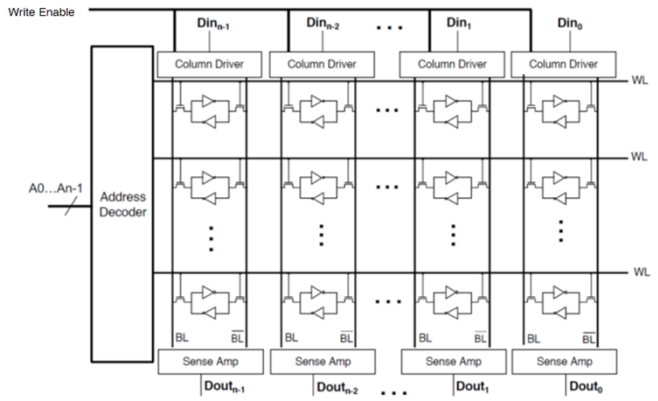
- Lab 2 has been graded.
  - Jiwon should have sent you an email with comments. Please get back to her with corrections (if needed).
- Lab 9 has been graded (by Prof. Patterson)
  - Those who require to resubmit, please redo, print out, and give directly to Prof. Patterson for fast turn around.
- Schematic requirement (for lab 1, 5, 7, 8, or A)
  - Print out your schematic and BOM for grading
  - This is due by Friday (but please complete sooner, if possible)

COURSE EVALUATIONS

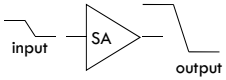
- Course evaluation forms are now available
- Please access using Banner self service
- Filling out this form provides me with important feedback about your experience with this course.
- Comments are confidential
- Available to me only after grades have been submitted.

- Thanks!

SRAM ARCHITECTURE



SENSE AMPLIFIERS



- Amplification: resolves data with small bit line swings
- Delay reduction: compensates for the limited drive capability of the memory cell

$$t_p = (C * \Delta V) / I_{av}$$

small

large

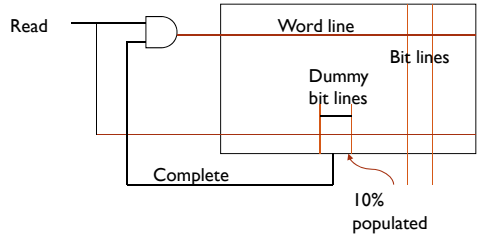
make Δ V as small as possible

- Power reduction: eliminates a large part of the power dissipation

$$P = \tfrac{1}{2} C * V_{DD} * \Delta V * f$$

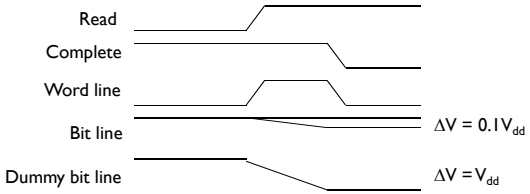
make Δ V as small as possible

PULSED WORD LINE FEEDBACK



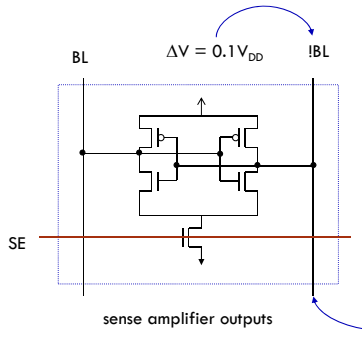
- Dummy column
  - height set to 10% of a regular column and its cells are tied to a fixed value
  - capacitance is only 10% of a regular column

PULSED WORD LINE TIMING

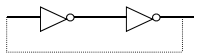


- Dummy bit lines have reached full swing and trigger pulse shut off when regular bit lines reach 10% swing

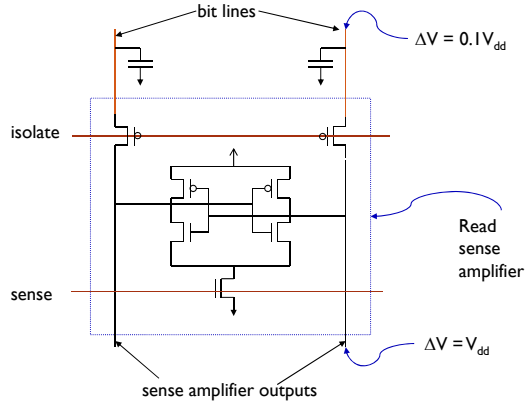
LATCH BASED SENSE AMPLIFIER



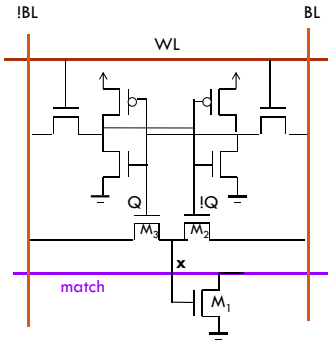
- When SRAM cell is read, SE=0 (disabling amplifier)
- After short read period, SE=1, turning on cross-coupled inverters



BIT LINE ISOLATION FOR SENSING

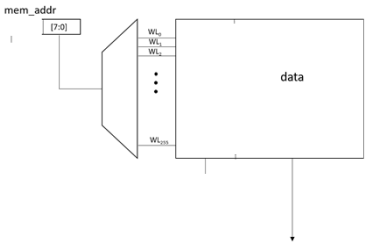


CONTENT ADDRESSABLE MEMORY



- Memory is addressed by its contents
- Writes progress as in a standard SRAM cell
- Compares the stored data (Q and !Q) to the bit line data
  - Precharged match line ties to all cells in a row
  - If Q and BL don't match, **x** is charged to $V_{DD} - V_T$ and the match line discharges
- This is a fancy address decoder!

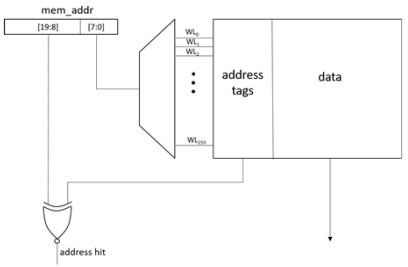
HOW DO YOU DESIGN A DATA CACHE FROM SRAM?



Say you want to store 1kB of data in your cache using SRAM

- *How many 32-bit words can you store in your SRAM?*
- *How many address bits do you need to access all words uniquely?*
- *If you have a 20-bit memory address, how many bit remain?*

WHAT IS THIS TAG FIELD?

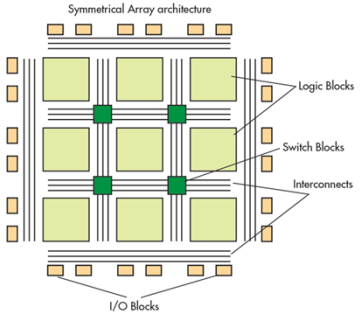


- *We have 8 bits of the address used to access the data*
- *How do you distinguish between address 1011100011 and address 0111100011 ?*
- *We need to store a piece of the memory address along with the data. This is the TAG field*

- *We have 20-8 = 12 bits remaining of the memory address that become the TAG field*
- *Read the tag along with the data to see if this the data you desire.*

FIELD PROGRAMMABLE GATE ARRAY (FPGA)

- FPGAs are chips containing configurable logic blocks (CLBs) and programmable interconnect
- Each CLB contains a reprogrammable LookUp Table (LUT) and Flip-Flops for storage.
- The CPLDs you have been using in your labs are scaled back version of FPGAs (10^3 vs. 10^5 logic blocks and less memory)

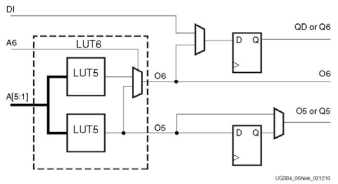


MODERN FPGAS

- Modern FPGAs contain many additional specialized blocks:
  - Internal memory (Block RAM)
  - Memory controllers
  - Clock multipliers/dividers
  - Digital signal processing (DSP) units for fast arithmetic
  - Bus interfaces
  - Simple processors (e.g., ARM)

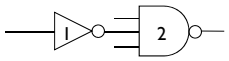
LOOKUP TABLES

- A Lookup Table is a logic function generator made up of memory that essentially stores the truth table of a function.
- An n-input LUT can implement any function consisting of *n* inputs
  - 2^{2^n} different functions possible, so for n=4, 16,536 different functions



The connectivity of a single LUT6 block in a Xilinx Spartan-6 FPGA.

LOOKUP TABLE



- How do you program a 3-input LUT for this function?
- This is a 1-bit wide memory with 2^3 address lines

LUT MEMORY CELLS

- It is convenient to program the FPGA and then retain that programming even when disconnected from power (i.e., using non-volatile memory.
- One way to do this is with flash-memory based FPGAs

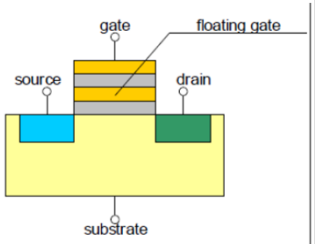


Fig. 2: A floating-gate transistor used in flash memory

FLOATING GATE TRANSISTOR

- Gate is electrically isolated, creating a floating node.
- A number of inputs are deposited above the floating gate and are electrically isolated from it.
- Since the floating gate is completely surrounded by a highly resistive material, the charge remains unchanged.