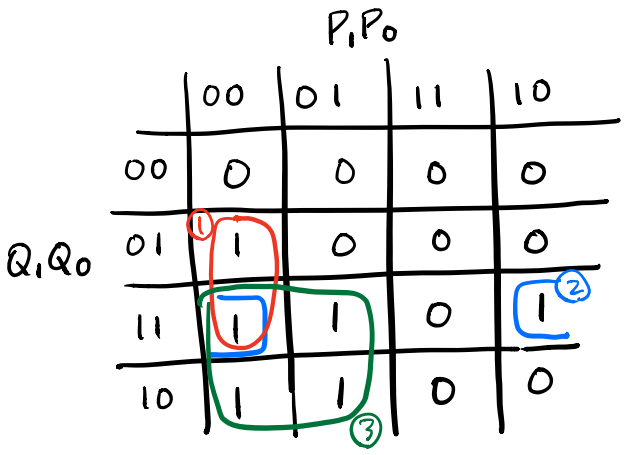
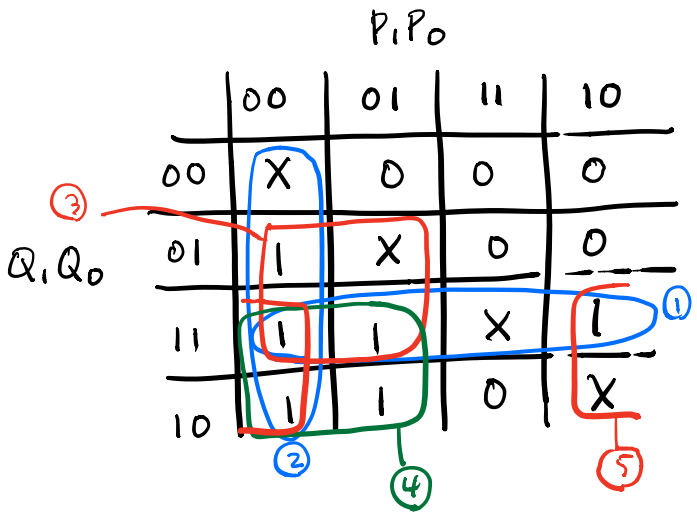
1. (a) $P < Q$ only



$out = \overline{P_1}\,\overline{P_0}\,Q_0 + \overline{P_0}\,Q_1Q_0 + \overline{P_1}\,Q_1$

①, ②, ③ are the prime implicants and the essential prime implicants.

(b) $P < Q$ w/ $P = Q$ don't care



①, ②, ③, ④, ⑤ are prime implicants.

possible solutions: (any of the three are correct)

Ⓐ if $out = Q_1Q_0 + \overline{P_1}\,\overline{P_0} + \overline{P_1}\,Q_1$

①, ②, ④ are the essential prime implicants.

Ⓑ if $out = Q_1Q_0 + \overline{P_1}\,Q_0 + \overline{P_1}\,Q_1$

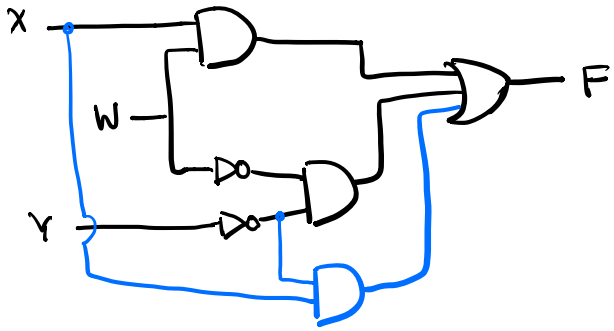
①, ③, ④ are the essential prime implicants.

Ⓒ if $out = \overline{P_1}\,Q_0 + \overline{P_1}\,Q_1 + \overline{P_0}\,Q_1$

③, ④, ⑤ are the essential prime implicants.

2. (a) $F = WX + \bar{W}\bar{Y} + X\bar{Y}$

W \ XY	00	01	11	10
0	1			1
1			1	1



There is a potential timing hazard when $X=1$, $Y=0$, and W switches from $1 \to 0$.

need to add the blue term to remove hazards.

(b) $F = W\bar{X}\bar{Y} + X\bar{Y}Z + XY + W\bar{Y}Z$

WZ \ XY	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	1	0	1	1
10	1	0	1	0

There is a potential timing hazard when $W=1$, $Y=0$, $Z=1$, and X switches from $1 \to 0$.

Need to add the blue term to remove hazards.

(c) $F = WY + \bar{W}\bar{Z} + X\bar{Y}Z + \bar{W}X\bar{Y} + WXZ + Y\bar{Z}$

WZ \ XY	00	01	11	10
00	1	1	1	1
01	0	0	0	1
11	0	1	1	1
10	0	1	1	0

There are multiple timing hazards in this circuit:

① when $X=1$, $Y=0$, $W=0$, and Z switches from $1 \to 0$.

② when $X=1$, $W=1$, $Z=1$, and Y switches from $1 \to 0$.

③ when $Y=1$, $Z=0$. (X can be anything) and W switches from $1 \to 0$

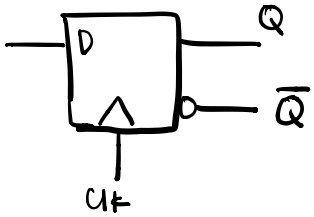
Need to add all blue terms to remove all three timing hazards.

3. (a) When T is low, the T flip-flop stores the value Q. When T is high, the T flip-flop toggles the value of Q at every positive clock edge.

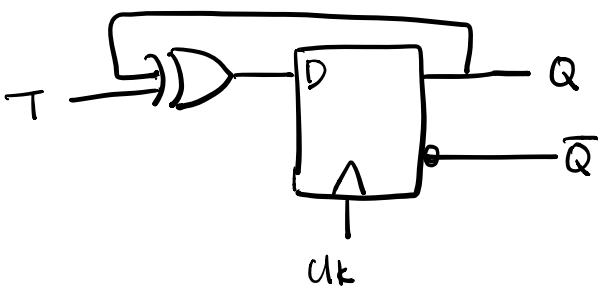
(b) $Q_{next} = \bar{T}Q + T\bar{Q} = T \oplus Q$ ($\oplus$: XOR)

Q \ T	0	1
0	0	1
1	1	0

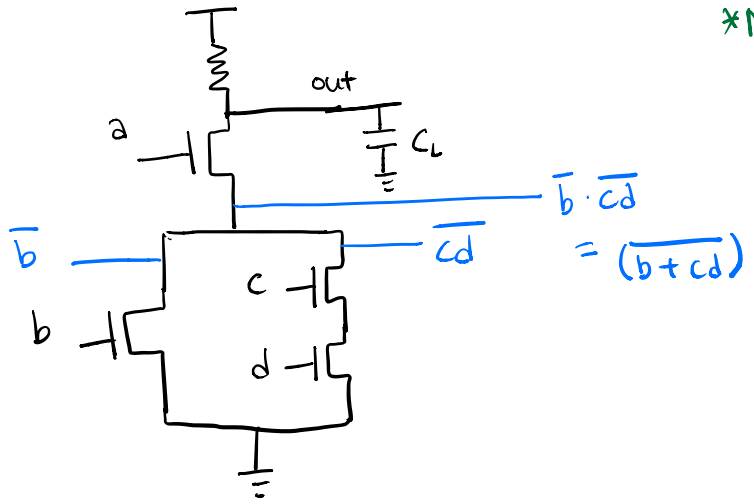
(c) D-flip flop symbol:



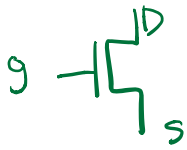
T-flip flop:



4.



*Note: NMOS transistor



when $g=0$ ($V_{gs} < V_{th}$) no current flows,

when $g=1$ ($V_{gs} \geq V_{th}$) current flows.

(a) current will flow when $a=1$ AND ($b=1$ OR $cd=1$)

(out = 0 when current flows, otherwise 1)

$$out = \overline{a(b+cd)}$$ //

(b) *Note: 1st order approximation $t_{PHL} = 0.69\, R_n \cdot C_L$ (R_n: total resistance to drain)

*Note: resistance of NMOS $R_n \propto \frac{L}{\mu_n W}$

t_{PHL} depends on total resistance to drain.

resistance of gates depends on L/W.

longest path in given circuit — when $a=c=d=1$

$$t_{PHL} = \underbrace{\alpha \frac{L_{min}}{W_{min}}}_{t_{PHL} \text{ for min. size inverter}} = \alpha\left(\frac{L_a}{W_a} + \frac{L_c}{W_c} + \frac{L_d}{W_d}\right)$$

Note: need to reduce resistance/gate but cannot reduce length beyond minimum size ⇒ increase width

assuming gates a, c, d are same size.

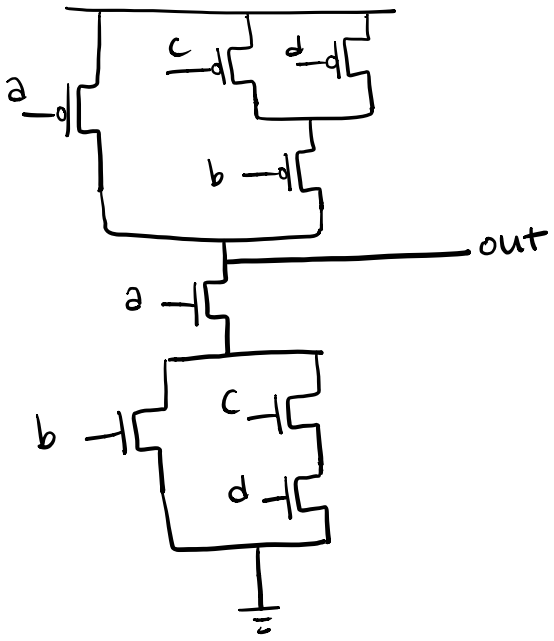
$$L_a = L_c = L_d = 50nm, \quad W_a = W_c = W_d = 450nm$$ //

when $a=b=1$.

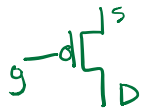
$$t_{PHL} = \alpha \frac{L_{min}}{W_{min}} = \alpha\left(\frac{L_a}{W_a} + \frac{L_b}{W_b}\right) = \alpha\left(\frac{L_{min}}{3W_{min}} + \frac{L_b}{W_b}\right)$$

$$L_b = 50nm, \quad W_b = 225nm$$ //

(c) fully - complementary CMOS gate



*Note : PMOS transistor



when g is high ($|V_{gs}| < |V_{thn}|$) no current flows.
when g is low ($|V_{gs}| \geq |V_{thn}|$) current flows.

$$t_{pLH} = 0.69\, R_p \cdot C_L$$
$$R_p \propto \frac{L}{\mu_p W}$$

$$\frac{L}{\mu_p W} = \frac{2.5L}{\mu_n W}$$

worst - case path : $c = b = 0$

$$t_{pHL} = \alpha \frac{L_{min}}{W_{min}}$$

$$t_{pLH}\ (\text{for this circuit}) = \alpha \cdot 2.5 \cdot \left(\frac{L_b}{W_b} + \frac{L_c}{W_c}\right) = \alpha \frac{L_{min}}{W_{min}}$$

$$\frac{L_b}{W_b} + \frac{L_c}{W_c} = \frac{1}{2.5} \times \frac{L_{min}}{W_{min}}$$

assuming PMOS gates b, c are the same size,

$L_b = L_c = 50nm$, $W_b = W_c = 2 \cdot 2.5 \cdot W_{min} = 750\,nm$

PMOS gate d should be the same size as PMOS gate c (for $b = d = 0$)

$L_d = 50nm$, $W_d = 750nm$

if $a = 0$ —— $t_{pLH} = \alpha \cdot 2.5 \frac{L_a}{W_a} = \alpha \cdot \frac{L_{min}}{W_{min}}$

$$\frac{L_a}{W_a} = \frac{L_{min}}{2.5\, W_{min}}$$

$L_a = 50nm$, $W_a = 375nm$

(d) $(a,b,c,d) = (1,0,1,1)$ causes worst-case fall delay.

$t_{pHL} \propto R_n$. where R_n is the effective drain resistance.

$(a,b,c,d) = (1,0,1,1)$ is when the drain path has highest resistance.

(e) $R_{min} = 5\,k\Omega = K\frac{L_{min}}{W_{min}}$

(K constant including μ_n)

$C_L = 50\,fF\ (= 50 \times 10^{-15}\ F)$

worst-case $t_{pHL} = 0.69 \cdot (R_a + R_c + R_d) \cdot C_L$

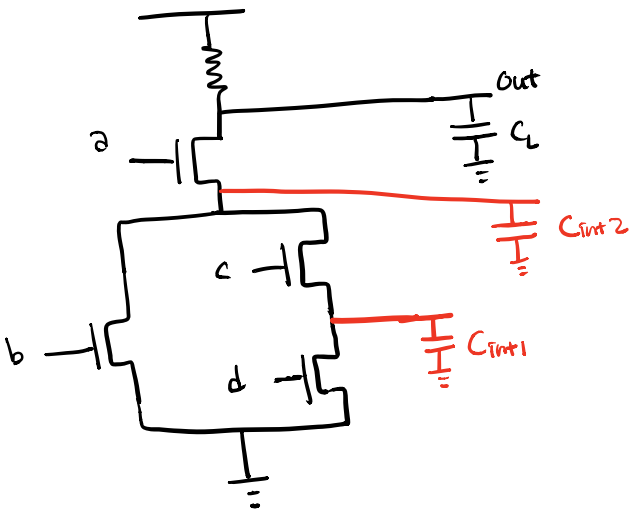
$R_a = R_c = R_d = K \cdot \frac{L_{min}}{3W_{min}} = \frac{5}{3}k\Omega$

$= 0.69 \cdot \left(3 \times \frac{5}{3} \times 10^3\ \Omega\right) \cdot 50 \times 10^{-15}\ F$

$= 172.5 \times 10^{-12}$ seconds

($1\ F \approx 1$ second $/\ \Omega$)

(f) pull-down path — NMOS circuit



$W_a = W_c = W_d = 3\,W_{min}$

$W_b = 1.5\,W_{min}$

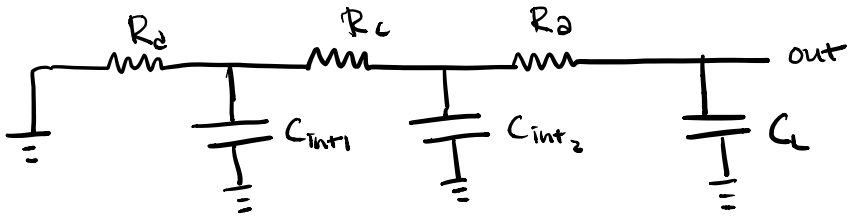
C_{int1} — connected to source of c and drain of d.

$C_{int1} = 3 \cdot C_{dmin} + 3C_{dmin} = 6 \cdot C_{dmin} = 3\,fF$

C_{int2} — connected to source of a and drain of b, c

$C_{int2} = 3\,C_{dmin} + 1.5\,C_{dmin} + 3\,C_{dmin} = 7.5\,C_{dmin} = 3.75\,fF$

(g)



(using input vector from part (c), transistor b is off)

$$t_{PHL} = 0.69 \cdot \left(3fF \times \frac{5}{3}k\Omega + 3.75fF \times \frac{10}{3}k\Omega + 50fF \times \frac{15}{3}k\Omega\right)$$

$$= 0.69 \times (5 + 12.5 + 250) \times 10^{-15} \times 10^{3} \text{ seconds}$$

$$= 184.575 \times 10^{-12} \text{ seconds}$$