1. A 2-bit "comparator" circuit receives two 2-bit numbers, $P = P_1P_0$, and $Q = Q_1Q_0$. The comparator circuit produces a 1 if and only if $P < Q$.

    a. Using a K-map, design a minimum sum-of-products circuit for this 2-bit comparator. Identify all the prime implicants and essential prime implicants.

    b. How would you answer for part (a) of this question if the output can be either 0 or 1 when $P = Q$?

2. For each of the following logic expressions, use a K-map to find all potential timing hazards in the corresponding two-level AND-OR circuit, and design a hazard-free circuit that realizes the same logic function.

    a. $F = WX + W'Y'$
    b. $F = WX'Y' + XY'Z + XY$
    c. $F = WY + W'Z' + XY'Z$

3. The table below summarizes the behavior of a *T flip-flop*.

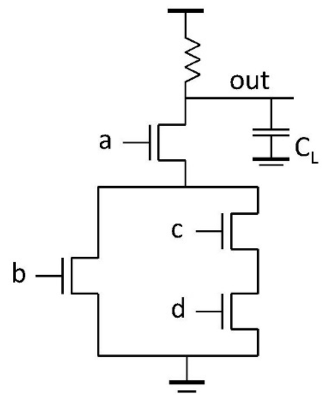
T	Clk	Q	Q_{next}
0	X	X	Q
1	Positive edge	0	1
1	Positive edge	1	0

    a. Describe in words the behavior of this device.

    b. Find a Boolean expression for this device's output.

    c. Using a D flip-flop and a minimum number of additional logic gates, design the T flip-flop.

4. Consider the following NMOS gate with pull-up resistor:



(a) What Boolean function does this gate implement?

(b) Assume a minimum transistor has W_{min}=150nm and L_{min}=50nm. Size the NMOS devices for the gate such that as a first order approximation, the t_{pHL} delay of the gate is the same as the t_{pHL} delay of a minimum sized inverter. Size the ***longest path first*** and write the transistor sizes (W and L) next to each transistor. Show your calculations below, if needed.

(c) Now consider designing the complex gate as a static, fully-complementary CMOS gate. Draw the transistor-level representation of the full gate and size the PMOS devices in terms of W_{min} such that rise time is approximately the same as fall time (for worst case paths). Assume that the mobility of the NMOS device is 2.5× greater than the PMOS (i.e., $\mu_n = 2.5\mu_p$)

(d) What input vector {a,b,c,d} produces a worst case fall delay t_{pHL}? Explain your reasoning.

(e) If the resistance of a minimum sized NMOS is R_{min}=5KΩ, and the output load is C_L=50fF, what is the approximate *worst case fall delay, t_{pHL}*, for the gate to reach the 50% point (ignoring effects of intrinsic capacitance on internal nodes)? Show your calculations.

(f) Now add source/drain intrinsic capacitance to all *internal* nodes in the pull-down path (ignore any additional capacitance at the output node). Assume that each source/drain connected to a node contributes a capacitance of $C_d = x \cdot C_{dmin}$ to the total node capacitance, where x is the width of the transistor relative to a *minimum sized transistor* and C_{dmin} = 0.5fF. Show your calculations for all the internal node capacitances and draw the capacitances with values on the diagram above.

(g) Given the additional internal capacitances from part (e), draw the equivalent RC network and re-calculate the worst case fall delay t_{pHL} for the gate using the Elmore delay model, assuming the same input vector from part (c). Explain your reasoning. Recall that the Elmore delay equation is:

$$t_p = \sum_{i=0}^{N} c_i r_{ij} = \sum_{i=0}^{N} c_i \sum_{j=0}^{i} r_j$$