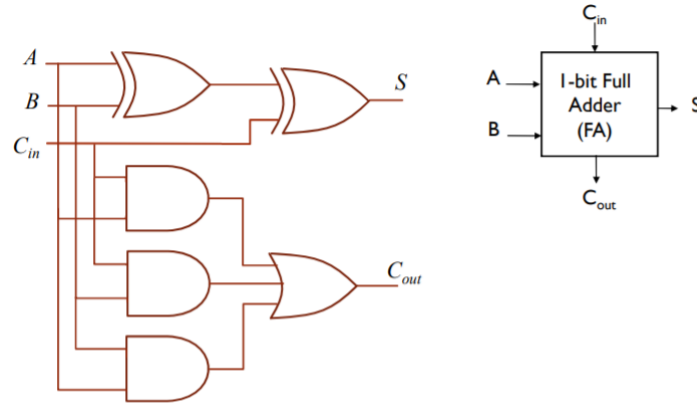


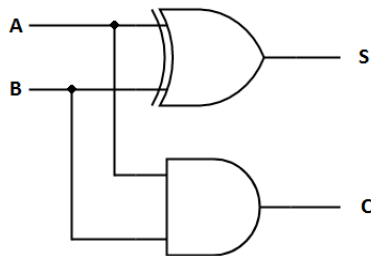
1. Assume that an inverting gate has a delay of 1 unit, an AND gate or an OR gate with no complemented inputs has a delay of 2 units, and an XOR gate has a delay of 3 units. Based on the full-adder design shown below, what is the worst-case delay from any input to any sum output and the carry output for an 8-bit ripple carry adder?



2. Using the same assumptions as #1, what is the worst-case delay from any input to any sum output, as well as the worst-case delay to the carry output for an 8-bit carry lookahead adder with 4-bit ripple carry adders? (Note that  $P_i$  and  $G_i$  are not provided and instead must be computed using the inputs  $A_i$  and  $B_i$ .)
3. When would a ripple-carry adder be preferred over other fast adder designs?

4. How would you design an 4x4 combinational multiplier using ROM? Determine the size of the array and what the address inputs would be.

5. Consider a 4x4 carry-save multiplier. Assume the full-adder design shown in #1, and the half-adder design shown in the Figure below. What is the critical path and the worst-case delay? Assume that all logic gates have a delay of  $t_G$ .



6. Compare the ROM-based multiplier and the carry-save multiplier from #4 and #5. What would be the advantage and disadvantage of the ROM-based multiplier?

7. Convert the following binary numbers to decimal assuming (1) unsigned binary notation, (2) ones' complement notation, and (3) two's complement notation.

- a. 1011
- b. 1100
- c. 10100100
- d. 10011110
- e. 01001001