```
//////////////////////////////////////////////////////////////////////////////////
//
// Create Date:    12:49:56 10/20/2017
// Design Name:
// Module Name:    three_bit
// Project Name:  Three_Bit_Count_Example
// Target Devices:  XC9572XL
// Description:  Verilog module for a simple 3-bit binary counter with no enable signal
//
// Revision 0.01 - File Created as a class example of simple FSM
//
//////////////////////////////////////////////////////////////////////////////////
module three_bit(input clk, output [2:0] qout);
//
// State Table - simple perpetual counter
parameter STATE0 = 3'b000, STATE1 = 3'b001, STATE2 = 3'b010, STATE3 = 3'b011,
                                        STATE4 = 3'b100, STATE5 = 3'b101, STATE6 = 3'b110, STATE7 = 3'b111;
//
// State register declaration
reg [2:0] pres, nxt;  // Register I/O names
always @ (posedge clk) pres <= nxt;             // instantiate register

// Next state logic
always @ (*) begin           // cominational logic
        case (pres)
                STATE0: nxt = STATE1; STATE1: nxt = STATE2;
                STATE2: nxt = STATE3; STATE3: nxt = STATE4;
                STATE4: nxt = STATE5; STATE5: nxt = STATE6;
                STATE6: nxt = STATE7; STATE7: nxt = STATE0;
                default: nxt = STATE0;
                endcase
        end

// Connect state register to output
assign qout = pres;

endmodule
```