
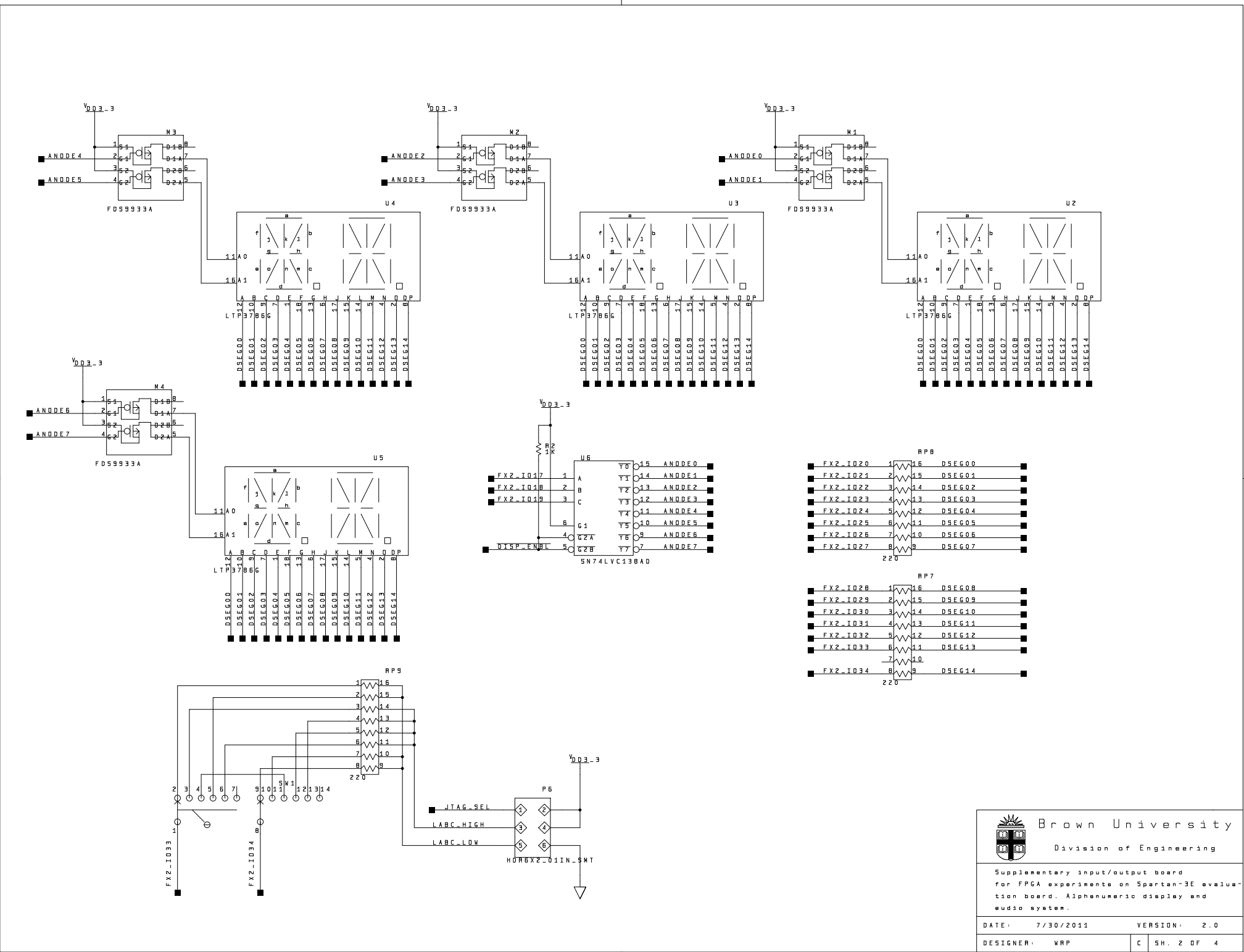



P4 TCDNN20		P3 TCDNN20		P2 TCDNN20	
FX2_I033	19 SIG00	FX2_I017	19 SIG00	FX2_I001	19 SIG00
FX2_I034	18 SIG01	FX2_I018	18 SIG01	FX2_I002	18 SIG01
FX2_I035	17 SIG02	FX2_I019	17 SIG02	FX2_I003	17 SIG02
FX2_I036	16 SIG03	FX2_I020	16 SIG03	FX2_I004	16 SIG03
FX2_I037	15 SIG04	FX2_I021	15 SIG04	FX2_I005	15 SIG04
FX2_I038	14 SIG05	FX2_I022	14 SIG05	FX2_I006	14 SIG05
FX2_I039	13 SIG06	FX2_I023	13 SIG06	FX2_I007	13 SIG06
FX2_I040	12 SIG07	FX2_I024	12 SIG07	FX2_I008	12 SIG07
FX2_CLKIN	11 SIG08	FX2_I025	11 SIG08	FX2_I009	11 SIG08
FX2_CLKOUT	10 SIG09	FX2_I026	10 SIG09	FX2_I010	10 SIG09
FX2_CLKIO	9 SIG10	FX2_I027	9 SIG10	FX2_I011	9 SIG10
	8 SIG11	FX2_I028	8 SIG11	FX2_I012	8 SIG11
	7 SIG12	FX2_I029	7 SIG12	FX2_I013	7 SIG12
	6 SIG13	FX2_I030	6 SIG13	FX2_I014	6 SIG13
	5 SIG14	FX2_I031	5 SIG14	FX2_I015	5 SIG14
	4 SIG15	FX2_I032	4 SIG15	FX2_I016	4 SIG15
	3 CLK		3 CLK		3 CLK

HDR26_DB[17:00]								LPC_PORT0B[21:00]							
HDR26_DB08	8	HDR26_DB09	9	HDR26_DB10	10	HDR26_DB11	11	LPC_PORT0B00	0	LPC_PORT0B01	1	LPC_PORT0B02	2	LPC_PORT0B03	3
HDR26_DB12	12	HDR26_DB13	13	HDR26_DB14	14	HDR26_DB15	15	LPC_PORT0B04	4	LPC_PORT0B05	5	LPC_PORT0B06	6	LPC_PORT0B07	7
HDR26_DB16	16	HDR26_DB17	17					LPC_PORT0B08	8	LPC_PORT0B09	9	LPC_PORT0B10	10	LPC_PORT0B11	11
								LPC_PORT0B12	12	LPC_PORT0B13	13	LPC_PORT0B14	14	LPC_PORT0B15	15
								LPC_PORT0B16	16	LPC_PORT0B17	17	LPC_PORT0B18	18	LPC_PORT0B19	19
								LPC_PORT0B20	20	LPC_PORT0B21	21				

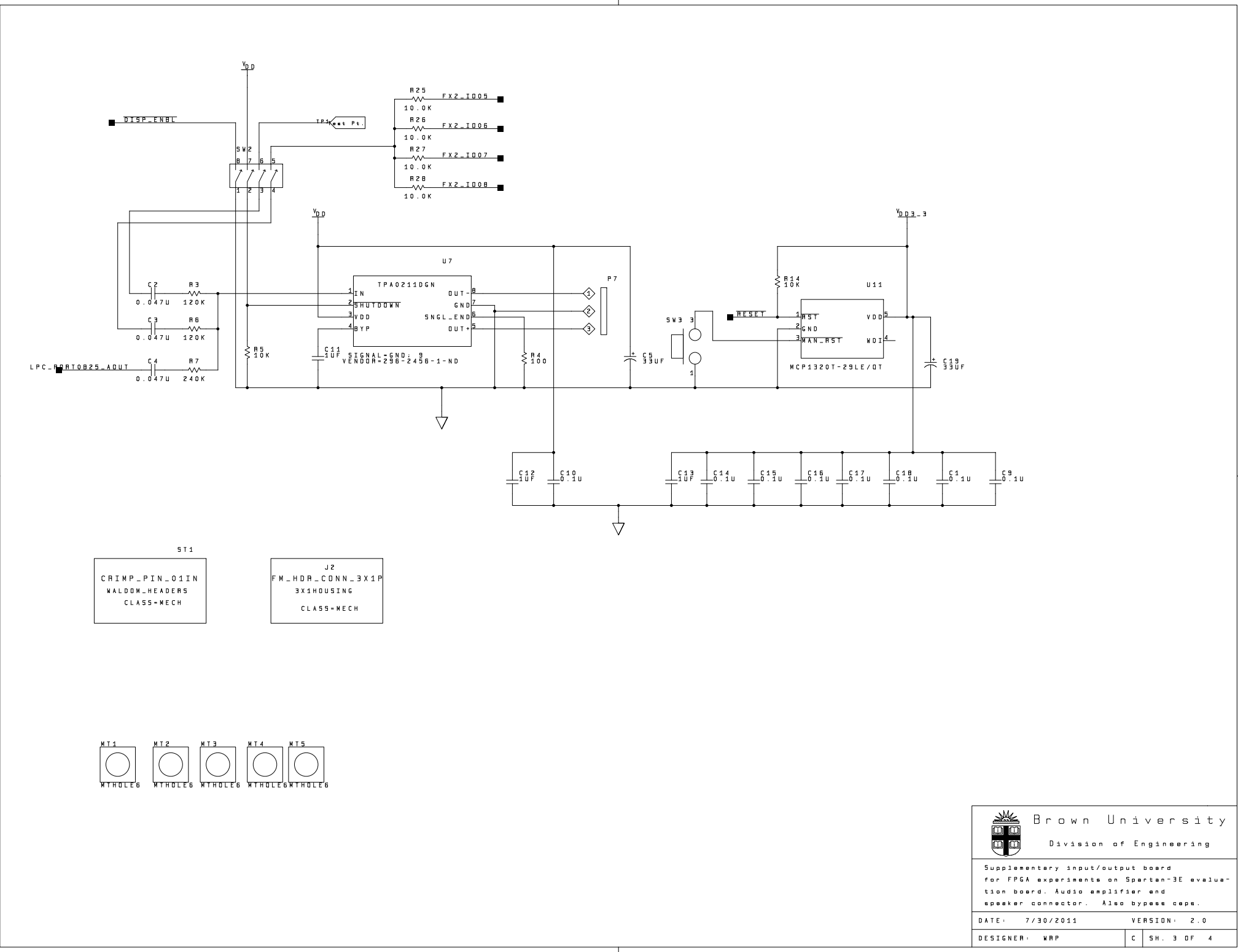
2.0	Correct JTAG pullups, pins for display size R packs
1.0	Baseline unit with triple usb support
REV.	Revision Notes
 Brown University School of Engineering	
Supplementary input/output board for FPGA experiments on Spartan-3E evaluation board. Connector and current limit resistor packs.	
DATE: 7/30/2011	VERSION: 2.0
DESIGNER: WRP	C SH.1 OF 4




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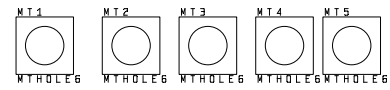
Supplementary input/output board
 for FPGA experiments on Spartan-3E evaluation
 board. Alphanumeric display and
 audio system.


DATE: 7/30/2011	VERSION: 2.0
DESIGNER: WRP	C SH. 2 OF 4



ST1
CRIMP_PIN_01IN
WALDOM_HEADERS
CLASS-MECH

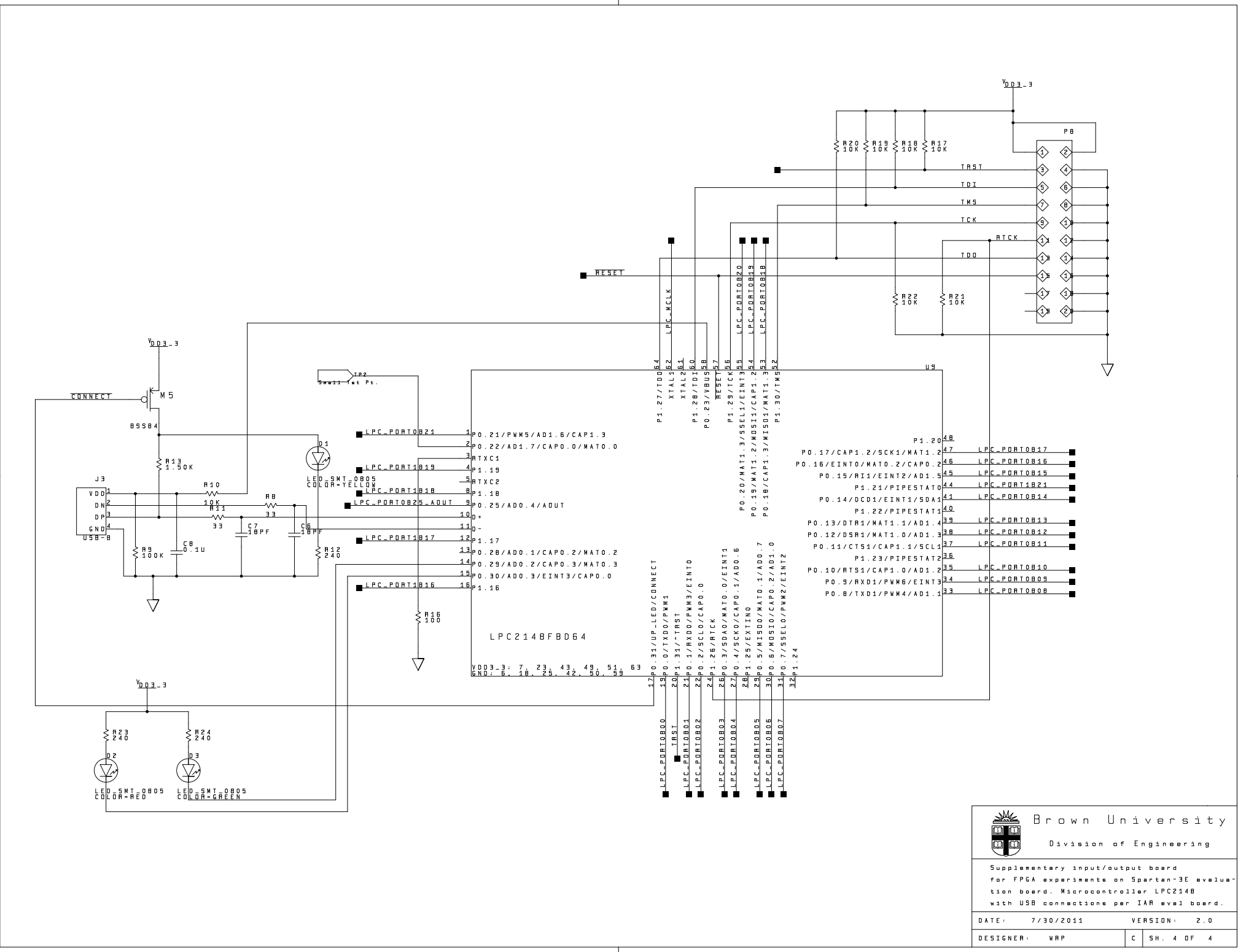
J2
FM_HDR_CONN_3X1P
3X1HOUSING
CLASS-MECH




 Brown University Division of Engineering	
Supplementary input/output board for FPGA experiments on Spartan-3E evalua- tion board. Audio amplifier and speaker connector. Also bypass caps.	
DATE: 7/30/2011	VERSION: 2.0
DESIGNER: WRP	C SH. 3 OF 4

A

B




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Supplementary input/output board
 for FPGA experiments on Spartan-3E evalua-
 tion board. Microcontroller LPC2148
 with USB connections per IAR eval board.

DATE: 7/30/2011	VERSION: 2.0
DESIGNER: WRP	C SH. 4 OF 4