Engineering 1630 – Digital System Design
Fall Semester AY 2016-17

Professor: Prof. Wm. R. Patterson
Office - B. H. 449, ext 3-1449.
William_Patterson@brown.edu

Office hours: I do not schedule regular office hours. Instead I am prepared to answer questions or deal with problems as they arise. I am available at any time you can find me in Barus & Holley (or *Au Bon Pain*). A list of my haunts and the phone numbers thereof is posted on my office door. If it is inconvenient to see you then, I will tell you so and arrange an alternate time. Otherwise, feel free to take advantage of my availability – the offer is genuine. I am especially available after class and am willing to make appointments either after class or by email, at least for a day or two ahead.

Course Goals: This course presents a broad range of techniques useful for digital logic design. Students completing ENGN1630 should

1. Be able to design combinational and sequential logic for a wide range of systems, including making appropriate allowances for timing constraints.

2. Be able to understand CMOS transistors and their use in logic circuits well enough to do timing, power, and load calculations, to use bidirectional buses properly, and to be prepared to study VLSI systems.

3. Be able to realize a logic design in an appropriate choice of discrete logic, a CPLD or an FPGA.

4. Be able to use CAD tools for schematic capture, logic simulation, and programmable design, and to understand the role and advantages of hardware description languages in design, particularly Verilog.

5. Be able to make use of memory and simple processors and to understand the idea of a register transfer machine.

Work Expectation: There are three hours per week of class for 14 weeks (42 hours). I usually make sure there are that number of hours by running over class time. I also ask questions of you during class expecting some response which means I expect your mind to be working during class. There are both a mid-term and a final exam. The preparation for each would normally require about 8 hours of study and review (16 hours). The primary way you demonstrate mastery of the material of the course is through completion of the lab challenges. Those have point weightings depending on the difficulty of the lab and it takes 62 points to pass the course. It will usually take about 2 hours of study and lab work to earn a point. The total is 42+16+124 = 182 hours.

Teaching Assistants: Reza Azimi will be this year's Head TA. While I have several seniors who took the course last year who would like to be TAs and who should be very good at the job, we have not yet worked out their schedule. Overall we should have 25 – 30 hours of lab staffing per

week. We will post the hours, names, and schedules of all the TAs on the class web site shortly. You are not limited to their hours for working – they aren't lifeguards – but you do need to work with one of them for evaluation of your work on each lab.

Laboratory Space: The lab will be in the Hewlett Electronics Lab on the first floor of Giancarlo – Room 196. The computers in Room 196 have been updated with the latest software from Mentor Graphics, Xilinx, and Aldec. I have tested the Mentor Graphics and most of the Xilinx programs. I expect to finish that before labs start.

Laboratory Hours: Hours will start on Thursday, Sept. 15th – if all goes well. The exact hours when TAs will be available are still to be determined as I get them lined up. The website will show TA hours as soon as they are settled. Eventually we will have the lab itself open 20 hours a day during the week and much of the weekend but there will only be TA coverage for about 30 hours.

Laboratory Grade: This is primarily a lab course so some 63% of the grade will depend on the Labs you do. There will be a mid-semester and a final exam. Full details are in the *"Evaluation"* section of the introduction to the lab manual.

Lab Manual and Kit: The lab manual and kit will be available together for a fee of $ 60. (I am still editing the manual.) Very likely I will handle distributing kits myself. There will be a rebate of $ 50 through the Controller's Office after the end of the semester if you return the major parts of the kit. The difference is a photocopying cost, which is a regrettable necessity.

I am not making many changes to the manual this year. Lab D on the design of a simple microprocessor that I introduced two years ago worked very well this past year. I reserve the right to add another lab on dynamic RAM and serial buses if Reza and I can finish developing it in time. As usual when making changes, there will be some errors in the lab manual. Please let me know if something there does not make sense. I am still editing the manual and it will have to go to the printers when I am done. Last year's lab manual is on-line at the class web site and can be used until I get the new one printed.

Textbook: The suggested **OPTIONAL** textbook is William J. Dally and R. Curtis Harting, *Digital Design, A Systems Approach*, Cambridge University Press 2012. (In conformity with federal regulations, I must state that the list price for this book is $ 150.) I started to use this book last year and I am not entirely comfortable with the choice. I do not follow a textbook very closely so this is an optional purchase for you. The lectures and the lab manual may be enough to get you through the course. The previous book for the course was John F. Wakerly, *Digital Design: Principles and Practices, 4th Ed.*, Pearson Higher Ed Inc. I prefer that book but it has become outrageously expensive ($ 220) and is showing its age. It is noteworthy for its coverage of both VHDL and Verilog and for a graceful writing style. Its main problem is that much of its "practical" material is getting obsolete.

High-Tech: There is a website for the course accessible through the University's web pages at http://www.brown.edu/Departments/Engineering/Courses/En163/home.html. It will have schedules, lab changes, TA access information, etc. I am working on updating the site now.

Topics:

1. Boolean algebra, logic minimization, SOP and POS forms, K-maps
2. MOSFETs, static logic circuits, noise margins, signal levels, open-drain and three state circuits, flip-flops
3. Sequential circuits and finite state machines with counters as special cases
4. Floating gate devices and their use to build CPLDs and nonvolatile memory
5. Logic programming in Verilog hardware description language as used to synthesize simple circuits
6. CAD for schematic capture and programmable device programming
7. Semiconductor memory: SRAM, DRAM, ROM – asynchronous and synchronous
8. Field Programmable Gate Arrays (Xilinx examples) for logic implementation
9. Arithmetic: adders, fast carry methods, simple multiply, number representation (2's complement integers, offset binary, IEEE 754 floating point standard)
10. Register transfer machines and very simple models of computer structure.

Collaboration: The lab manual has a statement on my collaboration policy, some of which I repeat here to emphasize what I expect. Generally:

1. You may collaborate on labs by discussing them with your classmates and to some extent with the TAs. The TAs are supposed to give hints or debug suggestions but not to tell you how to do the lab. Please don't push them to exceed these bounds. In giving or taking advice this way, it is important to be sure you understand the problem and its solution. You may get stumped when questioned by a TA and end up losing credit for the lab if you prove clueless about how it is supposed to work
2. In all design labs, you must build, debug and demonstrate the system on your own boards yourself – your own fingers, parts, documentation, etc. TAs will check board numbers and have the right to ask for documentation, that is, the schematic or outline material that you used to guide assembly. This includes data entry for any Verilog code. Type it yourself not copying someone else's file. Offering someone else's work for this is NOT allowed. Precisely because it is hard to detect that sort of cheating, I will deal with it harshly should we detect it.
3. For the written reports for labs 2, 6, and 9 or schematic capture, you must take the data and write the report yourself. There is a requirement that a TA certify that he/she saw you take the data or demonstrate the results of lab 9**. I take a particularly harsh view of copying data or even two people taking data together and using copies** for their reports. Data is a certification that you did the measurements, and right or wrong this is what you got. Science and engineering depend on the reliability of that sort of certification for progress. Mistakes in data are normal but fakes or copies are strictly forbidden. In the "real" world the penalty for plagiarism is often ostracism. Consider: http://www.bostonglobe.com/news/science/2014/08/05/author-retracted-stem-cell-papers-commits-suicide/PjUPxOBh3k2qnGPIzQMwHL/story.html
4. If in a written report you choose to copy some picture or text to explain your work, you **must explicitly attribute that material to its source** with a footnote, not just a bibliography. You cannot copy from Wikipedia and paste into the report and expect us not to notice. You must write the report yourself subject to the usual limits on quotation and I recommend generating the figures yourself too – you learn more that way.