Engineering 1630 - Fall 2013: Answers to the First Optional Problem Set

1.) The minimum expression is $OUT = \overline{A}\,\overline{B}\,\overline{C}\,D + A\overline{C}\,\overline{D} + BCD + \begin{cases} AB\overline{C} \\ ABD \end{cases}$ and the appropriate

K-map is:

AB╲CD	00	01	11	10
00		1		
01			1	
11	1	1	1	
10	1			

There are two non-essential primes, one of which is included in the minimized expression.

2.) The shortest possible Gray code sequence for four variables is 8. If you look at the K-map of problem one, you can see it requires traversing three states in one column to change both A and B. Similarly you have to traverse three columns to change both C and D. Shortest way to do both is a 3 x 3 path traversing 8 states. It is obviously possible to traverse all 16 boxes and if you look carefully you can find three intermediate sequences of 10, 12, and 14 states.

3.) The NOR multiplexor is very similar to the NAND-based mux and is drawn below. The primary difference is the polarity of the select signals at the 3-input NOR gates. They are the complements for the NAND case.

To derive this result systematically, notice that if you combine the outputs of a set of NOR gates in one more such gate, the output is a product of sums (POS) expression. Each sum has the inputs of one of the gates in the input set. For example,

$$\overline{\overline{(A+B)} + \overline{(C+D)}} = (A+B)\cdot(C+D)$$

Therefore, to push the multiplexor into NOR form, we need a POS expression for its output. The way to get such an expression systematically **for any system** is to form the complement of the output as an SOP form by summing all the Boolean terms that are not included in the original expression. The complement of that expression is the output itself, and using DeMorgan's theorems it can easily be pushed into POS form. (If the SOP form is minimum, then the resulting POS form will be too.) The problem with doing this in the multiplexor case is that there are 64 minterms for the inputs and only 32 of those contribute to the output. To catalog and minimize the remaining 32 terms by brute force is cumbersome. The simple way to do the problem is to observe that complementing the output of a multiplexor is the same as complementing all the I_n inputs because no matter which input is selected, selecting the complement of its I_n will give the same output as complementing the selected I_n itself. This finesses the problem of minimizing a complicated multi-input expression. Thus: $\overline{OUT} = \overline{I_0}\cdot\overline{S_1}\cdot\overline{S_0} + \overline{I_1}\cdot\overline{S_1}\cdot S_0 + \overline{I_2}\cdot S_1\cdot\overline{S_0} + \overline{I_3}\cdot S_1\cdot S_0$ and by applying DeMorgan's Theorems:
$OUT = (I_0 + S_1 + S_0)\cdot(I_1 + S_1 + \overline{S_0})\cdot(I_2 + \overline{S_1} + S_0)\cdot(I_3 + \overline{S_1} + \overline{S_0})$
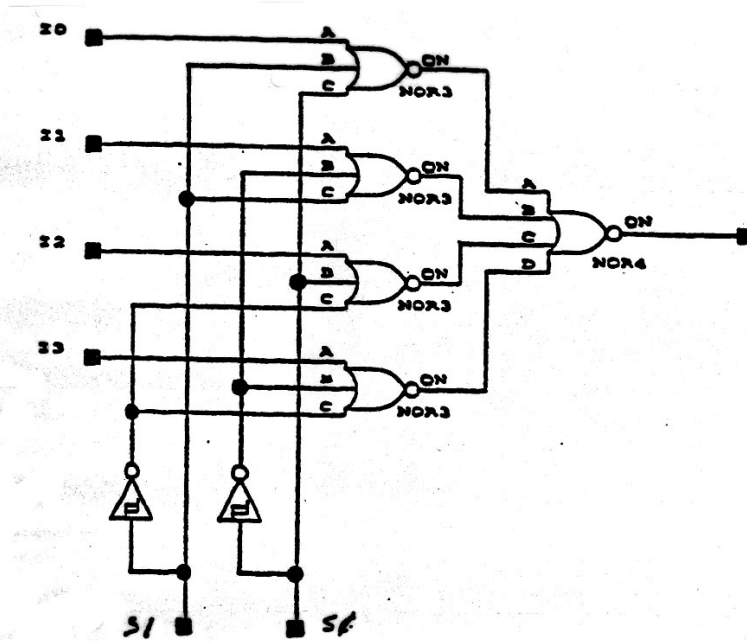
4.) $C = \bar{Y} \cdot \overline{Q_2} + X \cdot \overline{Q_1} \cdot Q_2$
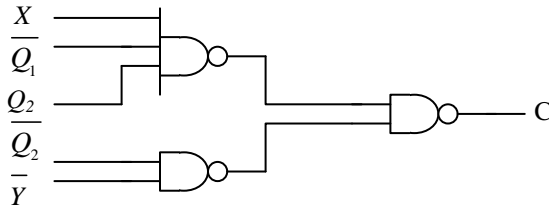
5.) The circuit is as shown on the right. For each transistor, if one neglects the term in the square of V_{DS}, then

$$I_D = \frac{W}{L} K(V_{GS} - V_{TH})V_{DS}$$

Because all three transistors have the same current and the same width to length ratio, we have:

$$(V_{GS1} - V_{TH})V_{DS1} = (V_{GS2} - V_{TH})V_{DS2} = (V_{GS3} - V_{TH})V_{DS3}$$

Clearly the voltage from source to drain of any one transistor has to be less than .3 volts because the sum of the three must be .9 volts or less. Also, the transistor on the bottom will have the smallest voltage since it has the largest gate voltage. Suppose we guess that $V_{DS1} = 0.25$ volts and see if that is acceptable. The drain current is

$$I_D = \frac{W}{L} K(V_{GS1} - V_{TH})V_{DS1} = 3 \cdot 5 \cdot 10^{-5} \cdot (4.1) \cdot 0.25 = 1.54 \cdot 10^{-4} \quad \text{amps.}$$

$V_{DS2} = .27V$

2
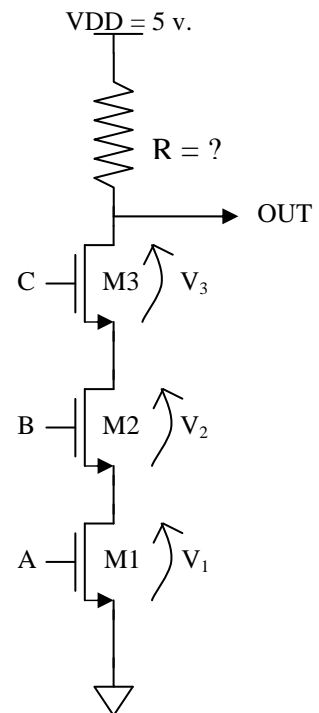
V_{DS3} = .29V

V_{OUT} = V_{DS1} + V_{DS2} + V_{DS3} = .81 V which is less than 0.9 by a little bit.

Finally, $R = \dfrac{(V_{DD} - V_{DS3})}{I_D} = \dfrac{5.0 - .81}{1.54 \cdot 10^{-4}} = 27.3$ Kilohms.

6.) This circuit can have glitches on D1 and D2. (The XOR was glitch free by definition.) All glitches are negative going and start a single propagation delay after the input transition. The possibilities I see are:

Before A B C	After A B C	Output Line	Glitch Width
001	110	D1	$1 \cdot \tau_P$
000	110	D1	$3 \cdot \tau_P$
010	110	D1	$3 \cdot \tau_P$
001	010	D2	$2 \cdot \tau_P$
100	010	D2	$2 \cdot \tau_P$
001	111	D2	$2 \cdot \tau_P$
100	111	D2	$2 \cdot \tau_P$

7.) Implement the CE (Count Enable) signal with a 1 of 2 multiplexor on the D line of each flip-flop. When CE = 0, the D's connect to the Q's. When CE = 1, the D's connect to the NEXT Q logic, which determines the count sequence. The state table is:

Q2	Q1	Q0	UP	$D'2$	$D'1$	$D'0$
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	1	0	0	0	1
0	1	1	1	0	1	0
0	1	0	0	0	1	1
0	1	0	1	1	1	0
1	1	0	0	0	1	0
1	1	0	1	1	1	1
1	1	1	0	1	1	0
1	1	1	1	1	0	1
1	0	1	0	1	1	1
1	0	1	1	1	0	0
1	0	0	0	1	0	1
1	0	0	1	0	0	0

3
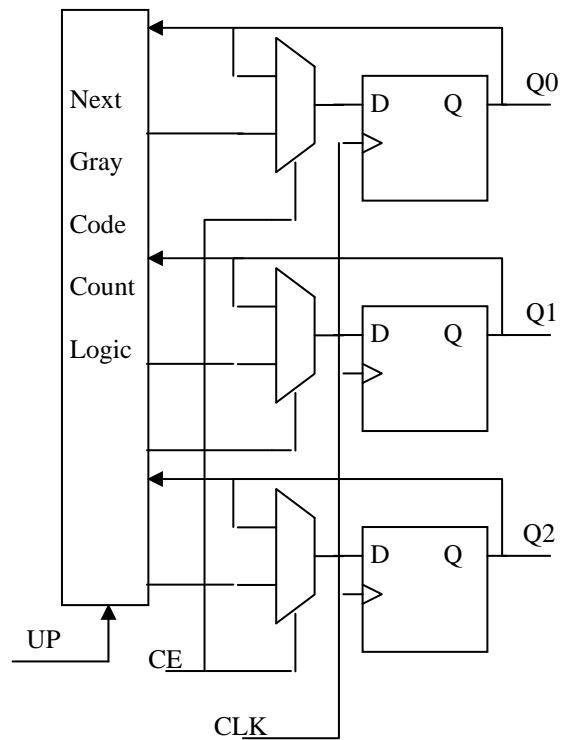
Q2Q1 \ Q0 UP	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

$$D_0' = \overline{Q2}\cdot\overline{Q1}\cdot UP + \overline{Q2}\cdot Q1\cdot\overline{UP} + Q2\cdot Q1\cdot UP + Q2\cdot\overline{Q1}\cdot\overline{UP}$$

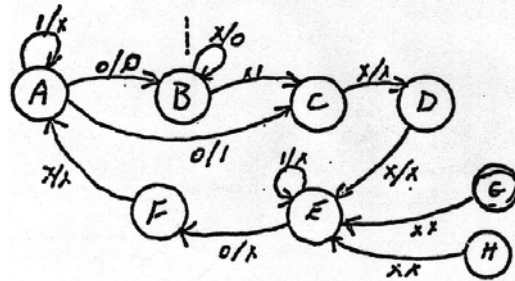| Q2Q1 \ Q0 UP	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	1	1	0	1
10	0	0	0	1

$$D_1' = Q1\cdot\overline{Q0} + \overline{Q2}\cdot Q0\cdot UP + Q2\cdot Q0\cdot\overline{UP}$$

Q2Q1 \ Q0 UP	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	1	1	1
10	1	0	1	1

$$D_2' = \overline{Q1}\cdot\overline{Q0}\cdot\overline{UP} + Q2\cdot Q0 + Q1\cdot\overline{Q0}\cdot UP$$

8.) The first step in the problem is to decide on the necessary states. I used a Moore machine, and I assigned states for each part of the cycle. Note the use of two states for timing the yellow light on the NS road. I chose the bit pattern for the states to minimize the decoding of GNS, YNS, etc. and to prevent glitches on TMI.

State	Bits: $Q_2\ Q_1\ Q_0$	Action/Function
A	1 0 0	GNS = 1; wait 40 sec.
B	1 0 1	GNS = 1; wait for ETW
C	0 0 1	YNS = 1; first cycle of yellow on NS
D	0 1 1	YNS = 1; second cycle of yellow on NS
E	0 0 0	GEW = 1; wait 40 sec.
F	0 1 0	YEW = 1; one cycle only

$x/y = TMO/ETW$

State	Q_2 Q_1 Q_0	TMO	ETW	Next State	D_2 D_1 D_0	GNS	TMI
A	1 0 0	1	X	A	1 0 0	1	X
A	1 0 0	0	0	B	1 0 1	1	X
A	1 0 0	0	1	C	0 0 1	1	X
B	1 0 1	X	0	B	1 0 1	1	X
B	1 0 1	X	1	C	0 0 1	1	X
C	0 0 1	X	X	D	0 1 1	0	0
D	0 1 1	X	X	E	0 0 0	0	1
E	0 0 0	1	X	E	0 0 0	0	0
E	0 0 0	0	X	F	0 1 0	0	0
F	0 1 0	X	X	A	1 0 0	0	1
G	1 1 0	X	X	E	0 0 0	X	X
H	1 1 1	X	X	E	0 0 0	X	X

This group may be either 1 or 0 but there can be no transition within the group.

$$GNS = Q_2$$

$$TMI = \overline{Q2} \cdot Q1$$

$$D0 = Q2 \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{TMO} + Q2 \cdot \overline{Q1} \cdot Q0 + \overline{Q2} \cdot \overline{Q1} \cdot Q0$$

$$D1 = \overline{Q2} \cdot \overline{Q1} \cdot Q0 + \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q0} \cdot TMO$$

$$D2 = Q2 \cdot \overline{Q1} \cdot ETW \left(\overline{TMO} + Q0 \right) + \overline{Q2} \cdot Q1 \cdot \overline{Q0}$$

9.) There are two identical gates interconnected. Transistors M1, M2,...M6 form one of them, a single compound gate with three inputs -- A, C, and QB (the output of the other gate) -- and one output -- QA. QA can be forced low by either a HIGH on QB (through M2) or by both A and B being HIGH (through M1 and M3 in series). Thus

$$\overline{QA} = QB + A \cdot C \quad \Rightarrow \quad QA = \overline{\left(QB + A \cdot C \right)}$$

The whole system is:
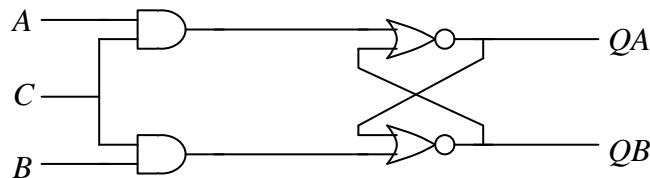
This is a clocked RS flip-flop!

Since QA changes value every 10^{-7} sec, its period is $2 \cdot 10^{-7}$ sec and the frequency is $5 \cdot 10^{+6}$ Hz. For each gate, $P_D = f_C \cdot C \cdot V_{DD}^2 = 5 \cdot 10^6 \cdot 7 \cdot 10^{-14} \cdot 25 = 8.75$ μwatts.

For two such gates: P_D = 17.5 μwatts.

10.)   When A = '1', $V_{DS1} \le 0.8$ volts from the requirements of the problem and both transistors have $|V_{GS} - V_{TH}| = 4.1$ volts. Since V_{DS1} is less than $|V_{GS} - V_{TH}|/(1+a) = 4.1/1.4 = 3.0$ volts, the proper form for the drain current of M1 is

$$I_{D1} = \frac{W_1}{L_1} \cdot K_N \left(V_{GS1} - V_{THN} - \frac{(1+a)}{2} V_{DS1} \right) V_{DS1} = \frac{W_1}{L_1} \cdot K_N (5 - 0.8 - 0.56) 0.8 = 2.93 \cdot \frac{W_1}{L_1} \cdot K_N$$

Transistor M2 has $|V_{DS2}| = 5 - .8 = 4.2$ volts, which is greater than $|V_{GS} - V_{TH}|/(1+a) = 3.0$. Therefore:

$$|I_{D2}| = \frac{W_2}{L_2} \cdot \frac{K_P}{2(1+a)} |V_{GS2} - V_{TH}|^2 = \frac{W_2}{L_2} \cdot \frac{K_P}{2.8} |4.2|^2 = 6.2 \frac{W_2}{L_2} \cdot K_P$$

Equating the two drain currents gives:

$$2.93 \frac{W_1}{L_1} (2.5 K_P) = 6.2 \frac{W_2}{L_2} K_P \quad \text{which implies} \quad \boxed{\frac{W_2}{W_1} \cdot \frac{L_1}{L_2} = 1.18}$$

The gate threshold is the value of input, V_{GS1}, for which $V_{OUT} = V_{DS1} = V_{GS1}$.

Since the gate and drain voltages of M1 are equal, the current through it is

$$I_{D1} = \frac{W_1}{L_1} K_N \left(\frac{1}{2(1+a)} \right) (V_{GS1} - V_{TH})^2 = \frac{W_1}{L_1} K_N (0.37)(V_{GS1}^2 - 1.6V_{GS1} + 0.64)$$

For the P channel device, M2, I will assume that V_{OUT} at gate threshold is high enough that $|V_{DS2}| = 5 - V_{OUT}$ is less than $|V_{GS}-V_{TH}|/(1+a) = 3.0$ volts. (I will check the assumption after the calculation, of course.) Then

$$|I_{D2}| = \frac{W_2}{L_2} K_P \left(|V_{GS2}| - V_{THP} - \frac{1+a}{2}|V_{DS2}| \right)|V_{DS2}| = \frac{W_2}{L_2} K_P (5 - .8 - 0.7(5 - V_{OUT}))(5 - V_{OUT})$$

At gate threshold: $V_{THG} = V_{OUT} = V_{GS1}$ and $|I_{D2}| = I_{D1}$.

$$\frac{W_1}{L_1} 2.5 K_P (0.37)(V_{GS1}^2 - 1.6V_{GS1} + 0.64) = \frac{W_2}{L_2} K_P (4.2 - 3.5 + 0.7V_{OUT})(5 - V_{OUT})$$

Use the result that $\dfrac{W_2}{W_1} \cdot \dfrac{L_1}{L_2} = 1.18$ to get

$$0.88V_{OUT}^2 - 1.4V_{OUT} + 0.56 = 1.18(3.5 - 2.5V_{OUT} + 0.7V_{OUT}^2)$$

and $\boxed{V_{OUT} = V_{THG} = 3.4 \text{ volts.}}$

For A = HIGH, $I_{D1} = \dfrac{W_1}{L_1} \cdot K_N \left(V_{GS1} - V_{THN} - \dfrac{(1+a)}{2} V_{DS1} \right) V_{DS1} = \dfrac{W_1}{L_1} \cdot K_N (5 - 0.8 - 0.56)0.8$

Substitute $I_{D1} = 4.37 \cdot 10^{-4}$ amp and $P_D = I_D V_{DD} = 2.18$ mW. Assuming that on average the input will be high half the time, the ~~average power dissi~~pation becomes:

$$\boxed{P_D = 1.09 \text{ mW.}}$$

11.)   If B is LOW, then the tristate gate is in its high-impedance condition. The output will be forced HIGH by the P-channel MOSFET. When B is HIGH, the transistor is turned off and the inverter turned on. Thus $C = \overline{B} + B \cdot \overline{A} = \overline{B \cdot A}$ (a NAND gate).

In the circuit below, transistors M1 - M4 are a three-state inverter. Transistor M5 is the pull-up transistor shown explicitly in the problem. (Note: there are several ways to make a tristate inverter but all will have the same logical function when connected this way.)

VDD

$\overline{B}$ M4   M5

M3

OUT

A   M2

B   M1