Engineering 1630 - Fall 20176: Answers to the First Optional Problem Set

1.) The minimum expression is $OUT = \overline{A}\,\overline{B}\,\overline{C}D + A\overline{C}\,\overline{D} + BCD + \begin{cases} AB\overline{C} \\ ABD \end{cases}$ and the appropriate K-map is:

$AB \backslash CD$	00	01	11	10
00		1		
01			1	
11	1	1	1	
10	1			

There are two non-essential primes, only one of which has to be included in the minimized expression.

2.) The shortest possible Gray code sequence for four variables is 8. If you look at the K-map of problem one, you can see it requires traversing three states in one column to change both A and B. Similarly you have to traverse three columns to change both C and D. Shortest way to do both is a 3 x 3 path traversing 8 states. It is obviously possible to traverse all 16 boxes and if you look carefully you can find three intermediate sequences of 10, 12, and 14 states.

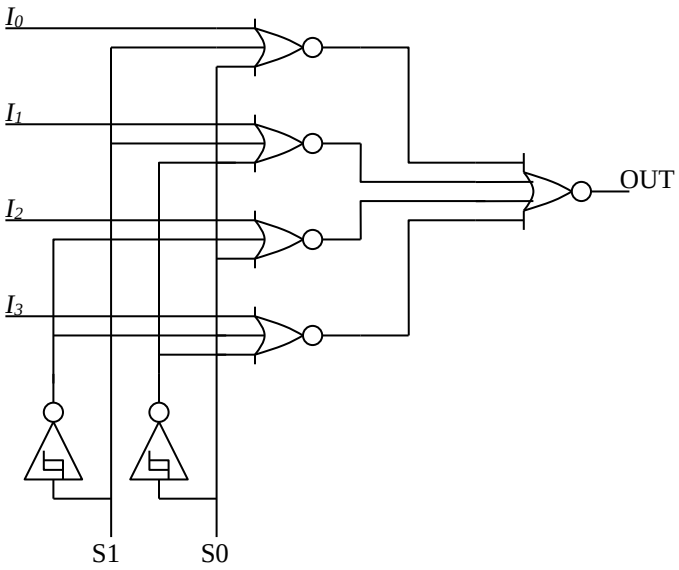
3.) The NOR multiplexor is very similar to the NAND-based mux and is drawn below. The primary difference is the polarity of the select signals at the 3-input NOR gates. They are the complements for the NAND case.

To derive this result systematically, notice that if you combine the outputs of a set of NOR gates in one more such gate, the output is a product of sums (POS) expression. Each sum has the inputs of one of the gates in the input set. For example,

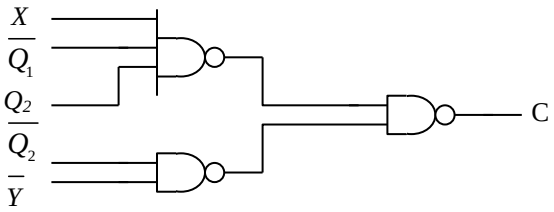
$$\overline{\overline{(A+B)} + \overline{(C+D)}} = (A+B)\cdot(C+D)$$

Therefore, to convert the multiplexor into NOR form, we need a POS expression for its output. The way to get such an expression systematically **for any system** is to form the complement of the output as an SOP form by summing all the Boolean terms that are not included in the original expression. The complement of that expression is the output itself, and using DeMorgan's theorems it can easily be pushed into POS form. (If the SOP form is minimum, then the resulting POS form will be too.) The problem with doing this in the multiplexor case is that there are 64 minterms for the inputs and only 32 of those contribute to the output. To catalog and minimize the remaining 32 terms by brute force is cumbersome. The simple way to do the problem is to observe that complementing the output of a multiplexor is the same as complementing all the I_n inputs because no matter which input is selected, selecting the complement of its I_n will give the same output as complementing the selected I_n itself. This finesses the problem of minimizing a complicated multi-input expression. Thus: $\overline{OUT} = \overline{I_0}\cdot\overline{S_1}\cdot\overline{S_0} + \overline{I_1}\cdot\overline{S_1}\cdot S_0 + \overline{I_2}\cdot S_1\cdot\overline{S_0} + \overline{I_3}\cdot S_1\cdot S_0$ and by applying DeMorgan's Theorems:

$$OUT = (I_0 + S_1 + S_0)\cdot(I_1 + S_1 + \overline{S_0})\cdot(I_2 + \overline{S_1} + S_0)\cdot(I_3 + \overline{S_1} + \overline{S_0})$$

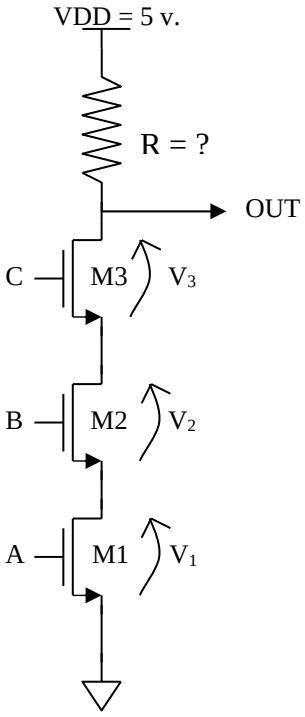


4.) $C = \overline{Y} \cdot \overline{Q_2} + X \cdot \overline{Q_1} \cdot Q_2$



5.) The circuit is as shown on the right. For each transistor, if one neglects the term in the square of V_{DS}, then

$$I_D = \frac{W}{L} K\left(V_{GS} - V_{TH}\right)V_{DS}$$



Because all three transistors have the same current and the same width to length ratio, we have:

$$\left(V_{GS1} - V_{TH}\right)V_{DS1} = \left(V_{GS2} - V_{TH}\right)V_{DS2} = \left(V_{GS3} - V_{TH}\right)V_{DS3}$$

Clearly the voltage from source to drain of any one transistor has to be less than .26 volts because the sum of the three must be .8 volts or less. Also, the transistor on the bottom will have the smallest voltage since it has the largest gate voltage. Suppose we guess that V_{DS1} = 0.2 volts and see if that is acceptable. The drain current is

$$I_D = \frac{W}{L} K\left(V_{GS1} - V_{TH}\right)V_{DS1} = 3 \cdot 7 \cdot 10^{-5} \cdot \left(4.1\right) \cdot 0.20 = 1.72 \cdot 10^{-4} \text{ amps.}$$

$V_{DS2}(5-.2-.9) = .2(5-.9)$ or $V_{DS2} = .21$

$V_{DS3} = .22V$

$V_{OUT} = V_{DS1} + V_{DS2} + V_{DS3} = .63$ V which is less than 0.8 by reasonable margin. Other slightly higher values are also possible.

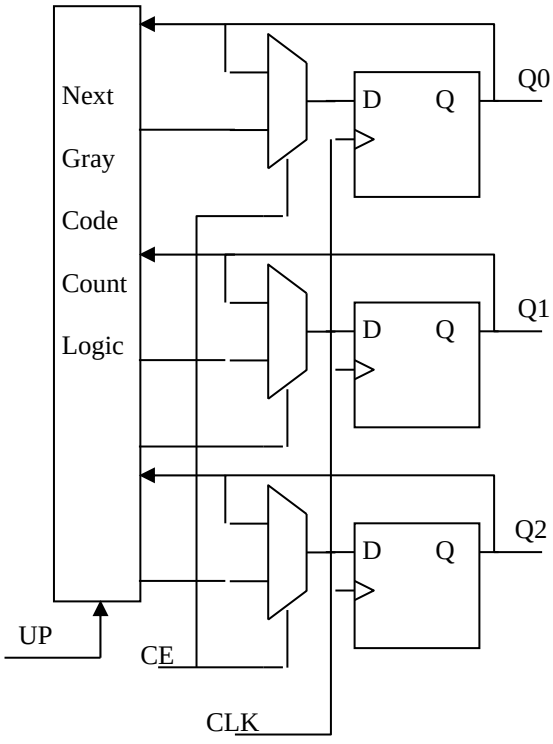
Finally, $R = \dfrac{(V_{DD} - V_{DS3})}{I_D} = \dfrac{5.0 - .63}{1.72 \cdot 10^{-4}} = 25.4$ Kilohms.

6.) This circuit can have glitches on D1 and D2. (The XOR was glitch free by definition.) All glitches are negative going and start a single propagation delay after the input transition. The possibilities I see are:

Before A B C	After A B C	Output Line	Glitch Width
001	110	D1	$1 \cdot \tau_P$
000	110	D1	$3 \cdot \tau_P$
010	110	D1	$3 \cdot \tau_P$
001	010	D2	$2 \cdot \tau_P$
100	010	D2	$2 \cdot \tau_P$
001	111	D2	$2 \cdot \tau_P$
100	111	D2	$2 \cdot \tau_P$

7.) Implement the CE (Count Enable) signal with a 1 of 2 multiplexor on the D line of each flip-flop. When CE = 0, the D's connect to the Q's. When CE = 1, the D's connect to the NEXT Q logic, which determines the count sequence. The state table is:

Q2	Q1	Q0	UP	$D'2$	$D'1$	$D'0$
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	1	0	0	0	1
0	1	1	1	0	1	0
0	1	0	0	0	1	1
0	1	0	1	1	1	0
1	1	0	0	0	1	0
1	1	0	1	1	1	1
1	1	1	0	1	1	0
1	1	1	1	1	0	1
1	0	1	0	1	1	1
1	0	1	1	1	0	0
1	0	0	0	1	0	1
1	0	0	1	0	0	0



Q2Q1 \ Q0 UP	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

$$D_0' = \overline{Q2}\cdot\overline{Q1}\cdot UP + \overline{Q2}\cdot Q1\cdot\overline{UP} + Q2\cdot Q1\cdot UP + Q2\cdot\overline{Q1}\cdot\overline{UP}$$

Q2Q1 \ Q0 UP	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	1	1	0	1
10	0	0	0	1

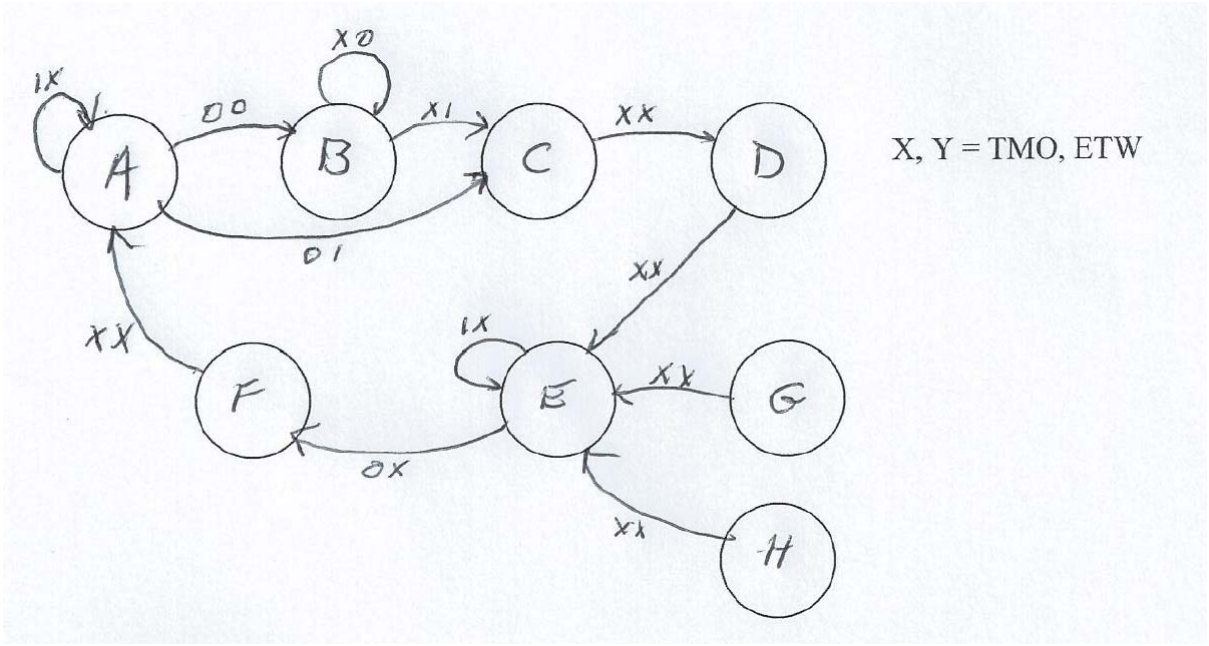
$$D_1' = Q1\cdot\overline{Q0} + \overline{Q2}\cdot Q0\cdot UP + Q2\cdot Q0\cdot\overline{UP}$$

Q2Q1 \ Q0 UP	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	1	1	1
10	1	0	1	1

$$D_2' = \overline{Q1}\cdot\overline{Q0}\cdot\overline{UP} + Q2\cdot Q0 + Q1\cdot\overline{Q0}\cdot UP$$

8.) The first step in the problem is to decide on the necessary states. I used a Moore machine, and I assigned states for each part of the cycle. Note the use of two states for timing the yellow light on the NS road. I chose the bit pattern for the states to minimize the decoding of GNS, YNS, etc. and to prevent glitches on TMI. Clearly this is not the only possible answer.

State	Bits: Q_2 Q_1 Q_0	Action/Function
A	1 0 0	GNS = 1; wait 40 sec.
B	1 0 1	GNS = 1; wait for ETW
C	0 0 1	YNS = 1; first cycle of yellow on NS
D	0 1 1	YNS = 1; second cycle of yellow on NS
E	0 0 0	GEW = 1; wait 40 sec.
F	0 1 0	YEW = 1; one cycle only



Pres. State	Q[2:0]	TMO	ETW		Next State	D[2:0]	GNS	TMI
A	100	1	X		A	100	1	X
A	100	0	0		B	101	1	X
A	100	0	1		C	001	1	X
B	101	X	0		B	101	1	X
B	101	X	1		C	001	1	X
C	001	X	X		D	011	0	0
D	011	X	X		E	000	0	1
E	000	1	X		E	000	0	0
E	000	0	X		F	010	0	0
F	010	X	X		A	100	0	1
G	110	X	X		E	000	X	X
H	111	X	X		E	000	X	X

This group of X's may be either 1 or 0 but there can be no transition within the group.

$GNS = Q_2$

$$TMI = \overline{Q2} \cdot Q1$$

$$D0 = Q2 \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{TMO} + Q2 \cdot \overline{Q1} \cdot Q0 + \overline{Q2} \cdot \overline{Q1} \cdot Q0$$

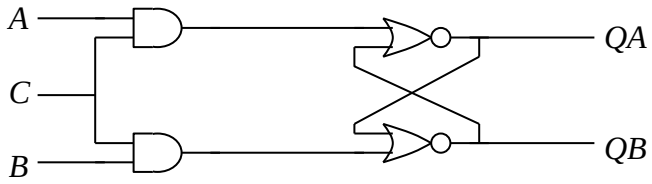
$$D1 = \overline{Q2} \cdot \overline{Q1} \cdot Q0 + \overline{Q2} \cdot \overline{Q1} \cdot \overline{Q0} \cdot \overline{TMO}$$

$$D2 = Q2 \cdot \overline{Q1} \cdot \overline{ETW} + Q2 \cdot \overline{Q1} \cdot \overline{Q0} \cdot TMO + \overline{Q2} \cdot Q1 \cdot \overline{Q0}$$

9.) There are two identical gates interconnected. Transistors M1, M2,...M6 form one of them, a single compound gate with three inputs -- A, C, and QB (the output of the other gate) -- and one output -- QA.

1. QA can be forced LOW by either a HIGH on QB (through M2) or by both A and B being HIGH (through M1 and M3 in series). Thus $\overline{QA} = QB + A \cdot C \quad \Rightarrow \quad QA = \overline{(QB + A \cdot C)}$. Equivalently, the output can be pulled HIGH by LOW on QB and a LOW on either A or C, that is, $QA = \overline{QB} * (\overline{A} + \overline{C}) = \overline{(QB + A \cdot C)}$ where the second equal sign is the application of DeMorgan's theorems.

2. The whole system is an RS flip-flop:



3. Since QA changes value every 10^{-7} sec, its period is $2 \cdot 10^{-7}$ sec and the frequency is $5 \cdot 10^{+6}$ Hz. For each gate, $P_D = f_C \cdot C \cdot V_{DD}^2 = 5 \cdot 10^6 \cdot 7 \cdot 10^{-14} \cdot 25 = 8.75$ μwatts. For two such gates: P_D = 17.5 μwatts.

4. To make a master-slave FF from these RS flip-flops, requires using two such flip-flops in tandem. To convert the RS inputs of the master to a D input requires an inverter between S, the D-input, and R. (As drawn above, if QA is the Q output of the flip-flop, then A is the R or reset input.) To activate the slave on the falling edge of the clock, requires a second inverter. The two RS flip-flops use 12 transistors and the inverters use 4 more for a total of 16.

5. Let W_{MIN} be the minimum manufacturable width of an NMOS transistor. Then the width of M1 is W_{MIN} and the widths of M2 and M3 are $2W_{MIN}$. The PMOS transistors always conduct in some series connection, the worst case of which is when only one of M5 or M6 conducts along with M4. Because they are PMOS devices, their widths must be multiples of $2.5 \cdot W_{MIN}$. Thus the widths of M4, M5 and M6 are $5 \cdot W_{MIN}$ each.

10.) When A = '1', $V_{DS1} \leq 0.8$ volts from the requirements of the problem and both transistors have $|V_{GS}-V_{TH}| = 4.1$ volts. Since V_{DS1} is less than $|V_{GS}-V_{TH}| = 4.1$ volts, the proper form for the drain current of M1 is

$$I_{D1} = \frac{W_1}{L_1} \cdot K_N \left(V_{GS1} - V_{THN} - \frac{1}{2} V_{DS1} \right) V_{DS1} = \frac{W_1}{L_1} \cdot K_N \left(5 - 0.8 - 0.32\right) 0.8 = 3.1 \cdot \frac{W_1}{L_1} \cdot K_N$$

Transistor M2 has $|V_{DS2}| = 5 - .8 = 4.2$ volts, which is greater than $|V_{GS}-V_{TH}| = 3.0$. Therefore:

$$|I_{D2}| = \frac{W_2}{L_2}\cdot\frac{K_P}{2}|V_{GS2}-V_{TH}|^2 = \frac{W_2}{L_2}\cdot\frac{K_P}{2}|4.2|^2 = 8.82\frac{W_2}{L_2}\cdot K_P$$

Equating the two drain currents gives:

$$3.1\frac{W_1}{L_1}(2.5K_P) = 8.82\frac{W_2}{L_2}K_P \quad \text{which implies} \quad \boxed{\frac{W_2}{W_1}\cdot\frac{L_1}{L_2} = 0.88}$$

The gate threshold is the value of input, V_{GS1}, for which $V_{OUT} = V_{DS1} = V_{GS1}$.

Since the gate and drain voltages of M1 are equal, the current through it is

$$I_{D1} = \frac{W_1}{L_1}K_N\frac{1}{2}(V_{GS1}-V_{TH})^2 = \frac{W_1}{L_1}K_N(0.5)\left(V_{GS1}^2 - 1.6V_{GS1} + 0.64\right)$$

For the P channel device, M2, I will assume that V_{OUT} at gate threshold is high enough that $|V_{DS2}| = 5 - V_{OUT}$ is less than $|V_{GS}-V_{TH}| = 3.0$ volts. (I will check the assumption after the calculation, of course.) Then

$$|I_{D2}| = \frac{W_2}{L_2}K_P\left(|V_{GS2}| - V_{THP} - \tfrac{1}{2}|V_{DS2}|\right)|V_{DS2}| = \frac{W_2}{L_2}K_P\left(5-.8-0.5(5-V_{OUT})\right)(5-V_{OUT})$$

At gate threshold: $V_{THG} = V_{OUT} = V_{GS1}$ and $|I_{D2}| = I_{D1}$.

$$\frac{W_1}{L_1}2.5K_P(0.5)\left(V_{OUT}^2 - 1.6V_{OUT} + 0.64\right) = \frac{W_2}{L_2}K_P(4.2 - 2.5 + 0.5V_{OUT})(5-V_{OUT})$$

Use the result that $\frac{W_2}{W_1}\cdot\frac{L_1}{L_2} = 0.88$ to get

$$1.25V_{OUT}^2 - 2.0V_{OUT} + 0.80 = 0.88\left(8.5 + 0.8V_{OUT} - 0.5V_{OUT}^2\right)$$

and $\boxed{V_{OUT} = V_{THG} = 2.94 \text{ volts.}}$

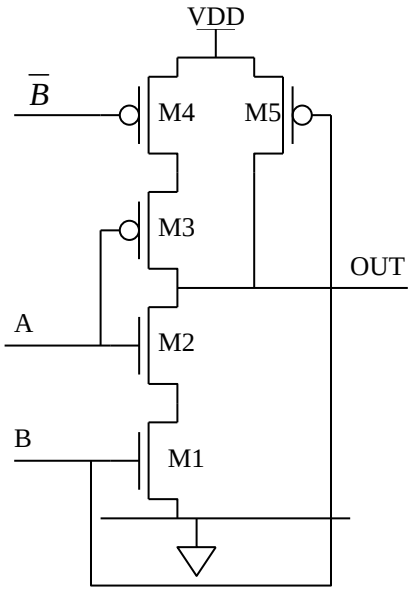
For A = HIGH, $I_{D1} = \frac{W_1}{L_1}\cdot K_N\left(V_{GS1} - V_{THN} - \frac{1}{2}V_{DS1}\right)V_{DS1} = \frac{W_1}{L_1}\cdot K_N(5-0.8-0.64)0.8$

Substitute $I_{D1} = 5.98\cdot10^{-4}$ amp and $P_D = I_D V_{DD} = 2.99$ mW. Assuming that on average the input will be high half the time, the average power dissipation becomes:

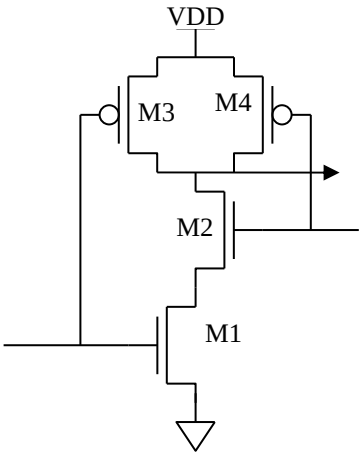
$$\boxed{P_D = 1.5 \text{ mW.}}$$

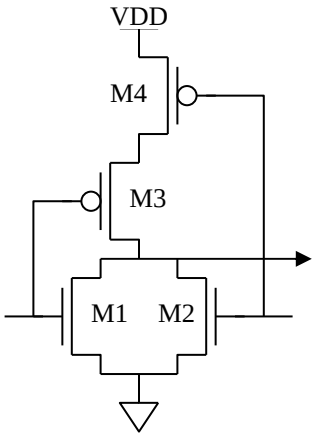
11.) If B is LOW, then the tristate gate is in its high-impedance condition. The output will be forced HIGH by the P-channel MOSFET. When B is HIGH, the transistor is turned off and the inverter turned on. Thus $C = \overline{B} + B\cdot\overline{A} = \overline{B\cdot A}$ (a NAND gate).

In the circuit below, transistors M1 - M4 are a three-state inverter. Transistor M5 is the pull-up transistor shown explicitly in the problem. (Note: there are several ways to make a tristate inverter but all will have the same logical function when connected this way.)



12. To do this problem you need the configurations of the NAND and NOR static gates. Here they are with NAND on the left:





1. When transistors are properly sized, all minimum gates have the same drive current. If we neglect the self-capacitance of the NAND gate, then when loaded by a single minimum width inverter it too will have a 15 ps delay. A 4X drive inverter has 4 times the input capacitance of a minimum inverter so the NAND delay will be 4*15 = 60 ps.

2. Let C_{MIN} be the gate capacitance of a minimum width NMOS transistor. In the manufacturing process of this problem, that means the total input capacitance of a minimum inverter is $3C_{MIN}$ because the PMOS device is twice the width of the NMOS. A 2-input NAND had the NMOS transistors each with twice the minimum width because of the series connection. The PMOS are also twice because of the mobility ratio. The

total input capacitance for one input is then $4C_{MIN}$. For the NOR gate with three inputs, the NMOS devices are each minimum width but the PMOS devices are 6X minimum width so each NOR input is $7C_{MIN}$. The total load for 2-NANDs, one NOR and 40 % wiring is $1.4(2\cdot 4+7)C_{MIN}$. The propagation delay is 15ps times 21/3 = 105 ps.

3. A 3-input NAND has NMOS devices with 6X minimum width because the output drive requires doubling the minimum size and the series connection requires another factor of 3. Similarly its PMOS devices are 4X so its input capacitance is $10C_{MIN}$. Total node capacitance is $1.4(2\cdot 7+10)C_{MIN} = 33.6C_{MIN}$. The propagation delay is 15 ps times 33.6/3 = 168 ps.