First Optional Homework Problem Set for Engineering 1630, Fall 2017

1. Using a K-map, minimize the expression:

$$OUT = \overline{A}\,\overline{B}\,\overline{C}D + A\overline{B}\,\overline{C}\,\overline{D} + ABCD + AB\overline{C}\,\overline{D} + \overline{A}BC\,D + AB\overline{C}D$$

How many non-essential primes are there in the K-map? How many included non-essential primes are there in the minimized OUT expression?

2. How many terms or elements does one of the shortest possible Gray code sequences in 4 variables have? All variables must change value at least once and the sequence must be closed, that is, start and end on the same term. (Try doodling on a K-map.) The longest sequence has 16 terms. How many different lengths of sequences are there with intermediate between the longest and shortest?

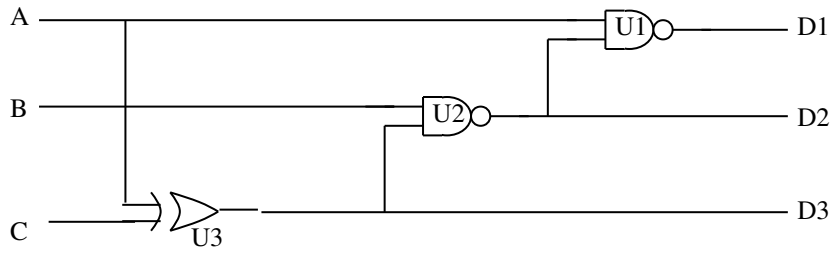
3. Draw the gate-level circuit for a four input multiplexor using only NOR gates.

4. Simplify the following expression and draw its gate-level circuit using only NAND gates:

$$C = \overline{X} \cdot \overline{Y} \cdot \overline{Q_1} \cdot \overline{Q_2} + X \cdot \overline{Y} \cdot Q_1 \cdot \overline{Q_2} + X \cdot Y \cdot \overline{Q_1} \cdot Q_2 + \overline{X} \cdot \overline{Y} \cdot Q_1 \cdot \overline{Q_2} + X \cdot \overline{Y} \cdot \overline{Q_1} \cdot \overline{Q_2} + X \cdot \overline{Y} \cdot \overline{Q_1} \cdot Q_2$$

5. Consider a three input NAND gate made with just N-MOSFETs and a resistor with V_{DD} = 5V. The transistors have parameters: $K_N = 7 \cdot 10^{-5}$ amp. per volt sq., $\frac{W}{L} = 3$, and $V_{TH} = 0.9$ volts. What resistor value is needed to make $V_{OL} \le 0.8$ volts. Sketch the circuit too. [The main difficulty in this problem comes from the slightly different gate-source voltages for each transistor in the series stack. To make the problem easier, neglect the term in the drain current proportional to $\frac{1}{2}V_{DS}^2$. That simplifies finding V_{DS}. You can do a problem like this by simulation if you have had ENGN162 or you can exploit the fact that it is a design problem with some latitude in values. The voltage across the grounded transistor has to be less than 0.8/3 so choose a value for V_{DS} a little lower than that and select the resistor to assure that. Then see if the output voltage meets the requirement.]

6. The circuit below has inputs, which always change essentially simultaneously, if they change at all. All input combinations are possible and so are all possible changes. Suppose the XOR gate is glitch-free but has a time delay of $2\tau_P$. All the other gates have delay, τ_P. Which output or outputs will have glitches? For each output susceptible to glitches, find at least one input transition that will cause a glitch and estimate how wide it will be in units of τ_P.



7. Design a three-bit Gray code counter with an Up/Down control line and a count enable (CE) line. Implement this with D - flip flops. (A Gray code is a binary sequence in which only one bit changes at each step of the sequence. The row or column markings of a K-map are an example. For the sequence in this problem, start off 000, 001, 011, 010.....) You may use three, one-of-two multiplexers for the count enable logic. Find the minimum logic needed to derive the Next D lines from the Q's and from the Up/Down line.

8. A traffic light placed at the intersection of a busy north-south (N-S) road with a lightly traveled east-west (E-W) road is connected to a sensor which detects traffic waiting on the east-west road. The sensor asserts (sets to '1') a signal line ETW (East-west Traffic Waiting) when such traffic is present. The traffic light is supposed to respond to this signal and to a clock signal in its controller by operating the light according to the following rules:

    1. After turning on the NS green light, it will ignore ETW and wait for 40 seconds.

    2. North-south traffic continues to have a green light until there is east-west traffic waiting (i.e. ETW=1).

    3. The yellow light will be on for N-S traffic for TWO (2) clock cycles.

    4. E-W traffic has a green light for 40 seconds.

    5. E-W traffic then has a yellow light for ONE (1) clock cycle before N-S has green again.

The problem is to design a controller for this traffic light in the form of the block diagram shown below. This is a finite state machine with the slight twist that one of its inputs (signal TMO, Timer Output) is the output of a monostable multivibrator or one shot (similar to the 74LS123 in your kit) which is used to time the 40 second intervals. The one shot responds to a rising edge at one input by immediately asserting an output for some set period of time independent of the subsequent history of the input. The signal line TMI (Timer Input) is an output of the next state logic which triggers the multivibrator on a low to high transition to begin a 40 second time interval. The D flip-flop between TMI and the multivibrator prevents glitches retriggering the one shot, that is, it prevents an edge on TMI from affecting the one-shot until the 40 sec time runs out. The timer output pulse itself clears the D flip-flop.

The system is to use three, edge triggered, D flip-flops, but will not need to use all the states. The state $Q_2 \cdot Q_1 \cdot Q_0 = 000$ is to be one of the states used. If the system should accidentally get to any unused state, it should make a transition to 000 immediately. The “light signal” outputs will consist of green, yellow and red light signals for the north-south traffic (GNS, YNS, RNS) and similar signals for east-west (GEW, YEW, REW). A given signal line should be at logic '1' when the corresponding light is lit. Questions:

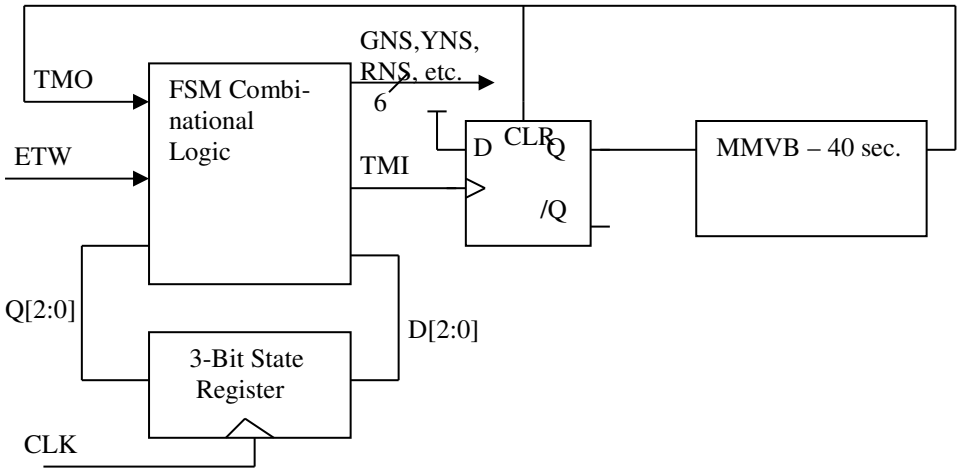
1. Make a table assigning particular conditions of the system to particular states of the flip-flops.

2. Make a state diagram of the system.

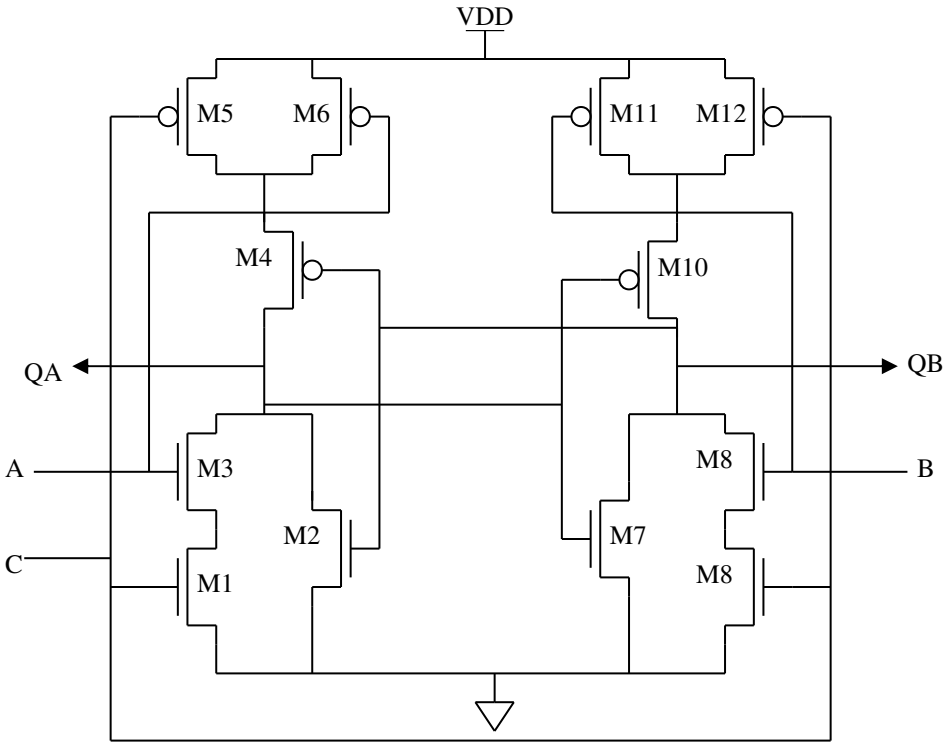
3. Make a transition table for the system showing the present state, the next state, the conditions of ETW and TMO which cause transitions, and the values which TMI and GNS should have for each combination of state and inputs.

4 Find Boolean expressions for D_2, D_1, D_0, TMI, and GNS in terms of Q_2, Q_1, Q_0, ETW and TMO.

5. Draw a gate implementation of the logic for TMI.



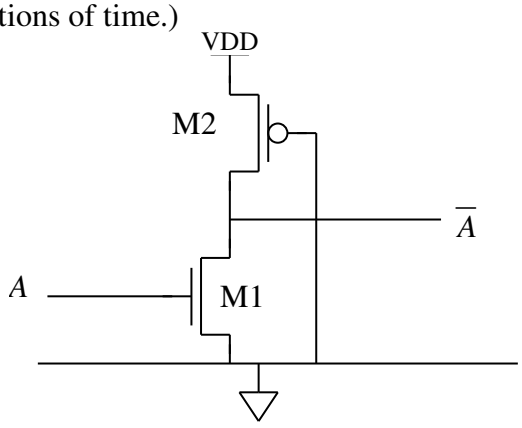
9. The circuit below is designed in static CMOS logic. Transistors M1, M2,....M6 form a single gate with inputs A, C, and QB.



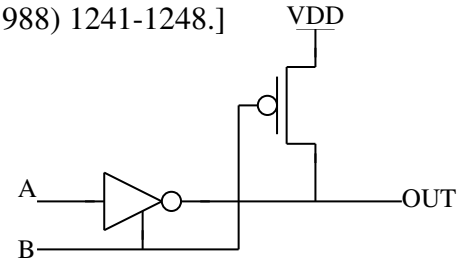
1. What logic function is implemented in this gate?
2. Draw a gate-level schematic, that is, replace the transistor version with standard gate symbols. What is the overall circuit?
3. If the capacitances at nodes QA and QB are both .07 pf. (which is typical of the levels actually encountered), what is the power dissipation if the inputs make Qa change state roughly at 10 MHz.? (The mean period of Qa is 200 ns and its mean frequency is 5 MHz. For comparison, one half of a 74LS74, which is not the same thing but which has some similarity, dissipates 10 mw. with essentially no change in power up to its limit of operation which is about 20 MHz.)
4. How many transistors would it take to make a master-slave flip-flop based on the partial design in this problem?
5. Suppose that the ratio of electron mobility to hole mobility and hence the ratio of PMOS to NMOS currents under the same voltage conditions is 2.5:1. (This is typical of devices with L > 100 nm and many things are still made at that scale.) Suppose also this is to be built with minimum size gates, what are the transistor sizes relative to minimum width N-channel devices?

10. For a given level of technology, a pure NMOS logic gate with a pull up resistor (or transistor) is sometimes faster than a conventional CMOS implementation. This is partly because the load capacitances driven by the output of a gate do not include the input capacitance of P channel devices in the next gate. The tradeoff is much higher power. For certain critical paths on a complex chip, this extra speed may be worth the tradeoff. The circuit below is one way to implement such a gate in a CMOS system by having the P channel device turned on at all times.

Assume that the input high level is 5 volts. What is the ratio of the width of the P channel device to the N channel width that will insure that V_{OL} is less than 0.8 volts? (Assume that the thresholds of the two device types are both 0.8 volts, that $K_N = 2.5 \cdot K_P = 7 \cdot 10^{-5}$ amp/V^2.) What is the **gate threshold** for this circuit? (I defined the "gate" threshold to be the value of input voltage to a gate at which the input and output voltages are equal.) If $\frac{W}{L} = 3$ for the N channel device, what is the power dissipation of this inverter? (Assume that the input is high and low for roughly equal proportions of time.)



11. The circuit below is a simple gate realized in an unusual way. What Boolean function does it realize? Draw the complete actual transistor version of the circuit. In doing so, assume that both B and its complement are available as inputs. [This type of gate has some advantages in certain circumstances because when embedded in a large system, it is easier to test for manufacturing faults. For a discussion of this issue, see M. Katoozi and M Soma, IEEE JSSC 23 (Oct. 1988) 1241-1248.]



12. In class I made an approximate argument that for custom on-chip logic, the propagation time, rise time and fall time of a logic gate are all proportional to the total capacitance on the output node of the gate. This was a similar to the argument in chapters 4 and 5 of Dally and Harting but did not depend on Ohm's law or the linearity of the transistors. In the simplest of circumstances, I ignored the effect of the self-capacitance of the gate on its output load capacitance. For a given manufacturing process, I expressed propagation time as a multiple of that of a minimum size inverter driving another such gate, τ_{MIN}. Let K_P be the ratio of electron to hole mobility which is the same at the PMOS width to NMOS width in an inverter. This makes the input capacitance of the minimum inverter $(1+K_P)C_{MIN}$, where C_{MIN} is the gate capacitance of a minimum size N-channel inverter. [I believe I used C_{MIN} to refer to the input capacitance of the minimum size inverter in class today (11/8/17). That didn't affect the result that a tree of 2-input multiplexers might often beat out a tristate bus for overall propagation delay at not too large a penalty in area. Sorry to confuse you without meaning to.]

You usually know by simulation what this minimum time is, so for the propagation time of a gate: $\tau_P \simeq \tau_{MIN}\left(\frac{C_{LOAD}}{(1+K_P)C_{MIN}}\right)$. Notice that only a capacitance ratio matters so we do not need exact values to estimate times under load. To the same degree of accuracy, the load capacitance C_{LOAD} is proportional to the total of all widths of all transistors connected to the output of the gate. The coefficient of proportionality is roughly independent of channel type or input/output side. Wiring capacitance may increase the load capacitance in the obvious way. To keep the rise and fall times symmetric, devices have to be scaled so that the pull-up and pull down currents are the same. This meant scaling PMOS widths by K_P and series connected devices by the number of devices in the series connection.

Suppose you are building something in a process for which the P to N width ratio of an inverter is $K_P = 2.0$. When additional transistors are connected in series in a gate, they must be wider by a factor of the number of series-connected devices to keep the current drive the same as the inverter. Multiple parallel devices are the same as the inverter size for that transistor type. You need to know

which gate types have series N-channel devices and which have P. A minimum size inverter in this process has a delay of $\tau_P = 15$ ps with one minimum inverter load.

I showed you the configuration of NAND and NOR gates in class and that is also in both the recommended text books.

1. What is the propagation time of a 2-input NAND gate loaded by an inverter with 4X the drive current of a minimum inverter in this process? [Hint: assume the transistors have been properly scaled that minimum gates have the same transistor currents as the transistors in the minimum inverter.]
2. Calculate the propagation time of a 2-input NAND gate when it is driving two 2-input NANDs and one 3-input NOR. Assume the wiring capacitance is about 40 % the total capacitance of the total gate input capacitances. (This is a common problem on-chip. Wiring capacitance is not negligible.)
3. Suppose the load were changed to 2 3-input NOR gates and one 3-input NAND that has 2X drive current, what would the delay become? Make the same assumption about wiring capacitance as above.