Instructions for Downloading and Testing Lab B and C

Loading compiled bit files to the XC3S500E evaluation board (applies to both labs):

- Follow the usual procedure to synthesize, fit, and place and route a Verilog-based design in the Xililnx Project Navigator. This is identical to what you have been doing for your CPLD designs. The only difference is targeting for the XC3S500E-FG320
- Open iImpact and double click on Boundary Scan. Right click on the blue text in the middle of the right pane and choose to initialize the chain. (You are not using the usual programming cable so the circuit is not found automatically.) The program should report finding three Xilinx components, one of which is the FPGA. Follow the prompt to verify the FPGA identity
- Right click on the FPGA symbol, choose Set Configuration File, and browse to the .BIT file in your Xilinx project directory. Assign that bit file to the FPGA. Right click on the FPGA again and choose "Program" to download the file.

Lab B:

Lab B is self testing. The music should start as soon as the file is downloaded and be readily recognizable. Remember that the switch settings can stop play so be sure to check those before despairing. There may be some confusion about the correct position of those switches, particularly the clock control switch, the rightmost one. That needs to be up or 1. Two of the setups have speakers without amplifiers and rely on an amplifier built into the support board. (You can tell the difference by whether the speaker plugs into the FPGA board or the support board.) For the board-based amplifier to work, the four dip switches in the upper right corner of that board must be in the up position.

Lab C:

The test software for Lab C is on the P:\ drive at P:\programs\MentorGraphics\TestSoftware\Lab_C. It is a single executable file that opens a console window with instructions for entering strings to write to your sign when you run it.