ENGN1630 – Digital System Design
Semester I, AY 2019-20
M, W 3:00pm-4:20pm

CLASS TIMES:	MW 3:00 – 4:20 p.m.	Barus & Holley 153
INSTRUCTOR:	R. Iris Bahar	CIT 449
	863-1430	Iris_Bahar@brown.edu
	Office Hours:	Mon. 4:30 – 5:30 pm, ERC lobby
		Tuesday, 10 – 11am, CIT 449
		or by appointment
GRAD TAS:	Jiwon Choe	Pratistha Shakya
	Jiwon_choe@brown.edu	pratistha_shakya@brown.edu
	ERC 340 (open desk area 3rd floor, south)	
	Office Hours:	TBD

COURSE WEBSITE: www.brown.edu/Departments/Engineering/Courses/En163/home.html
Included on the website are schedules, lab changes, TA access information, hints on Verilog, class PowerPoints, etc.

COURSE DESCRIPTION: Fundamentals of digital logic design including: Boolean algebra, gates, truth tables, logic families, flip-flops, finite state machines, memory, and timing. More advanced topics include A-D conversion, binary arithmetic, CPU organization, programmable logic (CPLDs and FPGAs), and Verilog. Extensive laboratory requirement. Not open to first year students; permission required for sophomores.

COURSE OUTCOMES: This course presents a broad range of techniques useful for digital logic design. Students completing ENGN1630 should:

1. Be able to design combinational and sequential logic for a wide range of systems, including making appropriate allowances for timing constraints.
2. Be able to understand CMOS transistors and their use in logic circuits well enough to do timing, power, and load calculations, to use bidirectional buses properly, and to be prepared to study VLSI systems.
3. Be able to realize a logic design in an appropriate choice of discrete logic, a CPLD or an FPGA.
4. Be able to use CAD tools for schematic capture, logic simulation, and programmable design, and to understand the role and advantages of hardware description languages in design, particularly Verilog.

5. Be able to make use of memory and simple processors and to understand the idea of a register transfer machine.

WORK EXPECTATION: There are three hours per week of class for 14 weeks (42 hours). I ask questions of you during class expecting some response, which means I expect your minds to be working during class. There are both a mid-term and a final exam. The preparation for each would normally require about 8 hours of study and review (16 hours). The primary way you demonstrate mastery of the material of the course is through completion of the lab challenges. Those have point weightings depending on the difficulty of the lab and it takes 62 points to pass the course. It will usually take about 2 hours of study and lab work to earn a point. The total is 42+16+124 = 182 hours.

TEACHING ASSISTANTS: While we have several seniors who took the course last year who have committed to be TAs (and should be very good at the job), we have not yet worked out their schedules. Overall, we should have 25-35 hours of lab staffing per week. We will post the hours, names, and schedule of all the TAs on the class website shortly. You are not limited to their hours for working, but you do need to work with one of them for evaluation of your work on each lab.

LABORATORY SPACE: The lab will be in the Hewlett Electronics Lab on the first floor of Giancarlo (B&H, room 196). The computers in room 196 have been updated with the latest software from Mentor Graphics, Xilinx, and Aldec. However, you should let me or a TA know if you encounter any problems with the software.

LABORATORY HOURS: Hours will start on Thursday, Sept. 12th, if all goes well. The exact hours when TAs will be available are still to be determined as they work out their schedules. The class website will show TA hours as soon as they are settled. Eventually, we will have the lab itself open 20 hours a day during the week and much of the weekend, but there will only be TA coverage for about 30 hours.

LABORATORY GRADING: There are a total of 14 lab assignments available in this course. Your lab grade is based on the number of labs you complete (there is no partial credit on lab grades). Instead, you will receive points for each successfully completed lab. Please see the lab manual for the point distribution for each lab. You need a minimum of 57 points to pass the lab part of the course. While there is no set due date for any particular lab, we have clustered lab assignments into groups with due dates:

GROUP 1: labs 0-3, due by Sunday, October 6

GROUP 2: labs 4-9, due by Sunday, November 17

GROUP 3: labs A, B, due by Friday, December 6
GROUP 4: labs C, D, due by Friday, December 13

COURSE GRADING: To pass the class, you must have passing grades on both the exam and lab parts of the course. Following is a tentative breakdown for the course grading:

Laboratory Assignments	55%	
Midterm Exam	15%	(in class, date TBD)
Final Exam	25%	(Friday, December 20, 9am-noon)
Class Participation	5%	

LABORATORY MANUAL/KIT: The lab manual and kit will be available together for a fee of $60 from George Worth (B&H 325). There will be a rebate of $50 through the Controller's Office after the end of the semester if you return the major parts of the kit. The difference is a photocopying cost, which is a regrettable necessity. There are some slight changes to the manual this year. Please let me know if something there does not make sense. Last year's lab manual is on-line at the class web site and can be used until we get the new one printed.

TEXTBOOK: **OPTIONAL**: John F. Wakerly, *Digital Design: Principles and Practices, 5th Edition,* Pearson Higher Ed Inc., 2018. Unfortunately, the list price is $307. Because the course uses Verilog, we had to switch from another (cheaper) textbook that is now based on VHDL. Regardless, the course does not follow a single textbook closely, thus purchase is optional. While the textbook is useful, the lectures and lab manual may be enough to get you through the course.

TOPICS: We roughly plan to follow Prof. Patterson's course outline from past years:

1. Boolean algebra, logic minimization, Sum-of-Product/Product-of-Sum forms, Karnaugh maps.
2. MOSFET transistors, static logic circuits, noise margins, signal levels, open-drain and 3-state circuits, flip-flops.
3. Transistor-level design of logic gates
4. Sequential circuits and finite state machines with counters and special cases.
5. Floating gate devices and their use to build CPLDs and non-volatile memory.
6. Logic programming in Verilog hardware description languages as used to synthesize simple circuits.
7. Basic CAD for schematic capture and programmable device programming.
8. Register transfer machines and very simple models of computer structure.
9. Semiconductor memory: SRAM, DRAM, ROM – asynchronous and synchronous
10. Field Programmable Gate Arrays (FPGAs) for logic implementation
11. Arithmetic: adders, fast carry methods, simple multiply, number representation (2's complement integers, offset binary, IEEE 754 floating point standard)

COLLABORATION: The lab manual has a statement on the class collaboration policy, some of which we repeat here to emphasize what I expect. Generally:

1. You may collaborate on labs by discussing them with your classmates and to some extent with the TAs. The TAs are supposed to give hints or debug suggestions but not to tell you how to do the lab. Please don't push them to exceed these bounds. If the lab manual seems vague in some places, that is deliberate. The point is that you need the exercise of working to understand the problem as well as working out for yourself the possible choices for its solution. In giving or taking advice this way, it is important to be sure you understand the problem and its solution. You may get stumped when questioned by a TA and end up losing credit for the lab if you prove clueless about how it is supposed to work.
2. In all design labs, you must build, debug and demonstrate the system on your own boards yourself – your own fingers, parts, documentation, etc. TAs will check board numbers and have the right to ask for documentation, that is, the schematic or outline material that you used to guide assembly. This includes data entry for any Verilog code. Type it yourself, not copying someone else's file. Offering someone else's work for this is NOT allowed. Precisely because it is hard to detect that sort of cheating, we will deal with it harshly should we detect it.
3. For the written reports for labs 2, 6, and 9 or schematic capture, you must take the data and write the report yourself. There is a requirement that a TA certify that he/she saw you take the data or demonstrate the results of lab 9. **We take a particularly harsh view of copying data or even two people taking data together and using copies for their reports.** Data is a certification that you did the measurements, and right or wrong this is what you got. Science and engineering depend on the reliability of that sort of certification for progress. Mistakes in data are normal but fakes or copies are strictly forbidden. In the "real" world the penalty for plagiarism is often ostracism. Consider: http://www.bostonglobe.com/news/science/2014/08/05/author-retracted-stem-cell-paperscommits-suicide/PjUPxOBh3k2qnGPIzQMwHL/story.html
4. If in a written report you choose to copy some picture or text to explain your work, **you must explicitly attribute that material to its source** with a footnote, not just in a bibliography. You cannot copy from Wikipedia and paste it into the report and expect us not to notice. You must write the report yourself subject to the usual limits on quotation and we recommend generating the figures yourself too – you learn more that way.

DIVERSITY & INCLUSION: It is our intent that students from all diverse backgrounds and perspectives be well-served by this course, that students' learning needs be addressed both in and out of class, and that the diversity that the students bring to this class be viewed as a resource, strength and benefit. It is our intent to present materials and activities that are respectful of diversity: gender identity, sexuality, disability, age, socioeconomic status, ethnicity, race, nationality, religion, and culture. Your

suggestions are encouraged and appreciated. Please let me know ways to improve the effectiveness of the course for you personally, or for other students or student groups. Likewise, I expect all students in class to be respectful of diversity and do their part in creating an inclusive environment for all in the classroom and the laboratory. Again, I would appreciate any suggestions for improving the learning environment in the lab with regard to student-student, student-TA, or student-professor interaction.