ENGN1600: Design and Implementation of VLSI Systems
Final Project

The final project for the course includes a full custom layout design appropriate for a 3 week assignment, typically done in groups of 1-3 people. The topic for your project may be one from the list below, or other appropriate topic of your choice. You are encouraged to relate the project to your own research interests, but it should not repeat a prior design you have done. Regardless of your choice, the topic needs to be approved by me ahead of time. The project must include schematic and full custom layout of your design, along with functional and timing simulation and power dissipation analysis. The criteria for good design is minimum area, minimum timing (clock frequency), as well as minimal power dissipation. Often, these are at odds, so some compromises will have to be made. The final project includes a project proposal, final report and a presentation.

Project Proposal
Due: Wednesday, November 23, by noon

Project proposals should be 2-4 pages in length. One proposal per team is sufficient. The proposal should include:

1. The names of the team members working on the project.
2. The project title as well as a one paragraph description of your design.
3. A rough description of how you intend to implement your design: what type of architecture (e.g., complementary CMOS, dynamic logic, transmission gates or any combination, sizing, timing, power constraints, etc.).
4. In your proposal, specify clearly the role of each team member in the project and describe how your team intends to divide the work.
5. Reference to at least one published article related to your design project.

Status Report
Due: Wednesday, December 3, by 5pm

Hand in a short written report (one per team) on progress of the project. Please include the following:

1. A high-level sketch of your design (may be hand drawn).
2. Expected outcomes.
3. A discussion of any preliminary results.
4. A more detailed description of how the group intends to divide the work among the team members.

Project Presentation
Date: Tuesday, December 13, 9am−12pm

This is the scheduled day of the final. The presentations should be 15–20 minutes long and should cover how the project was divided among the group members, particular challenges with the project, discussion on implementation, simulation results, and validation. The presentation should be fairly formal (i.e., with polished slides). All team members are expected to take part in the presentation. Attendance for all the presentations is mandatory for everyone in class.

Final Report
Due: Thursday, December 15, by 5pm

The final report (one per team) should refer back to the original project proposal. The report should include:

1. A reference to at least two published articles related to your design project (at least one of the articles must be less than 5 years old). You do not need to implement a specific design described in the papers, but the articles should in some way provide you with some new insight on the main design topic beyond what was covered in class.
2. A functional as well as architectural description (include some discussion of how and why it may differ from your project proposal description).
3. Color printouts of the layout design as well as waveforms to prove functional correctness. In addition, schematic and layout files should be emailed to me and Marco.
4. All figures, diagrams, layouts or waveforms should be clearly labeled and include a written description.
5. You should also describe your design choices, the alternatives you considered, your testing methodology, as well and any problems you encountered, and any anomalies.
6. For each block in your design include a functional description and a list of inputs and outputs.
7. Your report must include an analysis of your design in terms of area, timing (worst-case path delay) and dynamic power dissipation (static power analysis is optional). Analysis should include the tradeoffs at the conceptual level. In addition, timing analysis must include simulations using Calibre and area measurements should be obtained directly from layout.

A FEW WORDS ABOUT SIMULATIONS:

Simulation of a huge layout is going to require *a lot of time and patience*. Your final layout will contain **thousands** of transistors and past experience shows that it can take **N-hrs** ($1 \leq N \leq \infty$) for your design to simulate depending on the complexity of the design. There are a few *smart* things you can do to try and make your design simulate in some *finite* time.

a) Cut down on the number of input excitations. Choose a few reasonable input vectors to show that your design works. **DO NOT** try to simulate your layout for *all* possible input combinations.

b) Simulate your design in modules as you go along. This will save you a lot of pain if you need to debug your final layout.
c) In order to avoid having errors that might be hard to fix when you finish your project, double-check the correctness of each module by running DRC and LVS at each step of your design.
d) Large structures that include multiple instances of the same cell (i.e., memory arrays) can be simulated at the schematic level by representing the capacitance of multiple cells with one large lumped capacitance. In this way, you can get an idea of the timing behavior of your structure without instantiating every single element in the structure.
e) Think about the overall floorplan of your design before you begin putting all your modules together in layout. Pitch matching can be quite important. Leaving space for routing can also save you a lot of time and aggravation down the line.

Some project suggestions:

- Pipelined adder or other fast adder implementation
- Comparison of ripple carry adder vs. carry skip adder in terms of area, speed, and power
- N-bit Arithmetic Logic Shift Unit
- $N \times N$ Bit Pipelined Parallel Multiplier
- Magnitude Comparator — designed 2 different ways, or with 2 different logic styles
- An 8 word, 16 bit multi-port FIFO register file
- K-bit (16 rows by 16 bit) SRAM
- A fully associative memory array (requires CAM and SRAM logic)
- 8-bit Divider
- SECDED (single error correction, double error detection) logic
- An 8 entry by 16 bit instruction issue queue
- Comparison of leakage power dissipation for designs with and without sleep transistors (activates high V_{th} by using the stack effect when circuit is in idle mode).
- Layout of a datapath for a simple 8-bit processor
- Arithmetic unit that calculates accumulated sum, maximum input and minimum input of a stream of 8-bit numbers
- Vending machine or some other complex state machine.
- Design a neuron functional unit used in a deep neural network.
- We briefly touched on several different types of latches and dynamic logic (e.g., DCVS). Do a comparative study of these different designs to understand better their performance, power, and reliability benefits/weaknesses. Susceptibility to noise may be a particularly interesting aspect to explore.

The project complexity should match with the number of people on the team. That is, the larger the design team, the more complex I expect your design to be. Also note that this is not intended to be a complete list. You are encouraged to propose your own project idea (but please make sure you get my OK before delving into it).