A 56-mW 23-mm^2 Single-Chip 180-nm CMOS GPS Receiver With 27.2-mW 4.1-mm^2 Radio

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***Abstract*—A 56-mW 23-mm^2 GPS receiver with CPU-DSP-64 kRAM-256 kROM and a 27.2-mW 4.1-mm^2 radio has been integrated in a 180-nm CMOS process. The SoC GPS receiver, connected to an active antenna, provides latitude, longitude, height with 3-m rms precision with no need of external host processor in a [−40, 105] °C temperature range. The radio draws 17 mA from a 1.6–1.8-V voltage supply, takes 11 pins of a VFQFPN68 package, and needs just a few passives for input match and a crystal for the reference oscillator. Measured radio performances are NF = 4.8 dB, Gp = 92 dB, image rejection > 30 dB, −112 dBc/Hz phase noise @ 1 MHz offset from carrier. Though GPS radio linearity and ruggedness have been made compatible with the co-existence of a microprocessor, radio silicon area and power consumption is comparable to state-of-the-art stand-alone GPS radio. The one reported here is the first ever single-chip GPS receiver requiring no external host to achieve satellite tracking and position fix with a total die area of 23 mm^2 and 56-mW power consumption.**

***Index Terms*—GPS receiver, low power dissipation, system-on-chip (SoC).**

I. Introduction

THE integration of the single-chip CMOS GPS receiver prompted several CMOS design effort so far [1]–[6]. The target has been recently achieved [7]–[9] and single-chip CMOS GPS receivers are now ready to enter the mass market. In this work, an optimization of an 180-nm GPS SoC reported in [7] is described. In particular, with respect to [7], DC power consumption has been reduced to 27.2 mW by optimizing voltage-controlled oscillator (VCO) design and the radio has been made more rugged in order to extend operating temperature range up to [−40, 105] °C. Furthermore, a digital calibration of an external crystal has been introduced to allow use of an inexpensive crystal as a reference oscillator. The SoC GPS receiver reported here features 2-kV human body model (HBM) and 175-V machine model (MM) electrostatic discharge (ESD) protection [10].

In this paper, besides the RF improved performance, circuit and calibration techniques that allowed successful integration of the SoC GPS receiver are detailed. In fact, analog RF and digital baseband on the same die present serious noise problems for the sensitive radio. Techniques used to achieve co-habitation are described, including designing overload-tolerant RF stages with fully differential interconnection, using RF compatible packages, minimizing digital off-chip signals such as buses, choosing a frequency plan where processor harmonics cannot enter the IF stages, and implementing an isolation zone between the RF and baseband sections of the silicon. The issue of RF radio and CPU co-existence is made more challenging by the physical characteristic of the GPS signal that is 19 dB below thermal noise floor in its band: this radio needs to withstand noise and spurious signals generated by the on-chip microprocessor at much higher levels than thermal noise and, consequently, GPS signal.

The paper is organized as follows. In Section II, an overview of the SoC is given, more specifically, radio architecture with requirements for CPU co-existence and an overview of the used baseband. Circuit and calibration techniques are described in Section III. Implementation details are given in Section IV and experimental results in Section V. Discussion of results and comparison with the state of the art is reported in Section VI. Conclusions on the potential of RF CMOS or mainstream CMOS for GPS applications are reported in Section VII.

II. SoC Overview and Architecture

A. SoC Overview

An overview of the SoC GPS receiver is reported in Fig. 1. The required external components are an active antenna, a filter, a crystal oscillator, and a few passive components for input match and supply bypass capacitances.

The chip is fed with the GPS L1 signal from an active antenna, via the external RF filter. This allows remote placement of the antenna from the receiver itself and relaxes noise requirements.

The combination of external low noise amplifier (LNA) and GPS receiver brings the output signal (thermal noise and GPS data) to a level sufficiently high to overcome offset and noise of the 1-bit analog-to-digital (A/D) converter. A 1-bit solution has been used since the $4f_0$ (where $f_0 = 1.023$ MHz) IF sampled signal is basically thermal noise (GPS signal is at least 20 dB lower, as detailed in next section). Compared to a multi-bit solution, 1-bit sampling simplifies the IF section (i.e., allows use of a limiter after the IF filter) and simplifies the A/D and baseband with just 2-dB loss in signal-to-noise (S/N) ratio [11].

The A/D samples the $4f_0$ analog signal with a $16f_0$ clock: the 1-bit data stream is processed by the baseband, which calculates NMEA GPS coordinates and provides them off-chip via a serial connection.

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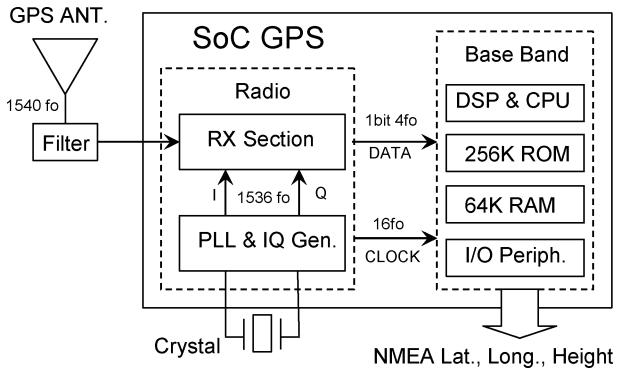

Fig. 1. SoC GPS and required external components.

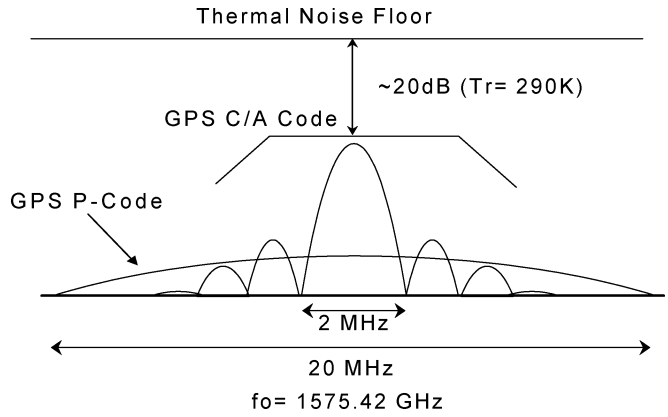

Fig. 2. GPS C/A and P-code spectrum.

B. Radio Architecture for GPS Signal

The GPS satellites broadcast signals at −130 dBm in a 20-MHz-wide band centered at 1.57542 GHz. The GPS signal code is a direct-sequence spread-spectrum signal where data are modulated onto the carrier such that the transmitted signal has a larger bandwidth than the information rate of the data.

Two DSSS signals are broadcast in the 20-MHz band centered at 1.57542 GHz: the P-code (precision code) and the C/A (coarse acquisition code) (Fig. 2).

For consumer applications, only the GPS C/A code is of interest: in this case, most of energy is located in a 2-MHz band. Received power is −130 dBm at the antenna of the GPS receiver. In the 2-MHz band of the GPS C/A code, where most of the energy is, the noise power KTB is −111 dBm, with an associated S/N ratio at the antenna of −19 dB.

For a consumer application, i.e., a high level of integration, zero IF (ZIF) or low-IF architecture must be selected. Given CMOS implementation (i.e., presence of flicker noise) and the nature of the GPS signal (where a significant amount of energy is contained at the center of frequency), a ZIF implementation is unpractical. For this reason, a low-IF architecture has been preferred for the front-end section. The use of a low-IF architecture calls for an on-chip image rejection. A block diagram of the radio is shown in Fig. 3.

As far as the choice of IF frequency, this results from a tradeoff between two conflicting requirements.

- Gain∗bandwidth product of the amplifiers in the IF section. In order to reduce power dissipation of the IF filter, it would be desirable to reduce IF frequency.
- Flicker noise corner frequency of the mixer. This one imposes a lower limit to the IF frequency since 1/f noise of the mixer contributes to the total noise figure of the receiver.

In our case, the optimal tradeoff is IF $= 4f_0$. The LNA–mixer combination has −29-dBm input 1-dB compression point, therefore, the use of a low-quality RF filter is enough to prevent blocking of the RX chain from UMTS and GSM carriers.

A 25-dB image rejection provided by the GPS radio relaxes the noise requirement of the LNA.

The VCO oscillates at twice the required frequency and quadrature signals are derived by means of a divide-by-two. This solution has been preferred to a power-hungry VCO with RC polyphase *I/Q* generation and to a lower consumption *I/Q*

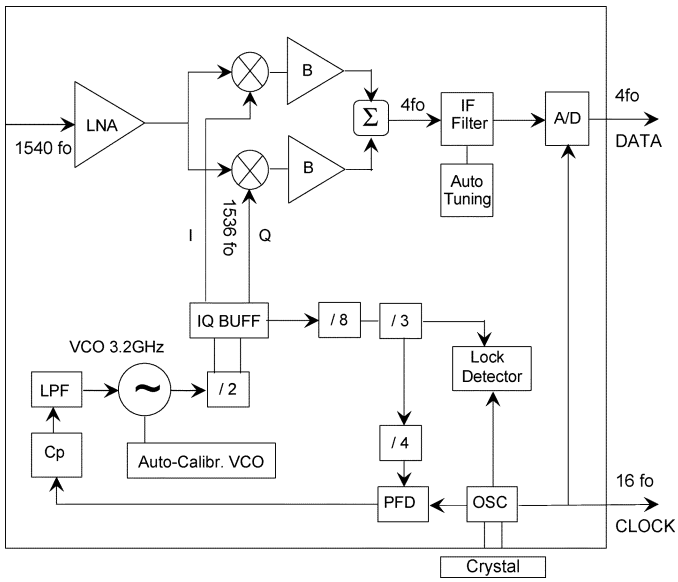

Fig. 3. Radio architecture.

VCO that would take more silicon area with respect to the preferred solution.

As far as frequency synthesizer specifications are concerned, no stringent requirements exist in terms of spurious levels and switch-on time for the applications. A single-loop phase-lock loop (PLL) with a low bandwidth can be used. This has the advantage of reducing spurious tones at the reference as well as the phase noise contribution due to the charge pump. A loop bandwidth of about 150 kHz has been chosen. The use of a low-bandwidth PLL calls for a low-phase noise VCO: an LC tank VCO has been used.

C. Frequency Planning

One of the strategies used to allow successful embedding of the GPS radio into an SoC is a careful frequency planning. This consideration led to the choice of an on-chip reference (and CPU master clock) at $16f_0$ since its high-order harmonics do not fall into the GPS band. High-order harmonics and their distance from the GPS signal is reported in Fig. 4.

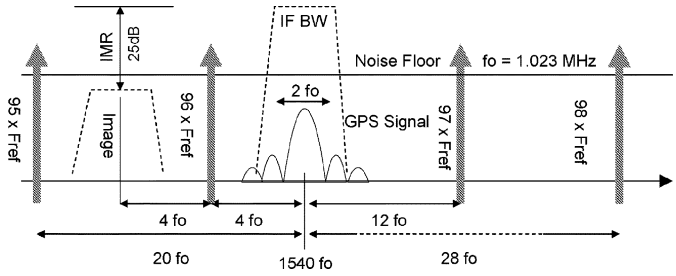

Fig. 4. GPS signal and high-order harmonics of clock.

TABLE I
GPS RADIO TARGET SPECS

	GPS Radio Target Specs	Unit
RF Frequency	1.575	GHz
Conversion Gain	> 90	dB
NF	< 6	dB
S11	< -10	dB
IF Frequency	4.092	MHz
IF Filter BW	< 2	MHz
P1dBin at LNA-MIX	> -30	dBm
P1dBout at LNA-MIX (Peak-Peak)	> 1	Vpp
P1dBout at IF Filter (Peak-Peak)	> 1.5	Vpp
Image Rejection IR	> 25	dB
In-Band Phase Noise Floor	< -80	dBc/Hz
Total Tuning Range	> 250	MHz
K_{VCO}	< 50	MHz/V

D. Radio Architecture for Microprocessor Co-Existence

The target specifications for a radio capable of operating in an SoC hostile environment are reported in Table I.

With respect to a stand-alone radio (i.e., a radio that is not integrated into an SoC), some parameters are more stringent, mainly dynamic range and VCO sensitivity to pulling.

As far as dynamic range is concerned, this can be important also in a stand-alone implementation if co-existence with other applications (such as GSM, UMTS, etc.) must be guaranteed. However, in our case ruggedness against interferers is a more severe problem: a microprocessor running GPS satellites tracking and positioning SW generates high- and low-frequency spurious signals that may harm radio RF performances. High-frequency spurious signals represent out-of-band RF blockers for the radio. These blockers can be significantly higher than the GPS signal since they are coupled at the input of the LNA, i.e., are not attenuated by the SAW filter (as in a stand-alone radio). Some of the higher order spurious can be identified and are reported in Fig. 4 with their relative position with respect to GPS signal and its image frequency. As far as low-frequency spurious signals, they may harm the IF filter section and the synthesizer.

As far as the synthesizer is concerned, low-frequency signals coupled by the VCO or PLL loop filter may pull the VCO. For this reason, K_{VCO} must be reduced to the maximum extent, which conflicts with required tuning range to compensate for processing spreads and temperature variation. It should be stressed that VCO pulling is not critical in a stand-alone GPS radio given the absence of a TX section.

As far as image rejection (IMR) is concerned, 25-dB IMR with $2f_0$ bandwidth are enough to avoid noise folding of the image frequency into the IF signal band. In addition to this requirement, in our case we have to consider the impact of high-frequency spurious: since the closest master clock harmonic is the 95th one, $12f_0$ away from the image signal (see Fig. 4), $2f_0$ IMR bandwidth is enough also for this SoC implementation. As far as the synthesizer is concerned, a reduction of the in-band phase-noise floor is desirable in order to reduce the risk of capturing (and down-converting into the IF signal band) high-frequency spurious generated by the baseband and propagated along the RF chain.

These considerations dictate the following radio requirements for SoC integration:

- fully balanced structures for improved noise rejection;
- narrowband LNA-mixer with large output P_{1db} (to cope with out-of-band blockers);
- narrowband auto-tunable IF filter with large output P_{1db} (to cope with in-band blockers);
- low K_{VCO} to reduce VCO modulation sensitivity;
- local bias circuitry for each building block;
- careful clocking strategy for sampled data and clocks generated by radio and propagated to baseband;
- careful supply and substrate isolation strategy;
- low phase noise of the synthesizer.

E. Baseband

The DSP delivers samples to the CPU after 62 μs of integration, giving a search bandwidth of 16 kHz in one pass for acquisition/cold start. After a satellite has been found and the oscillator calibrated, integration time switches to 1 ms, 1-kHz bandwidth, reducing the CPU load considerably. It tracks 12 satellites simultaneously, appearing to the software as 12 parallel channels, but in fact implemented at each stage with only the silicon needed to achieve the processing required for one channel. In fact, one numerical controlled oscillator (NCO) generates the independent frequency corrections for all 12 satellites. The CPU is an ARM7-TDMI and the I/O peripherals provided on the GPS SoC are reported in [10]. The SoC GPS has its on-chip standard GPS software (it is capable of operating in stand-alone mode with no need for an external host) with the added flexibility that customers can port their existing code. The SW mask ROM is a metal ROM, meaning that the programming is done only on the metal layers. The CPU is normally clocked at 16 MHz for a full GPS implementation.

There are 64 kB of SRAM on chip, with 256 kB of mask ROM. The SRAM has 4 kB in a separate block so that it can be battery backed, to store almanacs, ephemeris, position, and frequency information, in order that as a stand-alone GPS it features 3-second hot starts.

III. CIRCUIT IMPLEMENTATION

A. Low Noise Amplifier

Together with the DSP, the LNA sets a lower limit to the sensitivity of the system. It must be designed together with its ESD protection structures that typically worsen LNA performance. In Fig. 5, the CMOS LNA, the off-chip tuning inductor at the gate (L_G), the ESD structures and the parasitic capacitance at the input of M_{1a}–M_{1b} including the pad (C_{esd}) are depicted.

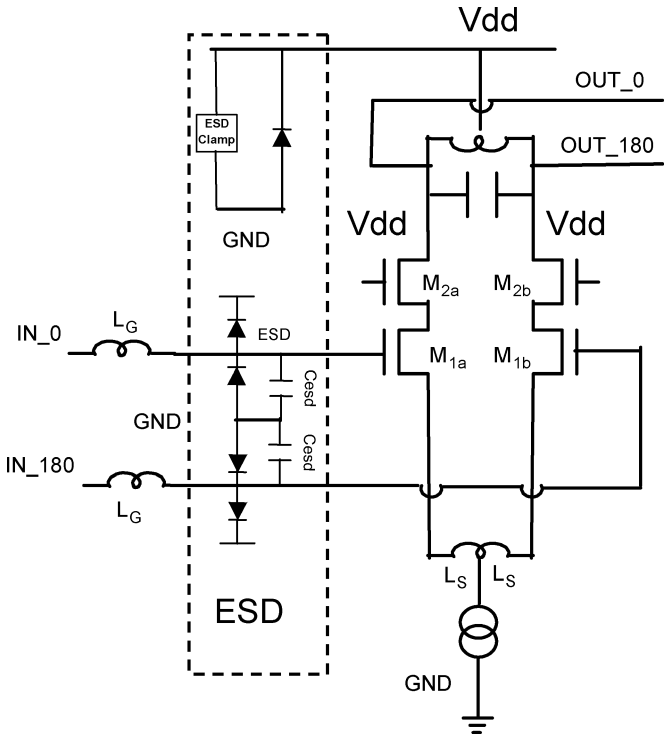

Fig. 5. LNA with ESD protection structures.

As far as the LNA is concerned, a single stage with on-chip degeneration has been used for reduced power consumption and improved linearity. For sake of simplicity, the impact of ESD structures (enclosed in dashed lines in Fig. 5) on input match and noise performances will be discussed later.

The cascode configuration improves the reverse isolation and reduces the Miller capacitance at the input of M_{1a}–M_{1b}. A 7-nH differential on-chip inductor with a quality factor $Q > 8$ tunes the output of the LNA. The 50-Ω input match is achieved with the combination of the on-chip inductor (L_S) and the off-chip inductor (L_G). The input impedance seen at the input of the LNA (IN_0 and IN_180) is

$$R_{\rm in}(f_0) = 2 \cdot \left[s \cdot (L_S + L_G) + \frac{1}{s \cdot C_{GS}(M_{1a})} + 2\pi \cdot f_T L_S \right] \tag{1}$$

where f_T is the cut-off frequency of M_1, L_S is on-chip inductive source degeneration, L_G is the off-chip inductor, $C_{GS}(M_{1a}) = C_{GS}(M_{2a})$ is the gate-source capacitance of MOS M_{1a} and f_0 is the operating frequency.

At the resonance frequency f_0, the input resistance is given by

$$R_{\rm in}(f_0) = 4\pi \cdot f_T L_S. \tag{2}$$

The input match is achieved making $R_{\rm in}(f_0) = 100\,\Omega$. A simplified expression of the noise factor that neglects the gate induced noise current and the non-quasi-static resistance $R_{\rm NQS}$ is [1]

$$F = 1 + \frac{2 \cdot (R_{LG} + R_{poly})}{4\pi f_T L_S} + \gamma(M1) g_{d0} \cdot 4\pi f_T L_S \cdot \left(\frac{f_0}{f_T} \right)^2 \tag{3}$$

where $R_{\rm poly}$ is the gate interconnects resistance of M_{1a}–M_{1b} that can be made negligible by using interdigitated structures. R_{LG} is the resistance associated with the tuning inductor L_G and g_{d0} is the zero bias drain conductance of M_{1a}–M_{1b}. The noise factor $\gamma(M_1)$ can be greater than 2 for short-channel devices operating in the saturation region due to "hot electrons" effect.

In our case, $R_{NQS} \ll 2\pi \cdot f_T L_S$, so it can be neglected. The gate-induced current noise has been taken into account in our simulations by using the MOS MODEL 9 [12].

The optimal sizing of M_{1a}–M_{1b} that minimizes the NF has been found by simulation and is equal to $140\ \mu$m/$0.18\ \mu$m.

The aspect ratio $\rm W_2/L_2$ of M_{2a}–M_{2b} has been driven by the following considerations: their thermal noise contribution increases when the ratio $C_d/g_{\rm m2}$ increases, where C_d is the total capacitance at the drain of M_{1a}–M_{1b} and g_{m2} is the transconductance of M_{2a}–M_{2b}. This would require minimization of C_d/g_{m2} i.e., large $\rm W_2/L_2$ (i.e., low value for $V_{gs}(M_{2a})$. However, since $V_{\rm ds}\ (M_{1a}) \cong V_{dd} - V_{gs}\ (M_{2a})$, this would imply an increase of $\gamma(M_1)$, i.e., an increase of noise contribution of M_{1a}–M_{1b}. The best value that reduces total noise figure (i.e., minimizes noise contributions of both M_{1a}–M_{1b} and M_{2a}–M_{2b}) has been found by simulation and is $\rm W_2/L_2 = 120\ \mu m/0.18\ \mu m$.

B. Impact of ESD Protection Structures

A typical ESD protection structure consists of a series resistance between the protected pin and the bond wire pad, plus two diodes connected between the protected pin and both ground and supply. For noise reasons, series resistance cannot be introduced and the arrangement shown in Fig. 5 has been used: diodes at the inputs of the LNA and an additional active clamp connected between supply and ground. Due to the presence of ESD structures, the input impedance at resonance is reduced according to the following expression [2]:

$$R_{\rm in}(f_o) \approx 2 \cdot \left[\frac{2\pi \cdot f_T \cdot L_S}{\left(1 + \dfrac{C_{\rm gate}}{C_{GS}(M_{1a})} \right)^2} \right] \tag{4}$$

where

$$C_{\rm gate} = C_{\rm esd} + C_{\rm miller}. \tag{5}$$

With respect to the situation with $C_{\rm gate} = 0$, 50-Ω match is achieved with a larger value of $4\pi \cdot f_T L_S$. This increases the contribution of the channel thermal noise to NF [see (3)] and reduces the available voltage gain. Another reason for the NF increase is the finite quality factor of the capacitances associated with ESD structures. However, a tradeoff between the effectiveness of the ESD protection structures and the LNA performance can be chosen: the two diodes feature the smallest possible capacitance allowed in order to protect the input pin up to $\pm$3-kV HBM pulses. The NF penalty incurred due to ESD structures has been evaluated at $\sim$0.1 dB.

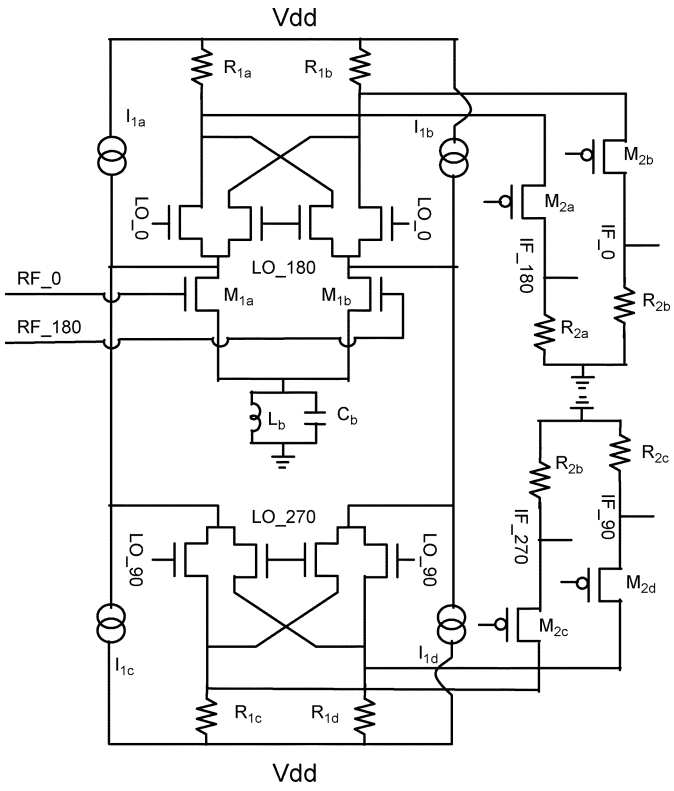

Fig. 6. Image rejection mixer.

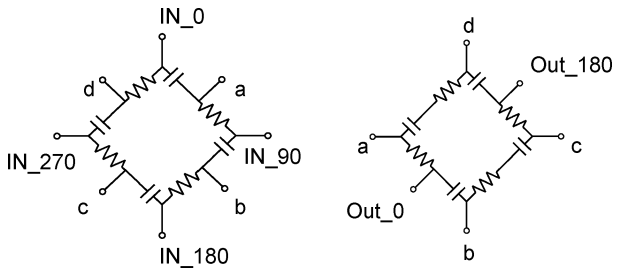

Fig. 7. IF combiner.

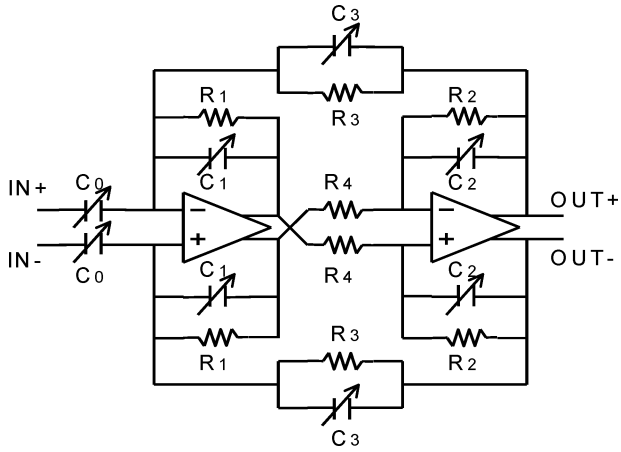

Fig. 8. Active RC filter.

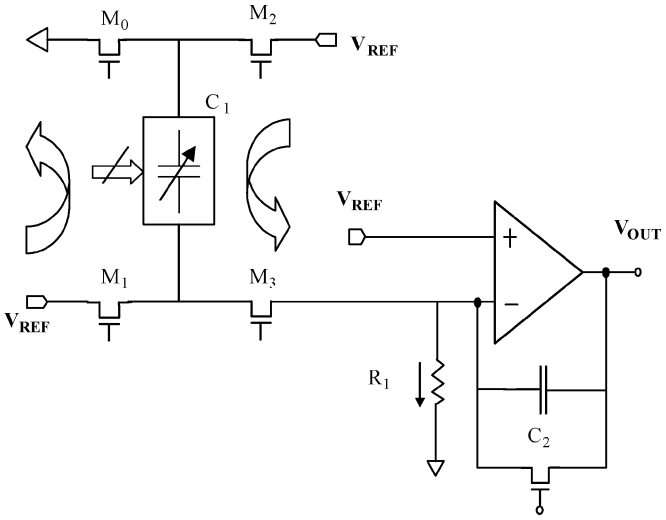

Fig. 9. RC filter auto-calibration machine.

C. Image Rejection Mixer

The image rejection mixer (Fig. 6) is directly connected to the LNA, i.e., its V–I converter composed of M_{1a}–M_{1b} is part of the LNA resonant load. It provides 4 *I/Q* signals (IF_0, IF_90, IF_180, IF_270) added into an IF combiner to provide image rejection. The Gilbert cell, stacked on top of the V–I converter, generates an IF current sourced by M_{2a}–M_{2b}–M_{2c}–M_{2d} and converted into a voltage swing across R_{2a}–R_{2b}–R_{2c}–R_{2d}.

Dynamic range is increased by this design solution and use of the L_bC_b tank that acts as a tail current generator. The reduction of the flicker noise corner frequency has been accomplished in the following ways:

- current mirrors I_{1a}–I_{1b}–I_{1c}–I_{1d} subtract DC current from Gilbert cell;
- R_{1a}–R_{1b}–R_{1c}–R_{1d} transconductor degeneration resistance.

The current mirrors I_{1a}–I_{1b}–I_{1c}–I_{1d} solve the tradeoff between 1/f noise of the Gilbert cell and thermal noise of the V–I converter, respectively increased and decreased when bias current increases. R_{1a}–R_{1b}–R_{1c}–R_{1d} do not contribute to 1/f noise and reduce 1/f noise of M_{2a}–M_{2b}–M_{2c}–M_{2d}. The IF combiner (Fig. 7) is driven by a 1-mA voltage follower.

The $4f_0$ IF frequency and the required bandwidth allow a realization with the cascade of two RC passive polyphase filters centered, respectively, at $3f_0$ and $5f_0$. A rejection of 30 dB across the 2-MHz band is achieved for $\pm 20\%$ RC time constant spread. The LNA-mixer combination feature NF $=$ 3.6 dB, Gain $=$ 34 dB, balanced output P_{1dB} (peak-to-peak) $=$ 1 Vpp and draws 4.2 mA.

D. Auto-Tuned IF Filter—Limiting Amplifier—1-Bit A/D

The IF filter implements a fourth-order transfer function with $4f_0$ center frequency and provides antialiasing function before the baseband A/D. It is based on the cascade of two similar bandpass cells (Fig. 8). An active-RC solution has been preferred to a lower power consumption *gm-C* approach to improve linearity and ruggedness versus interferers.

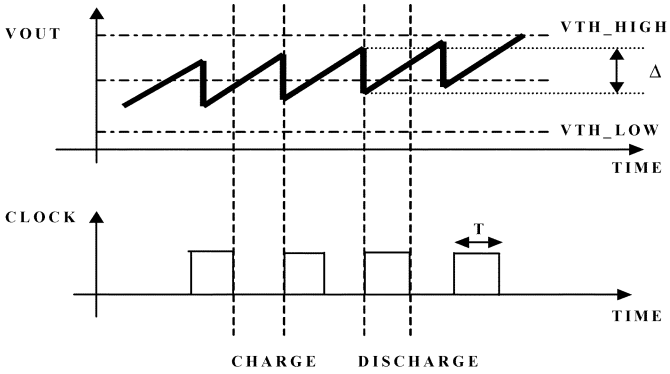

Fig. 10. $V_{\rm OUT}$ waveform.

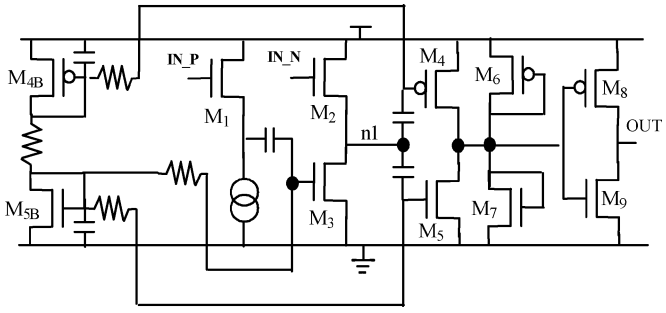

Fig. 11. ECL CMOS schematic.

The $2f_0$ bandwidth captures most of the GPS signal energy and filters out-of-band spurious signals, either down-converted by the LNA-mixer, or directly coupled by the substrate.

An auto-calibrating machine adjusts the filter RC time constants to track process and temperature variations. The principle of operation is the following. Referring to Fig. 9, capacitor C_1 and resistor R_1 represent a scaled replica of the IF filter RC cells; during the charge state (Fig. 10), capacitor C_1 will be charged to $V_{\rm REF}$ through M_0 and M_1, while the constant current that is drawn from R_1 will discharge the feedback capacitor C_2 generating a ramp at the output of the operational amplifier $V_{\rm OUT}$ with a slope proportional to $R_1 \cdot C_2$.

After a half clock period, equal to T, C_1 will be rapidly discharged through M_2 and M_3 causing an instantaneously decrease of $V_{\rm OUT}$, given from the following formula:

$$\Delta = V_{\rm REF} \cdot C_1/C_2. \tag{6}$$

The output ramp will increase the output voltage again since the discharge of C_1 will take place. Stable condition will be reached when

$$\Delta = \frac{V_{\rm REF}}{R_1 \cdot C_2} \cdot T \Rightarrow T = R_1 \cdot C_2. \tag{7}$$

If the time constant is different from the period T, the ramp will continuously increase/decrease its value reaching a threshold voltage; this information will then be used from the digital part of the auto-calibrating machine varying the value of capacitor C_1 through the word N (4 bits) in order to achieve stable condition. Every time the word N has to be increased/decreased, the feedback capacitor C_2 will be discharged through a shunt MOS in order to restart the cycle from $V_{\rm REF}$.

The IF filter and its auto-tuning machine draw 3.3 mA with a balanced output $P_{1\rm dB}$ (peak-to-peak) $= 1.6$ Vpp and a voltage gain of 38 dB. A limiting amplifier AC coupled to the IF filter provides additional 20-dB voltage gain to drive the latched 1-bit converter.

E. Frequency Synthesizer and I/Q Local Oscillator Signal Generation

The frequency synthesizer (see Fig. 3 for its block diagram) is fully integrated and generates *I/Q* signals to drive the image rejection mixer and the two clock signals needed by the baseband. *I/Q* generation is implemented by means of a VCO running at twice the LO frequency and of a divide-by-two stage, implemented with ECL-like dividers.

Since in a GPS radio there is no risk of LO pulling due to the TX section, it would be possible to generate *I/Q* signals with a quadrature VCO running at the same LO frequency, but the 2∗LO VCO approach has been used to reduce silicon area.

An *I/Q* Buffer block is used to drive both the *I/Q* mixer LO port and the feedback divider while maintaining *I/Q* 90 degrees phase shift accuracy. With reference to Fig. 3, the feedback divider is made of a CMOS dynamic divide-by-8 stage plus a CMOS static divide-by-12 stage. The divide-by-8 draws 800 μA and is realized as a cascade of equal CMOS dynamic divide-by-2 stages of the true-single-phase clock (TSPC) type [13] to minimize current consumption. In fact, the first divide-by-two draws only 100 μA at an input frequency of 1.57 GHz. However, these dividers need a CMOS signal at their input so an ECL-to-CMOS converter is interposed between the *I/Q* buffer and this block. In the adopted CMOS technology, this block is still feasible at a reasonable current consumption level (650 μA) with the circuit shown in Fig. 11.

The input differential signal (IN_P, IN_N) is first converted to single-ended at the node n1. The buffered IN_P signal drives the gate of M_3 acting as a common-source inverting stage. The IN_N signal is buffered by means of M_2 whose bias generator is replaced by M_3. With respect to a simple source follower, the addition of M_1–M_3 contributes to the generation of an output signal with equal rise and fall time at node n1. This signal is amplified by means of the AC coupled CMOS amplifier made of M_4, M_5, M_6, and M_7 that generates a 1-Vpp signal and buffered by the inverter M_8–M_9. The phase-frequency detector (PFD) is a CMOS implementation based on two edge-triggered D flip-flops with a delay on the reset path to avoid the dead zone. The charge pump consists of switched MOS mirrors optimized for flicker noise and matching at a switching speed compatible with the PLL input frequency (16.368 MHz). The charge-pump output current is generated starting from a bandgap reference current generator and is digitally programmable between 100–700 μA. In the typical setting (400 μA charge-pump output current), the DC current consumption of the charge pump and PFD is 550 μA (current consumption of PFD is negligible).

F. Integrated and Programmable Loop Filter

The passive loop filter is referred to a "quiet" ground to avoid the risk of unwanted VCO modulation. Similarly

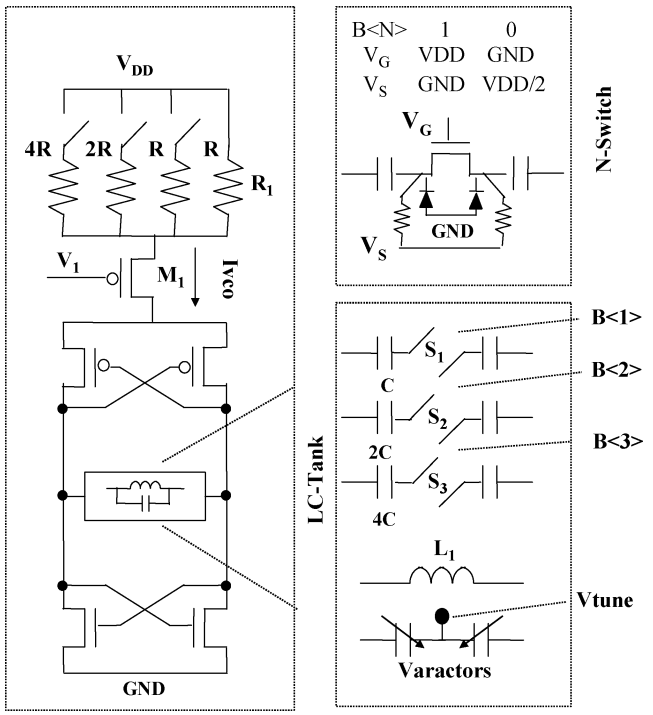

Fig. 12. VCO with frequency-amplitude digital calibration.

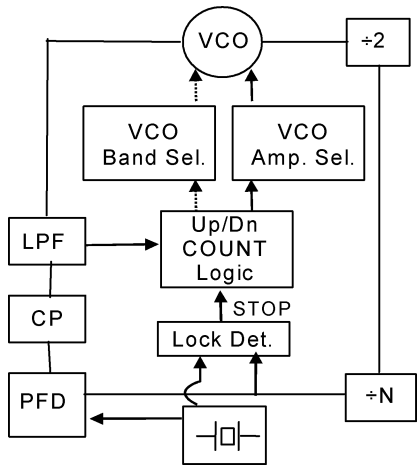

Fig. 13. VCO frequency and amplitude calibration machine.

to the charge pump, the PLL loop filter has been made digitally programmable to allow measurements of the synthesizer spectrum for different loop-filter and charge-pump current settings in the noisy SoC environment. The minimum and maximum achievable loop bandwidth are 70 kHz and 500 kHz, respectively. In the typical condition, a 150-kHz bandwidth is obtained for a nominal charge-pump current of 400 μA using a 700 pF/5k/50 pF loop filter and a $\mathrm{K_{VCO}}$ of about 50 MHz/V.

G. VCO: Digital Tuning of Frequency and Amplitude

The narrowband PLL requires a VCO with low phase noise, therefore an LC VCO has been preferred to a ring oscillator (Fig. 12). The need to improve robustness of the VCO against unwanted noise/spurious modulation calls for a reduction of the $\mathrm{K_{VCO}}$ that is conflicting with the required 25% total tuning range needed to compensate for temperature variations and process spreads. To address this issue, the total tuning range has been split into eight different overlapping sub-bands. The selection of the sub-band is made by means of an array of binary weighted capacitors. A total tuning range of 350 MHz is covered in this way with a reduced $\mathrm{K_{VCO}}$ of $\sim$50 MHz/V. A P+/N-well junction varactor in parallel to the integrated symmetrical octagonal inductor $L_1 = 1$ nH allows a fine tuning for each of the eight sub-bands. Parasitic capacitances of the coarse-tuning switch S_1, S_2, S_3 have been reduced by inversely biasing drain and source junction when the switch is in the off-state. The implementation is depicted in Fig. 12: with $B\langle N\rangle = 1$ the N-switch is in the on-state and $V_G = V_{\mathrm{DD}}$ and $V_S = \mathrm{GND}$. When the N-switch is in the off-state, i.e., $B\langle N\rangle = 0$, then $V_G = \mathrm{GND}$ and $V_S = V_{\mathrm{DD}}/2$. In this way, parasitic junction capacitances of the switch are reduced, and therefore, tuning range is extended.

The VCO features a digital amplitude calibration scheme: the bias current is changed by means of a bank of programmable resistors. Those resistors also act as degeneration resistances for the M_1 transistor, thus reducing 1/f noise of M_1 and its folding around the carrier. The state machine used for VCO frequency and amplitude calibration is shown in Fig. 13.

As far as amplitude is concerned, the machine works in the following way: at start-up the VCO is biased with maximum current and lock condition is verified. With the PLL in locked condition, VCO bias current is digitally reduced until the PLL unlocks. In this way, the minimum I_{VCO} current that keeps the PLL locked is identified, i.e., VCO running and capable of driving the 3.2-GHz dividers by 2. After the amplitude locking procedure is completed, the PLL is restarted with minimum $I_{\mathrm{VCO}}+1$ LSB bit current more in order to ensure lock condition even in the presence of temperature changes. The advantages of the VCO digital amplitude are the following.

- Since the peak detector is absent, there is no load at the tank, therefore, no tuning range reduction is incurred.
- 1/f noise associated with *analog* automatic gain control circuits is avoided.
- 1/f noise contribution of M_1 is reduced by the bank of resistances at its source, so their noise folding around the carrier. This is particularly important since the VCO is used in a narrowband PLL, i.e., synthesizer in-band phase noise is mainly due to VCO contribution. On the other hand, resistances introduce a thermal white noise inversely proportional to resistance R. Since 1/f noise reduction of M_1 is directly proportional to R, for any given VCO bias current it is possible to find the optimum value of R that minimizes VCO phase noise in the region of interest. In our case, we selected $R = 120\ \Omega$.

With respect to [7], in this design an optimization of the VCO allowed the reduction of its current consumption to 2.3 mA while extending at the same time the operating temperature range from $[-40, 85]\,^{\circ}\mathrm{C}$ up to $[-40, 105]\,^{\circ}\mathrm{C}$.

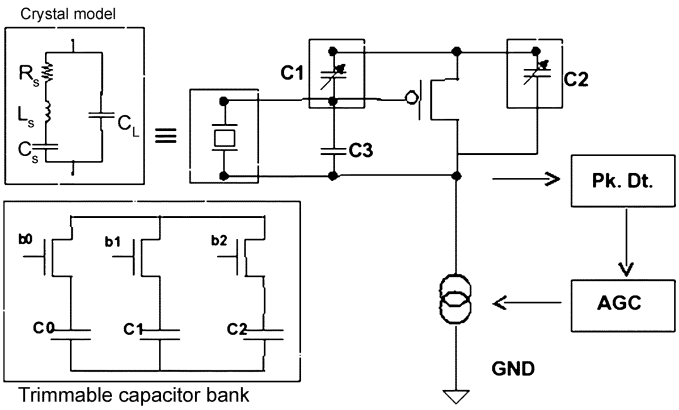

Fig. 14. Pierce oscillator.

H. Digitally Trimmable Crystal Oscillator

The $16f_0$ reference frequency is provided by an on-chip Pierce oscillator coupled to an AT-cut 16.368-MHz crystal (Fig. 14).

It draws 20 μA and additional 180 μA are needed in the following buffer. The oscillation frequency of the circuit is given by [14]

$$f_{asc} = \frac{1}{2\pi\sqrt{L_s \dfrac{C_s C_L}{C_s + C_L}}} \approx \frac{1}{2\pi\sqrt{L_s C_s}} \cdot \left(1 + \frac{C_s}{2C_L}\right) \quad (8)$$

where L_s and C_s are the resonator's motional inductance and capacitance, respectively, and C_L is the equivalent parallel capacitance dominated by C_1 and C_2.

The baseband requirements in term of reference accuracy are $\pm$50 ppm. This accuracy is mainly driven by the crystal accuracy and partly due to the spread of off-chip capacitances and on-chip and off-chip parasitic. In order to allow use of a low-quality crystal (i.e., with reduced requirements on accuracy), a possible strategy is to introduce an on-chip tuning strategy that allows the reference circuits to compensate for crystal variations. With respect to [7], in this work C_2 is implemented as a variable capacitor bank driven by a three-bits word. In this way, for a given set-up of external capacitances (i.e., a nominal reference oscillator), 10 ppm pulling from nominal frequency can be achieved by changing on-chip C_2 capacitance.

I. GPS Radio and SoC—Data and Clock Interfaces

The radio provides to baseband GPS data as a 1-bit $16f_0$ stream and a $16f_0$ clock. CMOS logic signals are converted in balanced currents, propagated across the die and transferred into a low impedance current-to-voltage converter incorporated into the baseband. The converter is placed into the silicon isolation area that separates the radio from the rest of the SoC and recovers CMOS logic signals that are propagated to baseband. The current-mode solution avoids charging and discharging long connection paths (with associated capacitances) with CMOS rail-to-rail signal that would inject high-order harmonics of the clock (i.e., interferers for the radio) into supply voltage, ground and substrate. The differential solution is easy to implement and reduces the magnetic field generated by currents switching across long metal paths.

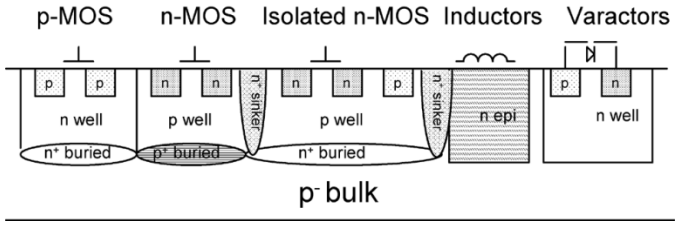

Fig. 15. Cross section of 180-nm RF CMOS.

IV. Implementation Details

A. Process

A triple-well 180-nm RF CMOS process with six metal levels, nMOS f_T in excess of 55 GHz and 10 Ω-cm substrate resistivity has been used. On-chip inductors with patterned ground shield and quality factor in the range of 6–8 at 1.6 GHz can be realized. NMOS transistors can be isolated from the p-substrate by means of an N+ region. Since this is an epi-process, the N+ region is significantly less resistive with respect to a conventional triple-well in non-epi CMOS processes, thus improving the isolation from the substrate. High-linearity 0.85-f_T/μm^2 MIM capacitances and highly resistive poly resistors are available from the device library. A schematic cross section of the process is shown in Fig. 15.

B. Package

The single-chip GPS has been housed into a standard 68-pin package (VFQFPN68), 11 of them used by the GPS radio. In order to save pin number and take advantage of the reduced parasitic inductance, critical RF signal ground pads have been directly bonded to the package ground slug. Conversely, noisy digital circuitry uses standard ground pads (i.e., separated from the ground slug).

C. SoC Floor Plan and Isolation of the Radio from Baseband

The layout of the single-chip GPS receiver is shown in Fig. 16. It uses 23 mm^2 including bond pads and has been defined with the help of substrate simulations. The adopted isolation strategy takes into account process and package.

The radio section measures 2.25×1.8 mm^2 without bond pads (Fig. 17). Differential inductors have been used with exception of the one used in the mixer. Highly resistive poly resistors and MIM capacitors have been used to design the RC cells for both the IF filter and auto-tuned machine in order to assure higher density and linearity.

The following countermeasures have been taken to improve the isolation of the GPS radio from the digital core.

- An empty silicon area separates radio and baseband.
- Radio and baseband have separate ESD rings that connect at one point.
- Patterned ground shields are introduced under inductors and bond wire pads.
- Each sensitive nMOS transistor in the radio has been separated by an N+ region from the substrate. The local ground has been taken separately to a pad, directly wire-bonded to the ground slug of the QFN package.

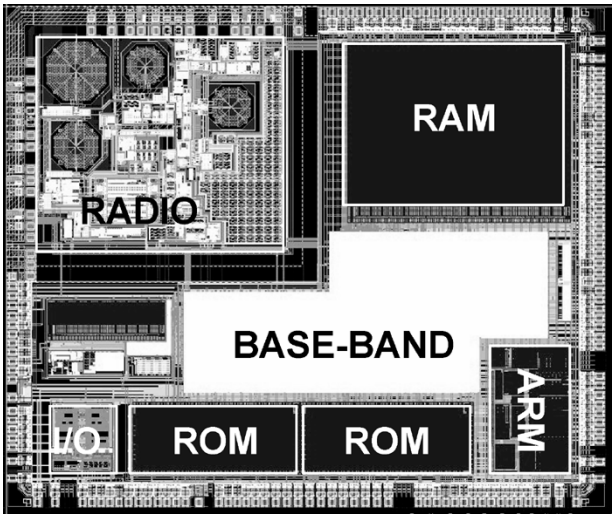

Fig. 16. SoC layout.

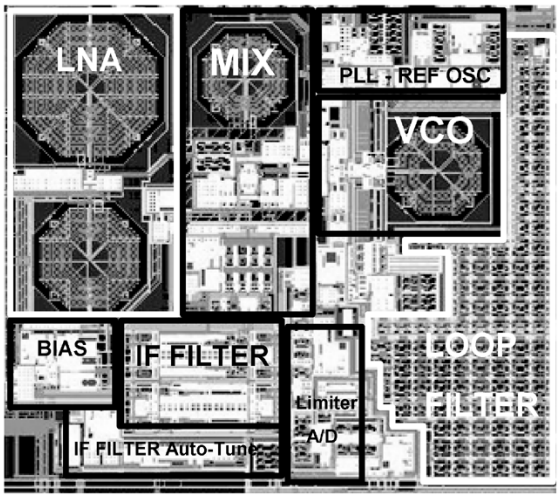

Fig. 17. GPS radio embedded into SoC.

- A careful radio floor plan has been used. The LNA and mixer are placed at the top left, away from the digital core. Thanks to VCO digital biasing and low K_{VCO}, the PLL loop filter and VCO are robust enough to be placed, together with the A/D and IF filters, closer to the digital core.

D. Application Board

A photograph of the RF application board for automotive applications, i.e., with ceramic protection filter, LNA, SAW filter, and reference crystal, is shown in Fig. 18. Passive capacitances needed to tune the crystal load, LNA input match, and supply voltage bypass have not been soldered in this board. While systems with an integrated antenna can omit the protection filter, experience shows that where there is an external antenna connector in the automotive environment, a filter that is robust to DC and ESD is required. The layout is in module format, to demonstrate the small size while allowing mounting on a demo board with power supplies, interfaces, and connectors. It also provides an artwork with all interfaces taken to the edge, so equipment manufacturers can re-use the layout directly on their own boards. For laboratory characterization, a board with access to test and measurement points on the silicon has been used.

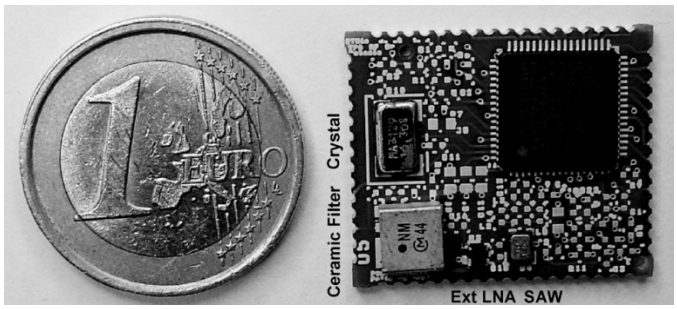

Fig. 18. Board layout for automotive application.

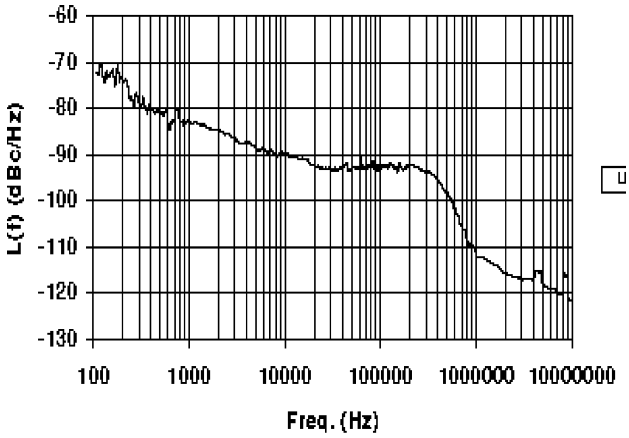

Fig. 19. Measured PLL phase noise with baseband turned off.

V. Experimental Results

A. Radio RF Parameters—Baseband Off

The SoC has been qualified for volume production between [−40, 105] and withstands up to 2-kV HBM and 175-kV MM [10]. The radio operates between [−40, 105] °C and in the typical condition draws 17 mA from a supply voltage in the 1.6–1.8-V range. Measurements have been done at the testing outputs before and after the IF filter with a balanced-to-unbalanced voltage buffer stage that drives the spectrum analyzer. The synthesizer phase noise, measured at the output of the LNA-mixer, is reported in Fig. 19 with baseband turned off. The thermal noise floor masks the PLL phase noise far away from the carrier. With baseband turned off, the IF filter output spectrum with a $1540 f_0$ RF tone applied at the input of SoC has been taken (Fig. 20). The RF tone is down-converted to $4 f_0$ and the thermal noise is shaped by the radio. A summary of radio measured parameters with baseband turned off is given in Table II.

B. Radio RF Parameters—Baseband On

In Fig. 21, the same plot is taken with on-chip CPU DSP running SW for satellite tracking and position fix. The intensive baseband processing increases the noise floor with the addition of spurious tones. The most important spurious are $16 f_0$ and the intermodulations between $16 f_0$ and $4 f_0$: $8 f_0$, $12 f_0$, $22 f_0$. With

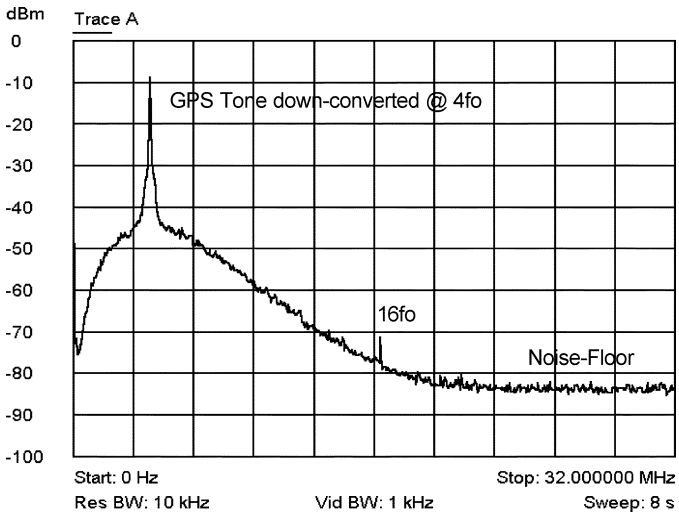

Fig. 20. IF filter output spectrum: 1540f_0 signal down-converted by the radio to 4f_0, baseband turned off.

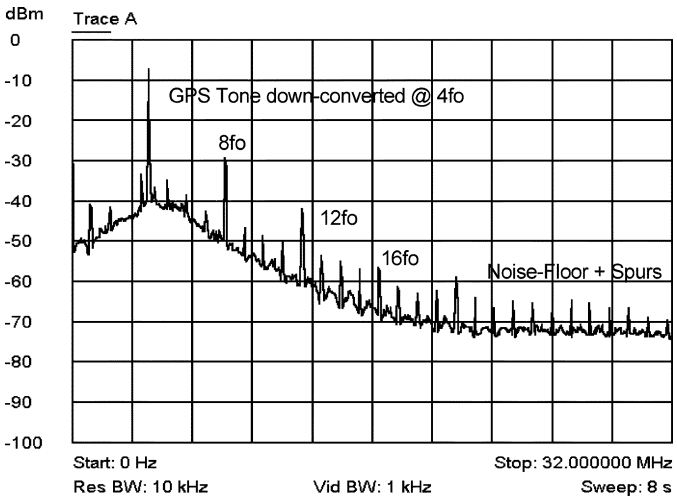

Fig. 21. IF filter output spectrum: 1540f_0 signal down-converted by the radio to 4f_0, baseband turned on.

TABLE II
MEASURED RADIO PARAMETERS

	Measured Performances	**Unity**
Voltage Gain	92	dB
S11	< -12	dB
Noise Figure NF	4.8	dB
Image Rejection (centre-of-band)	30	dB
Image Rejection Bandwidth	3	MHz
P1dB input of LNA-MIXER (Balanced)	-29	dBm
P1dBout of LNA-MIXER (Balanced, peak-to-peak)	1	Vpp
P1dBout of IF Filter (Balanced, peak-to-peak)	1.6	Vpp
PhaseNoise @1 MHz	-112	dBc/Hz
PhaseNoise @100 KHz	-92	dBc/Hz
Total Current Consumption	17	mA
Total Power @ Vdd=1.6V	27.2	mW

baseband turned on, there is ∼10 dB increase in the thermal noise floor away from the carrier (i.e., at offset higher than 16f_0). This is not important for the application, since just the 2f_0 bandwidth centered at IF = 4f_0 contains GPS information and is processed by the baseband. In this 2f_0 band (centered at 4f_0), baseband processing causes an increase of ∼2 dB in NF.

C. SoC Operation and Discussion of Results

Satellites tracking and position fix (with 3-m rms precision) has been achieved by the SoC GPS receiver connected to a GPS active antenna in an outdoor environment.

The impact of CPU DSP processing on the radio has been attenuated thanks to architectural, design, layout, and isolation strategies. In particular, the VCO is not modulated and the radio is not saturated by interferences generated by CPU DSP, since those spurious signals are well below output P_{1dB}. As a consequence, radio 1-bit A/D is still in the condition to toggle on thermal noise and GPS signal (as specified thermal noise is 20 dB higher than GPS signal in its 2-MHz band) and transfer this information to baseband, where latitude, longitude, and height are calculated. The effect of the 2 dB increase in NF when baseband is turned on is attenuated by use of active antenna and the RF performance of the radio is still enough to allow the baseband to calculate the GPS position with 3-m rms. This has been demonstrated in an outdoor environment with the SoC connected to a GPS active antenna. Sensitivity of the SoC GPS is −130 dBm, therefore, it is suitable for outdoor applications.

TABLE III
GPS SoC—COMPARISON WITH STATE OF THE ART

SoC	**This**	**[8]**	**[9]**	**Unit**
Architecture	Low-IF IF=4 MHz	Double IF IF1=2 MHz IF2=1 MHz	Low-IF IF=4 MHz	
Tracker	YES	YES	YES	
Full Stand-Alone Positioning	YES	Info Not Available	Info Not Available	
Sensitivity	Out door	In door	Indoor	
Area of SoC	23	40	12.8	mm^2
Area of Radio	4.1	4.6	~ 5.6 (*)	mm^2
Pw of SoC	56	57	84 (**)	mW
Technology	180	180	90	nm
ESD HBM/MM	2/175	Info Not Available	Info Not Available	KV/V

(*) Area estimated (**) Including regulators

VI. COMPARISON WITH STATE OF THE ART

In Table III, this work is compared with reported SoC GPS receivers, while in Table IV comparison is restricted to the radio embedded into SoC implementations. To the best of the authors' knowledge, this is the first SoC GPS capable of working as a satellite tracker and also providing stand-alone position features. This means that, with no need of an external host, this SoC runs the GPS application SW and provides NMEA coordinates.

TABLE IV
GPS RADIO—COMPARISON WITH STATE OF THE ART

	This	[8]	[9]	Unit
Image Rejection	30	30	18	dB
Noise Figure	4.8	4	2	dB
PhaseNoise @100-KHz	-92	-92	-88	dBc/Hz
P1dB input LNA-MIXER	-28	-	-5	dBm
P1dBout LNA-MIXER	1	-	-	Vpp
P1dBout IF Filter	1.6	-	-	Vpp
Auto-calibration Filters -VCO	Present	Present	Present	
Radio/SoC Power Dissipation	20/56	24/57	- / 84	mW

This SoC has been qualified for production and withstands up to 2-kV HBM and 175-V MM model.

In terms of radio architecture, this work and [9] use a low-IF architecture with $4f_0$ IF frequency, while [8] uses a double-IF approach.

As far as the frequency synthesizer is concerned, this work and [9] use a VCO running at twice the operation frequency followed by a divide-by-two, while [8] uses a quadrature VCO. Power dissipation of [9] is higher than this work and [8], but it includes voltage regulators, so it is difficult to quote dissipation of radio and SoC stand-alone. Radio die area is equivalent in all implementations, since analog circuits do not scale down with technology. The total area of the 90-nm implementation [9] is much less than this work and [8] since baseband area is reduced.

VII. CONCLUSION

A 23-mm^2 GPS receiver with radio ARM7-DSP-64 kRAM-256 kROM has been integrated in a 180-nm CMOS process. The SoC GPS receiver needs only an active antenna, a crystal, and a few passives for input match and provides latitude, longitude, and height with 3-m rms precision. An external host is not required, and the SoC temperature range is $[-20, 105]$ °C. The architectural, design, layout, and isolation strategies that allowed successful co-existence of GPS radio with baseband processing have been reported. The 4.1-mm^2 radio draws 17 mA from a voltage supply in the 1.6–1.8-V range and takes 11 pins of a VFQFPN68 package. Experimental results have been compared with the state of the art, i.e., the only two existing SoC GPS receivers, in 180-nm and 90-nm CMOS technology. To the best of the authors' knowledge, this is the first SoC GPS capable of working as a satellite tracker and also providing stand-alone position features, i.e., capable of running the GPS application SW and providing NMEA coordinates without need of an external host.

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From 1988 to 1992, he was with Semiconductor Complex Limited, Mohali, India, as a Member of the Design Development Team, developing mixed analog–digital macrocells and telecommunications products. Since 1993, he has been with STMicroelectronics. His present activity and interest is to define, develop, and attain maturity of Systems-on-Chip targeted for the automotive industry in RF CMOS and embedded Flash process.

Massimo Franciotta was born in Salerno, Italy, in 1967. He graduated from the University of Pavia, Italy, in 1991.

He spent two years in the Microelectronic Laboratory o f the same university as a research assistant participating in national research programs on the design of analog integrated circuits. After military service, in 1994, he joined CSEM (Centre Suisse d'Electronique et Microtechnique), Neuchâtel, Switzerland, where he was involved in the design of fully integrated low-power transceivers (100 kHz–450 MHz frequency range) for short-range data links in BiCMOS and CMOS technology. Since 1998, he has been with the TPA Technology Center of ST Microelectronics, Catania, Italy, as a Senior RF Designer working on IF circuits for mobile terminals in BiCMOS technology. He is currently involved in the design of low-power fully integrated GPS receivers in deep-submicron CMOS technology. He holds one patent and has several publications.

Nino G. Bellantone was born in Reggio Calabria, Italy, in 1971. He graduated in electronics engineering from the University of Bologna, Italy, in 1996. Currently, he is working toward the Ph.D. degree in electronics and communications at the University of Reggio Calabria.

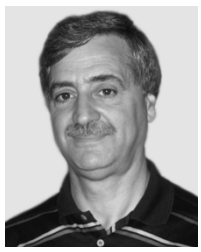
His working experience started as a software engineer with AISoftware SpA, Milan, Italy. Since 1999, he has been with STMicroelectronics, Catania, Italy, as an RFIC Designer, where he has been involved in the design and development of several RF-IPs for DVB-S, GPS, short-range radar sensors, and FM radio projects. His research interest is focused on CMOS fully integrated frequency synthesizers and oscillators and on receiver architecture for low-power mobile communications.

Michele Vaiana was born in San Cataldo, Italy, in 1974. In 1999, he received the degree in electronic engineering (*summa cum laude*) from the University of Palermo, Italy.

In 2000, he joined STMicroelectronics where he was involved in the design of LDMOS power amplifier for wireless applications. Since 2002, he has been engaged in the design of integrated RF circuits in BiCMOS and CMOS technology. Currently, he is an RF PA IC Design Engineer in the PA IC team at Catania, Italy. He holds one patent and has coauthored a few conference papers.

Valentina Mandará was born in Ragusa, Italy, in 1974. In 2001, she received the degree in electronic engineering from the University of Catania, Italy.

Since 2001, she has been with STMicroelectronics as an Analog Designer.



Mario Paparo (M'91) was born in Randazzo (Catania), Italy, in 1952.

He has been with SGS (now STMicroelectronics) since 1977, where he has taken various responsibilities in the design, application, testing and R&D co-ordination of analog, smart power, mixed-signal silicon ICs for telecommunications, radio frequency, power management, and industrial applications. Since 1994, he has been managing the design and development activities of STMicroelectronics Technology Center of Catania. The center is mainly focused on the development of low-power ICs for wireless and portable equipment, RF MMICs and advanced RF IPs for W-CDMA, GPS, WLAN, broadcast satellite receivers, RF PA modules and power management ASICs for cellular application in silicon technologies (BiCMOS, Si-Ge, BCD, 130–65 nm CMOS). He is an author or coauthor of several papers on analog ICs design and application. He holds 15 patents on analog and smart power integrated circuit and active devices design.

Mr. Paparo served on the IEEE ISSCC Wireless Communication Technical Committee in 2003 and 2004.