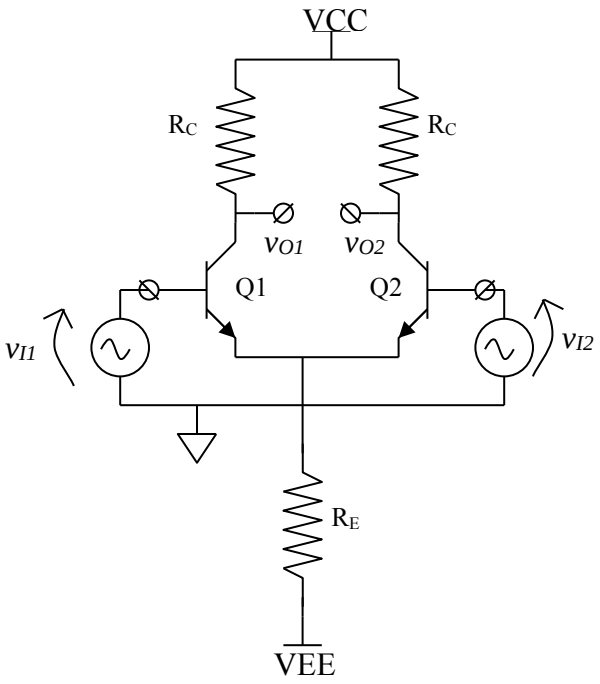
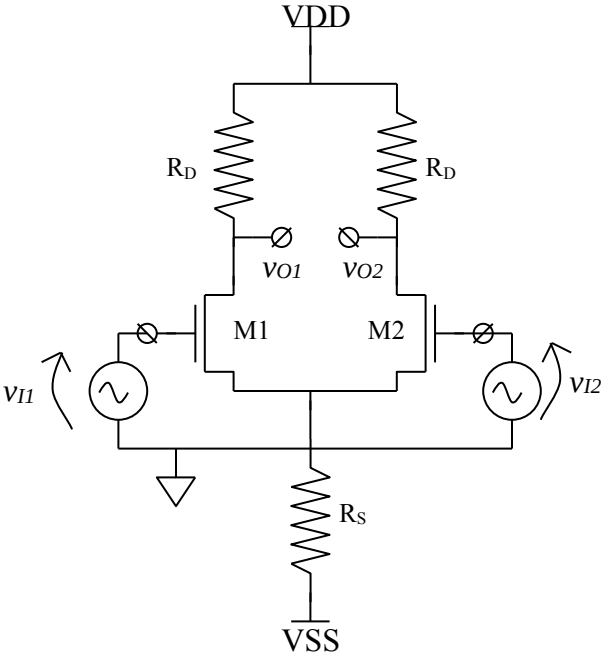
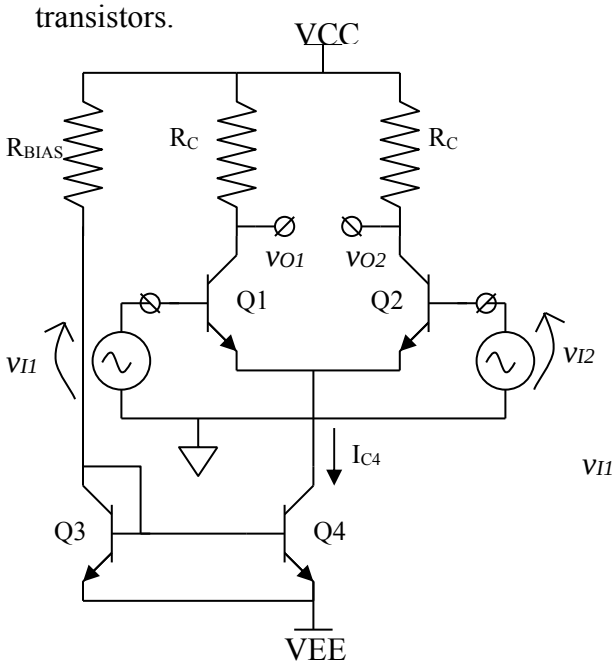


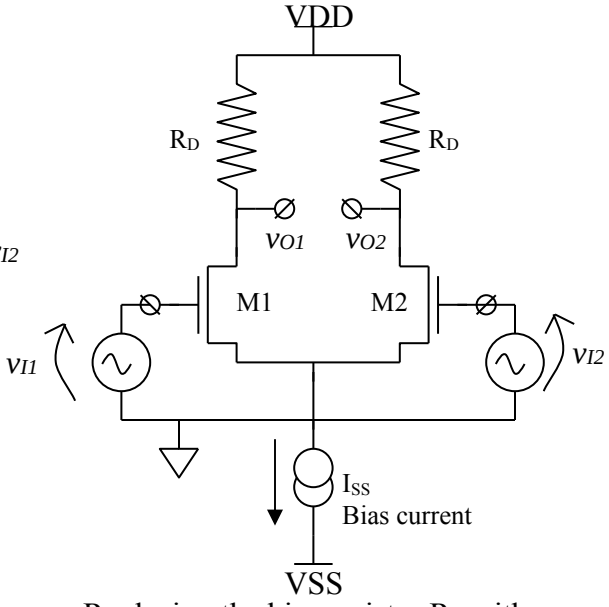
Discrete, resistor-based differential amplifier with "long-tailed" pair of NPN transistors.



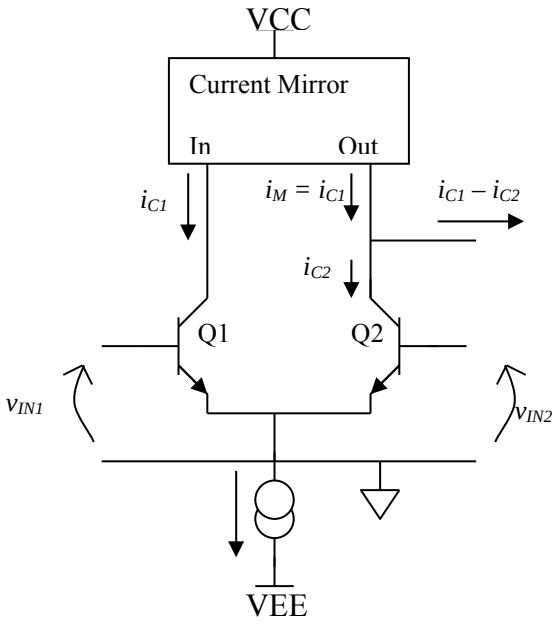
Discrete resistor difference amplifier with N-channel MOSFETs. Not very practical because of poor MOSFET performance with resistor loads.



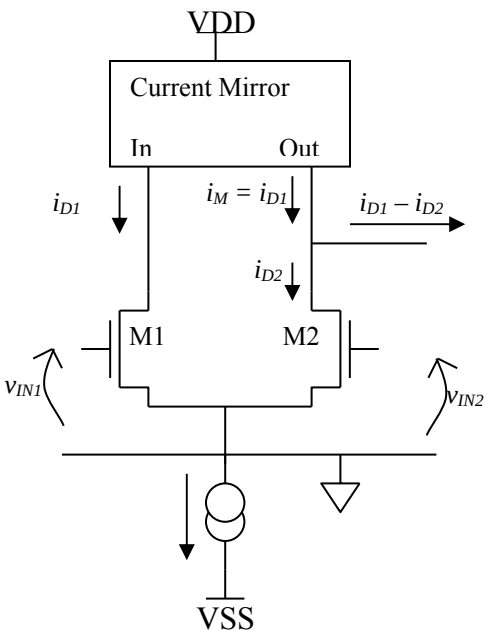
Q4 acts as a constant current source replacing R_E to make the outputs more nearly proportional to the input voltage difference. R_{BIAS} sets the current by determining the current in Q3 and the current in Q4 is the same because Q3 and Q4 are matched.



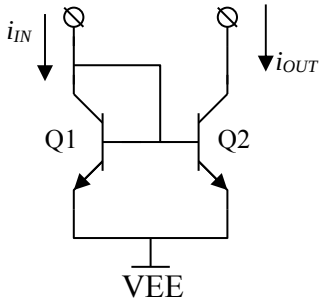
Replacing the bias resistor R_S with a constant current source reduces cost, area, and most importantly the error. The common mode rejection ratio improves markedly.



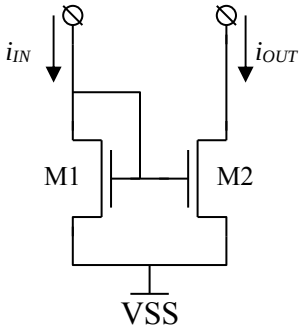
Concept of using a current mirror circuit to allow subtraction of collector currents at a simple node by KCL.



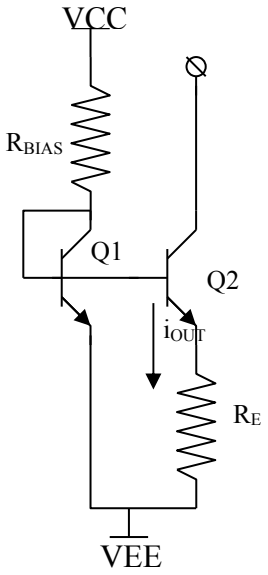
Use of a current mirror in N-channel MOSFET difference amplifier for single ended output and higher common mode rejection.



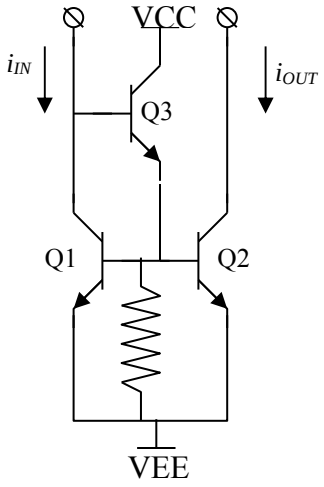
The most basic current mirror with $i_{OUT} = \frac{h_{FE} i_{IN}}{h_{FE} + 2}$ and an output resistance equal to $r_{O2} = \frac{V_{CE} + V_A}{I_C}$.



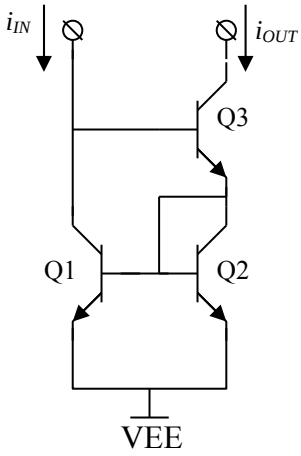
The primitive current mirror in MOS devices. Because MOSFETs usually have lower output resistances than BJTs, this circuit often causes lower gains than its BJT counterpart.



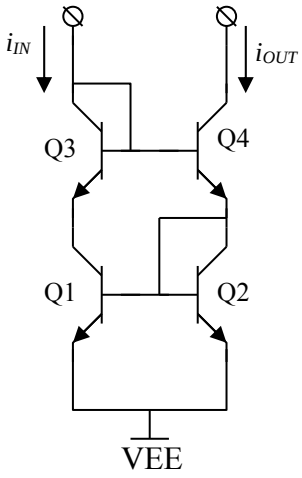
Widlar current source, for which $I_{C2} = \frac{kT}{qR_E} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$. The collector current of Q2 may be much lower than Q1 with only a modest value for R_E. The output impedance is also raised by a factor usually between 3 and 6 times the value of r_{02}.



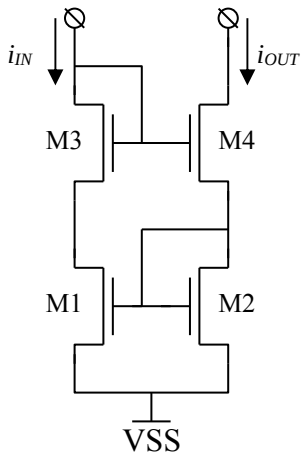
Current mirror using a common collector stage to balance input and output. Output impedance is still r_{O2}. The minimum output voltage is very low – V_{CESAT} of Q2.



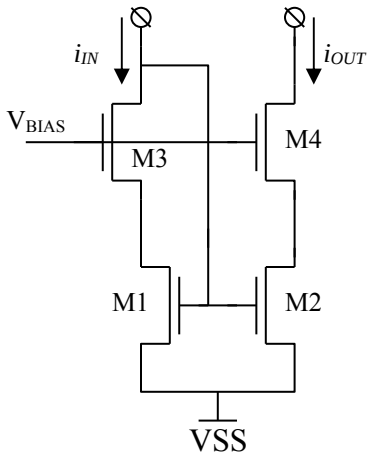
Wilson current mirror –this has a much higher output resistance from the cascoding effect of Q3. However its minimum output voltage is higher by V_{BE}.



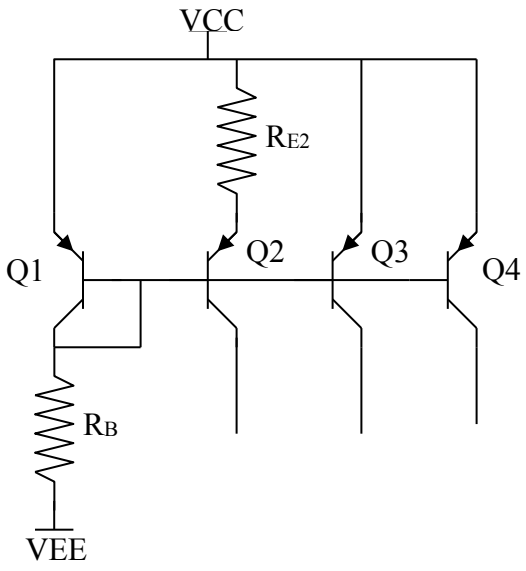
Wilson current mirror with an additional transistor, Q3, to equalize the collector-emitter voltages of the matched pair Q1-Q2. Reduces current mismatch from the Early effect.



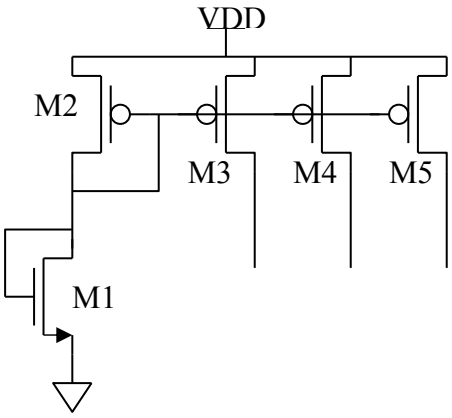
A Wilson current mirror in MOS devices with a fourth transistor, M3, to equalize the drain-source voltages of the matched pair M1 – M2. Because of the relatively high value of V_{TH}, this circuit, which requires a minimum voltage drop of $2(V_{TH}+V_{OV})$ across the left and $V_{TH}+2V_{OV}$ on the right, may not be satisfactory for low voltage systems.



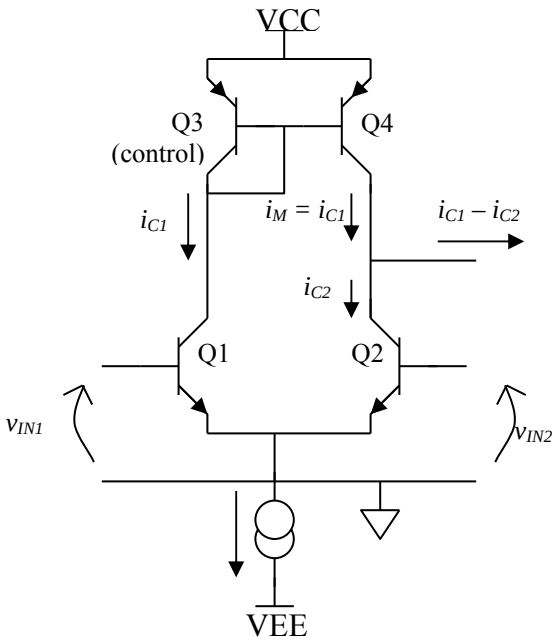
A cascoded current mirror with M3 and M4 as the cascoding transistors. With careful selection of V_{BIAS} this circuit can have an output resistance that is much higher than the uncascoded version. The advantage over the Wilson configuration is that it can operate with input to V_{SS} drop of only $V_{TH}+V_{OV}$ and output to V_{SS} of $2V_{OV}$.



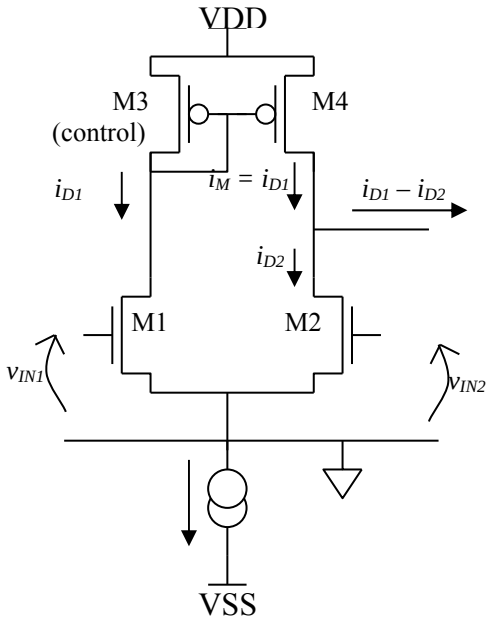
Multiple PNP current sources; I_{C3} and I_{C4} are matched to I_{C1} (the control transistor) but I_{C2} is reduced by R_{E2}. The Q2 – R_{E2} combination is a Widlar current source.



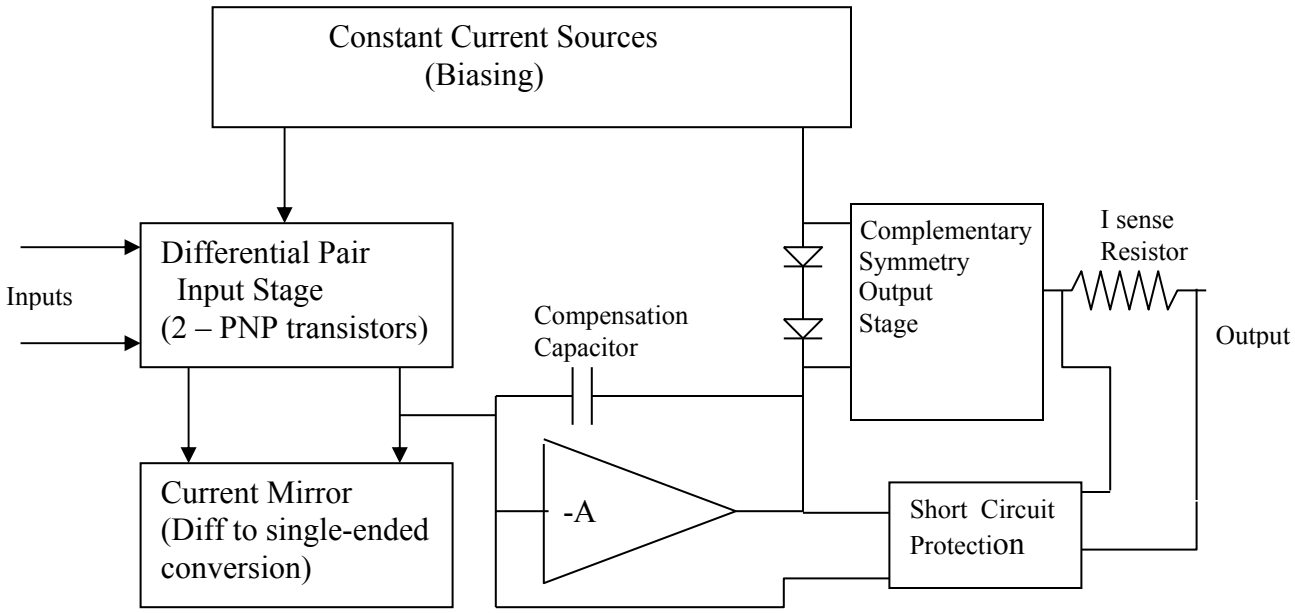
Multiple P-channel sources: M1 is a long, narrow device that sets the current level. Usually M2, M3, M4, and M5 have the same lengths but may differ in width to set different output current values. When precise matching is needed, wider devices are made of paralleled devices with the same width as the control transistor, M2.



Simplest bipolar current mirror within a differential amplifier. Q3 is the control transistor for the current source Q4. Because Q3 is connected as a diode, it has a low impedance to the power supply. Q4 is open collector and so exhibits a relatively high output impedance, that is, it approximates a constant current source.



Simplest CMOS MOSFET current mirror within a differential amplifier. M3 is the control transistor for the current source M4. Because M3 has its drain and gate connected, it has a low impedance to the power supply ($Z_{M3} = 1/g_{m3}$). M4 has an open drain and so exhibits a relatively high output impedance, that is, it too approximates a constant current source.

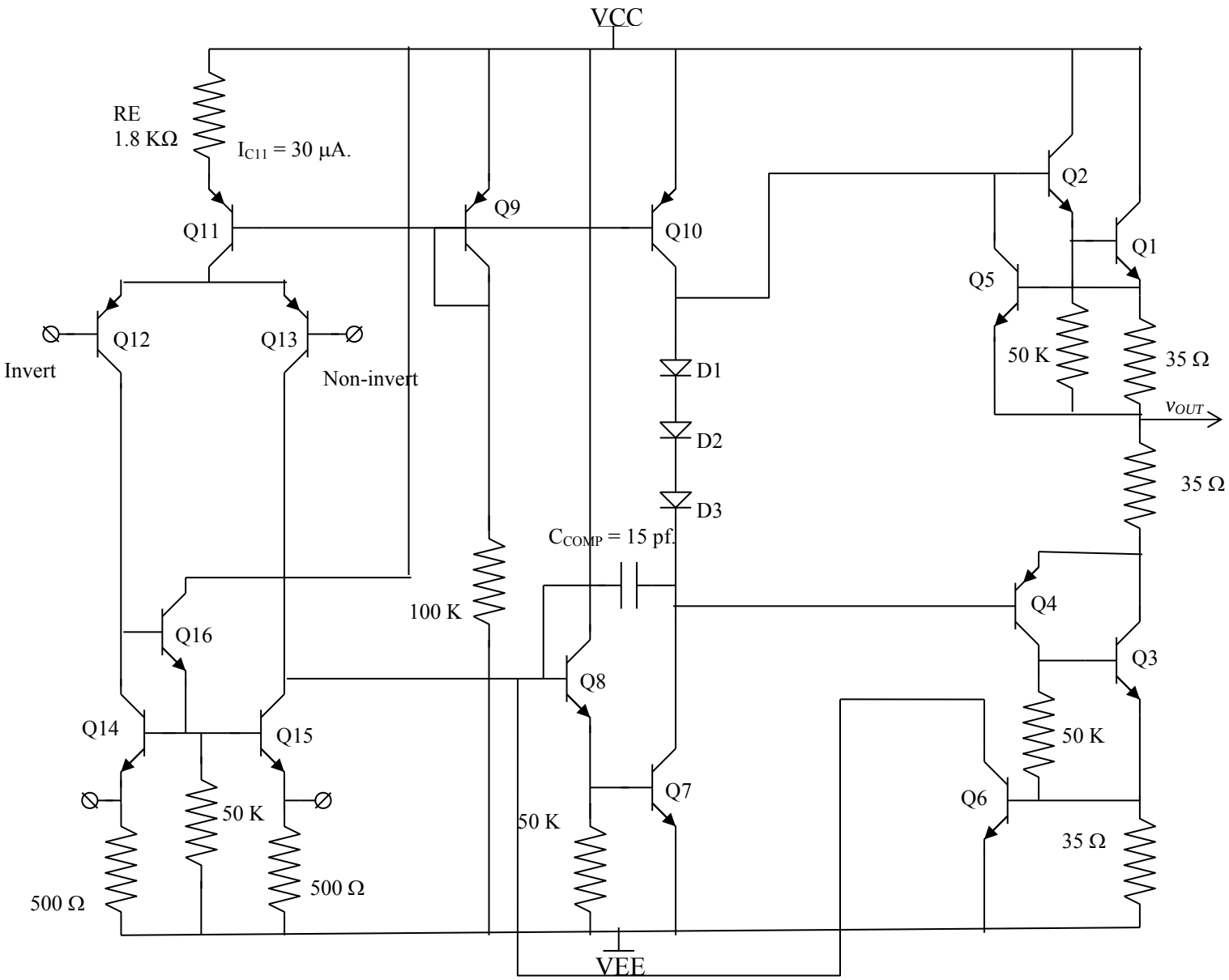


Block Diagram of a Bipolar Operational Amplifier

The tables show the quiescent conditions for the transistors in the bipolar operational amplifier that I use in class. The assumptions about the devices are:

Device Type	V_{BE}	$h_{FE} = \beta$	V_A	V_{CESAT}
NPN	0.6 volts	100	150 volts	0.2 volts
PNP	0.6	70	30	0.3

Quiescent Currents and Transistor Model Parameters					
Transistor	**IC**	**IB**	**re**	**ro**	**gm = IC/kt/q**
Q7	227 ua.	2.27 ua.	113 ohm	704 kohm	8790 usie.
Q8	14.2	0.142	1.8 K	12.4 Meg.	549 usie.
Q9	227	3.35	113	132 K	8720
Q10	227	2.3	113	174 K	8720
Q11	30	0.43	860	1.3 Meg.	1150
Q12, Q13	15	0.21	1.72 K	2.7 Meg.	573
Q14, Q15	15	0.15	1.72 K	10.7 Meg.	576
Q16	12.3	0.12	2.1 K	14.2 Meg.	477


VCC
RE
1.8 KΩ
I_{C11} = 30 μA.
Q11
Q9
Q10
Q2
Q1
Q5
Q12
Q13
Invert
Non-invert
50 K
35 Ω
D1
D2
D3
v_{OUT}
35 Ω
C_{COMP} = 15 pf.
100 K
Q4
Q16
Q3
Q8
Q14
Q15
50 K
Q7
Q6
50 K
35 Ω
500 Ω
500 Ω
VEE