Current versus Voltage Characteristics of Long-Channel MOSFETs

It is surprisingly difficult to calculate the current-voltage relations of MOSFETs to good accuracy over a wide range of conditions as device dimensions shrink. This has been the subject of intense research activity for many years and continues in the realm of submicron devices even today. Still one needs approximate methods for hand calculations even if they are not entirely accurate. Such calculations are key to understanding what a circuit is supposed to do and to finding initial device sizes. Customarily, the ideal long-channel formulae are used for this purpose. From simplified basic physics, these relations are:

$$I_{DS} = \frac{W}{L}\cdot K_N \cdot \begin{cases} I_S \exp\left(\dfrac{q\left(V_{GS}-V_{TH}\right)}{n_{st}kT}\right) & \text{if } V_{GS} \le V_{TH} \\ \left(V_{GS}-V_{TH}-\dfrac{(1+a)}{2}V_{DS}\right)V_{DS}\left(1+\lambda \mathrm{V_{DS}}\right) & \text{if } V_{DS} \le \dfrac{\left(V_{GS}-V_{TH}\right)}{(1+a)} \\ \dfrac{\left(V_{GS}-V_{TH}\right)^2}{2(1+a)}\left(1+\lambda \mathrm{V_{DS}}\right) & \text{if } V_{DS} \ge \dfrac{\left(V_{GS}-V_{TH}\right)}{(1+a)} \end{cases}$$

where:

- W is the width of the device
- L is the channel length of the device
- K_N is a manufacturing parameter with dimensions amps/volt^2 that captures the oxide capacitance per unit area and the electron channel mobility. When you want to relate the current to the device material properties, one uses the relation $K_N = \mu_e C_{OX}$ where μ_e is the mobility of the inversion layer electrons (slightly lower than the mobility in the bulk material) and C_{OX} is the capacitance per unit area of the oxide. If t_{OX} is the thickness of the insulating oxide, then $C_{OX} = \varepsilon_{OX} / t_{OX}$.
- a is a dimensionless manufacturing parameter related to substrate doping; usually it lies between 0 and 1. It is a rough approximation to account for the growth of the depletion layer to the body at the drain end of the device as drain voltage increases. Most textbooks just assume that a = 0.
- λ plays the same role for a MOSFET as the Early voltage does for a bipolar transistor. It has units of volts^{-1} and its inverse is effectively an Early voltage. The effect of the term in λ, an increase in drain current with increasing V_{DS} is due to channel length modulation. The effective channel length gets smaller as V_{DS} makes the drain depletion thickness larger. As a result, one can reduce the value of λ by increasing the value of L. However, MOSFETs do not conform to the Early model as well as bipolars do, so λ also changes somewhat with quiescent conditions

In principle these equations hold so long as the electric field in the device is weak enough that the channel mobility is not affected by it. (The average speed of an electron is given

by the mobility times the electric field, $\mu_e \vec{E}$, only as long as the magnitude of $\left|\vec{E}\right|$ is less than about $1 \cdot 10^4$ V/cm. Above that the velocity is approximately constant, around $6 \cdot 10^{+6}$ cm/sec.) Whether this condition is met depends primarily on V_{GS}. Usually the equations will be satisfactory if

$$V_{GS} < V_{TH} + (1+a) L \cdot 10^4$$

where the length is in centimeters. If this condition is not met, then much more complicated equations are necessary. Fortunately the circuits we encounter will meet this requirement.

There are several problems with these equations. First of all, the current near and below threshold is not zero. Instead below threshold one sees a current:

$$I_D = I_S \exp\left(\frac{q(V_{GS} - V_{TH})}{nkT} \right)$$

where I_S is a subthreshold current that is dependent on geometry and manufacture and n is an ideality constant related to the capacitance from channel to substrate. Usually, n is in the range $1 < n < 2$ for small signal MOSFETs and $3 < n < 6$ for power MOSFETs.

A second problem is that the threshold voltage depends on the voltage between the source and substrate. This is not important in power MOSFETs such as the one you used in lab 3 because the source and substrate are tied together internally. However, in the amplifier circuits we will look at shortly, there is often such a potential difference. The threshold as a function of the source-substrate potential is approximately:

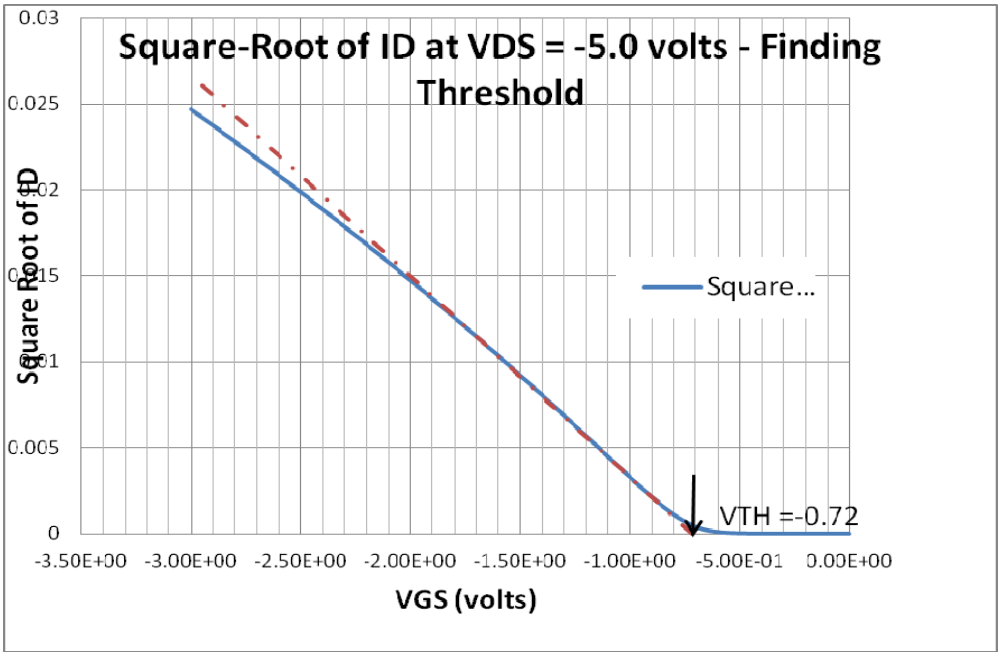
$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{V_{SB} + V_{BI}} - \sqrt{V_{BI}} \right)$$

where V_{TH0} is the threshold with the source and substrate connected, γ is a manufacturing parameter, and V_{BI} is the built-in potential of the source-substrate junction.

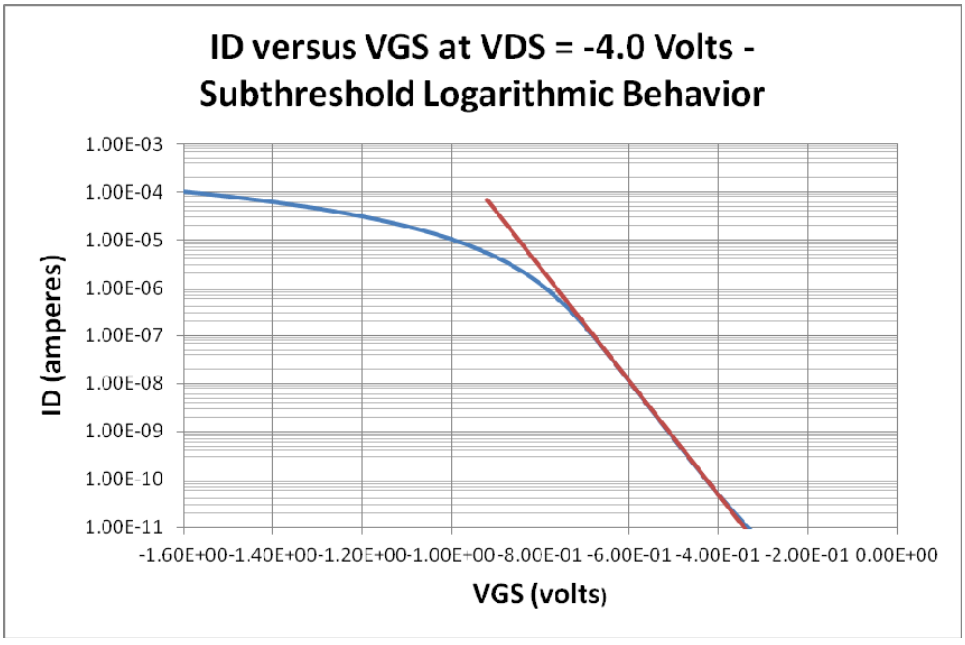
The ALD1107 Devices

Now for some data. Here is data from P-channel MOSFETs in an ALD1107 device. (The ALD1106 (N-Channel) and ALD1107 (P-channel) devices are almost the only discrete packaged MOSFETS of the kind used for analog circuit design. Most such design with CMOS devices is done within integrated circuits.) In principle all voltages and current directions change sign as P-material replaces N-type and vice versa. The figures honor that convention but it is easier for me to explain the formulae without worrying about the signs.

The first step is to see what V_{TH0} might be. In the active region, the drain current is proportional to the square of the difference of the gate and threshold voltages, that is, $I_D \propto (V_{GS} - V_{TH})^2$. If one plots the square root of ID against V_{GS} in this region, then one ought to get a straight line whose intercept with the x-axis is the threshold. Here is such a plot with an overlaid straight line extending back to V_{TH0} = -0.72 volts. Notice that at the threshold, the current is not zero!

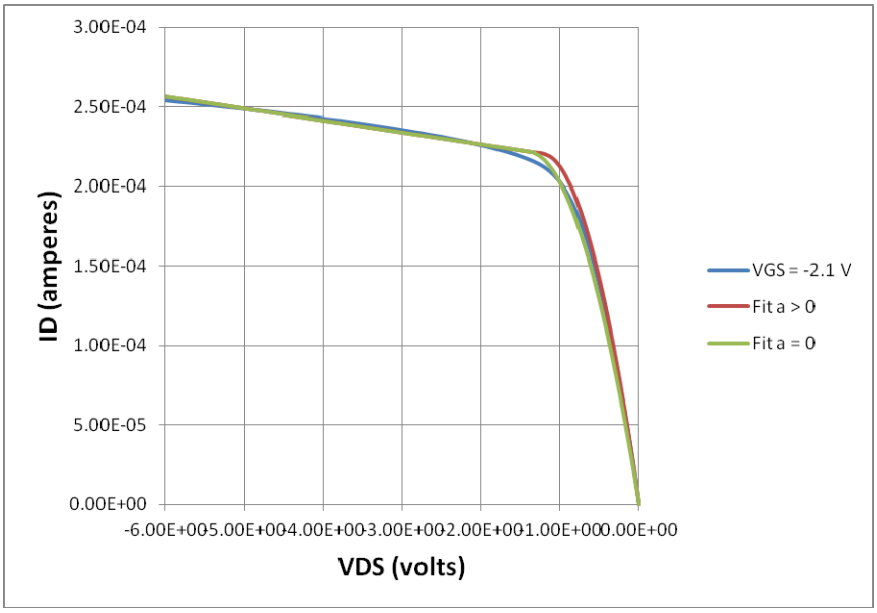


The next graph shows how the current varies below threshold on a logarithmic y-axis to show the ideality factor. I have drawn a straight line asymptotic to the curve in the range of $1 \cdot 10^{-11} < I_D < 3 \cdot 10^{-7}$. The slope yields an ideality factor of $n = 1.41$, and the value of I_S is about 0.48 µamp.

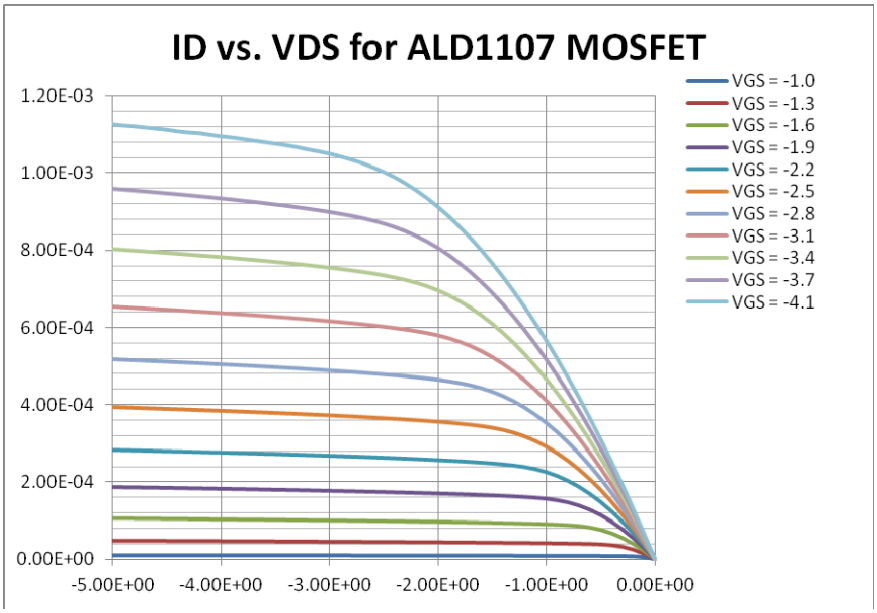


The next graph shows I_D as a function of V_{DS} for one value of V_{GS} = -2.1 volts. I have overlaid two curves from the long-channel equations. The first curve has $a = 0.14$ representing the best fit both at the origin and at high values of V_{DS}. The second curve uses $a = 0$ for simplicity. (For some devices, a is larger (.3 to .6) and more important. In some

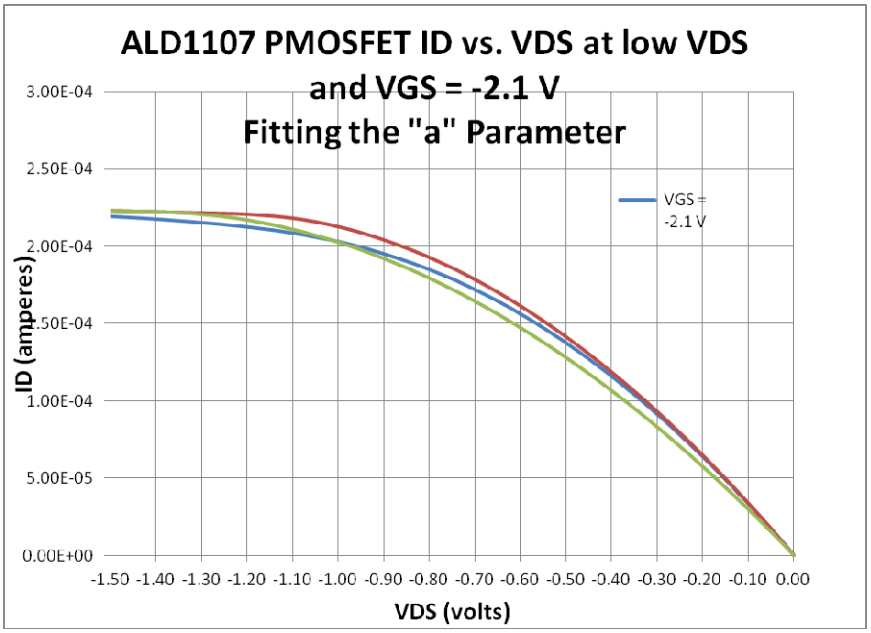
circuits, such as digital switches, the fit to ID vs VDS at the origin is quite important and *a* has to be taken into account. However, if you are only going to use the device in its forward active region, then fit at the origin may be traded off for mathematical simplicity. This assumption that $a = 0$ is what Razavi uses in his chapter on MOSFET operation.) In the latter case, K_P is adjusted to get a good fit at higher voltages. Neither curve does very well near the changeover between the two equation forms. Notice that the output conductance, that is, the slope of the I-V curve, is a particularly poor fit to the data at some low drain voltages. One implication of this is that λ is not well defined there and attempts to use it for gain and output impedance calculations in that bias range will usually give significant errors.



The next figure shows a full set of I-V curves for a range of gate and drain voltages. Families of curves such as this one are key to understanding how to model devices in amplifier and filter applications.



Here is a graph showing the fit to I-V near VDS = 0 at an expanded scale.



Finally, in designing circuits to have minimum electrical noise, it is important to have some transistors have a high transconductance per ampere of drain current and others a relatively much lower value. One arranges for this by sizing transistors to have Q-points with different values of overvoltage, $V_{OV} = V_{GS} - V_{TH}$. This graph shows both the transconductance per ampere as a function of the overvoltage and the theoretical limiting values of this ratio above and below threshold.