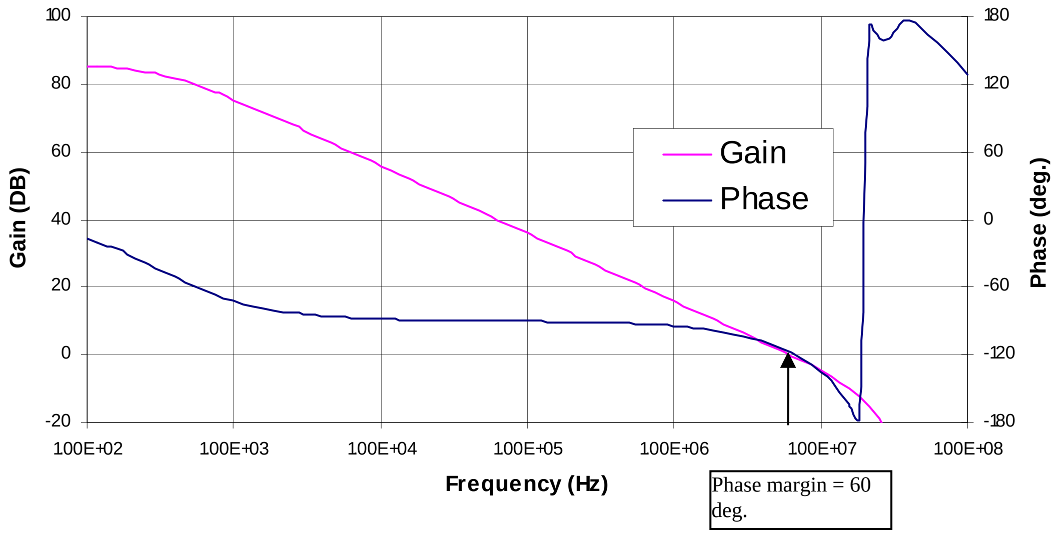
Example of a MOSFET Operational Amplifier:

This circuit is one I "designed" as an example for Engineering 1620. It is certainly not fully optimized and I am not sure it is free of errors. It is based on a 1.5 micron, P-well process and therefore uses an N-channel differential pair for its input. This is somewhat unusual because P-channel devices have lower intrinsic noise and are the device-type of choice for the input stage. I did this simply to avoid doing your SPICE assignment for you. The overall properties of the circuit are given in the table below.

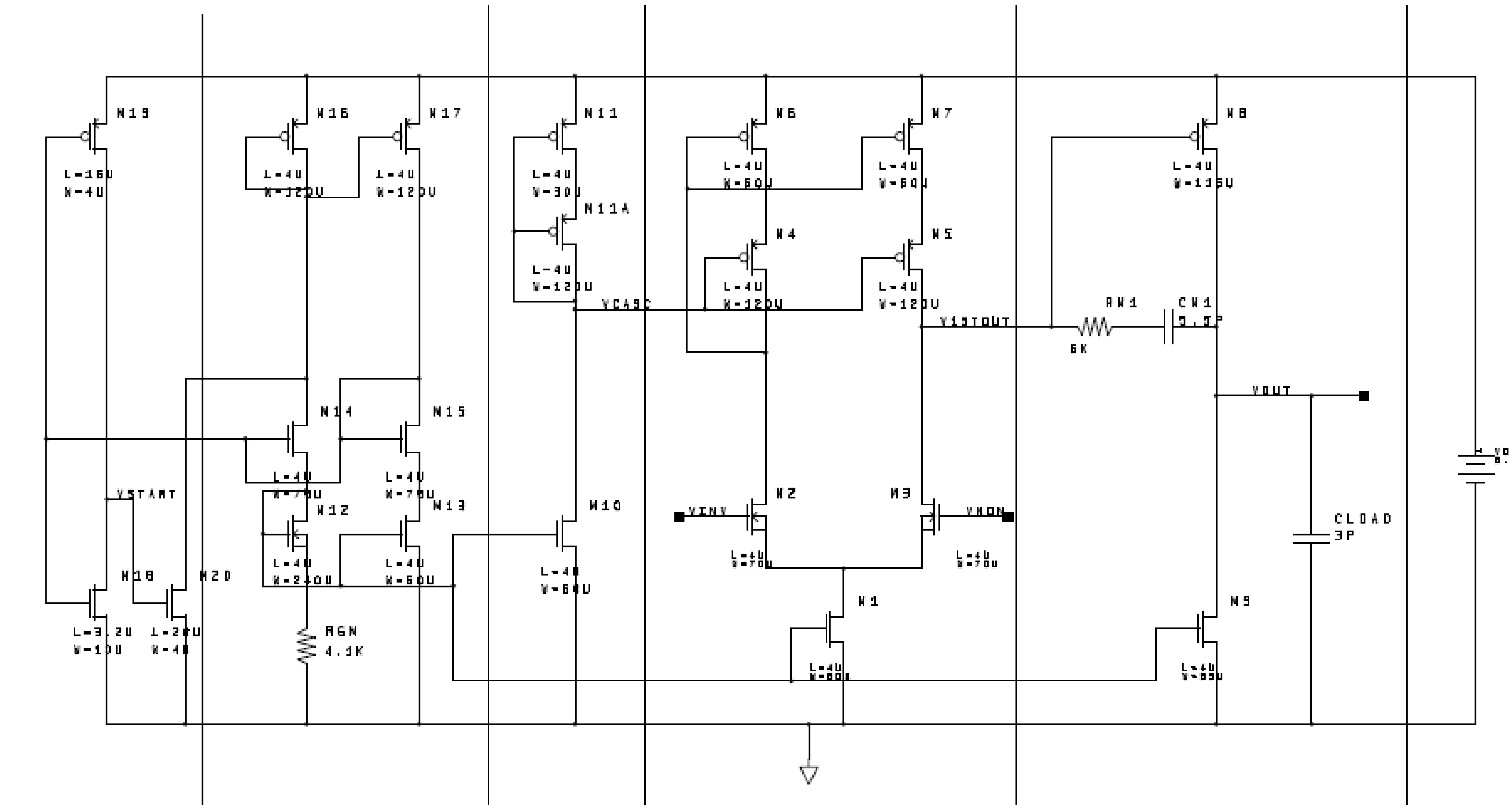
Amplifier Property	Value
A_0 – DC Gain	86 DB (X20,000)
f_p – dominant pole position	400 Hz
f_{GBW}	8.0 MHz
f_U – unity gain frequency	5.6 MHz
Output stage resistance at low frequency	277 K
Zero position	10.7 MHz
Slew Rate	$7 \cdot 10^6$ V/sec
Output stage quiescent current	65 μa
Opamp quiescent current	103 μa
Bias circuit quiescent current	104 μa
Total system quiescent current	210 μa
VDD	5.0 volts
Total system power	1.1 mW

MOSFET Operational Amplifier Gain and Phase



Parameter Table for MOSFET Opamp Example

element	model	vds	vgs	vth	vov	id	gm	ro
m1	nssb	0.748	0.851	0.547	0.304	3.77E-05	2.90E-04	5.54E+05
m10	nssb	3.368	0.851	0.547	0.304	4.12E-05	3.11E-04	8.09E+05
m12	nssb	0.711	0.711	0.546	0.165	3.51E-05	5.01E-04	5.05E+05
m13	nssb	0.838	0.851	0.547	0.304	3.79E-05	2.91E-04	5.92E+05
m14	nssb	3.078	1.079	0.840	0.239	3.51E-05	3.27E-04	8.12E+05
m15	nssb	1.092	1.092	0.836	0.256	3.79E-05	3.31E-04	6.32E+05
m18	nssb	0.023	1.930	0.559	1.371	5.36E-06	3.42E-06	4.34E+03
m2	nssb	3.156	0.752	0.547	0.205	1.89E-05	2.22E-04	1.36E+06
m20	nssb	3.929	0.023	0.594	-0.571	7.88E-12	4.17E-13	1.00E+12
m3	nssb	3.089	0.752	0.547	0.205	1.89E-05	2.22E-04	1.36E+06
m9	nssb	1.654	0.851	0.547	0.304	5.63E-05	4.29E-04	5.19E+05
m11	pssb	0.478	1.632	0.746	0.886	-4.1E-05	6.34E-05	2.13E+04
m11a	pssb	1.154	1.154	0.793	0.362	-4.1E-05	2.08E-04	6.64E+05
m16	pssb	1.072	1.072	0.737	0.335	-3.5E-05	1.92E-04	7.27E+05
m17	pssb	3.070	1.072	0.727	0.344	-3.8E-05	1.99E-04	7.14E+05
m19	pssb	4.977	3.070	0.781	2.289	-5.4E-06	4.35E-06	9.43E+07
m4	pssb	0.512	1.048	0.812	0.236	-1.9E-05	1.42E-04	8.52E+05
m5	pssb	0.579	1.047	0.812	0.235	-1.9E-05	1.42E-04	9.19E+05
m6	pssb	0.584	1.096	0.741	0.355	-1.9E-05	9.73E-05	1.09E+06
m7	pssb	0.585	1.096	0.741	0.355	-1.9E-05	9.73E-05	1.10E+06
m8	pssb	3.346	1.164	0.726	0.437	-5.6E-05	2.35E-04	5.96E+05



Startup circuit

Constant gm bias Controls all current sources

Set voltage to cascoded mirror

Input differential pair, current-mirror and bias tail-current source

Common source output stage with pole/zero frequency response shaping exploiting the Miller effect.

VDD supply