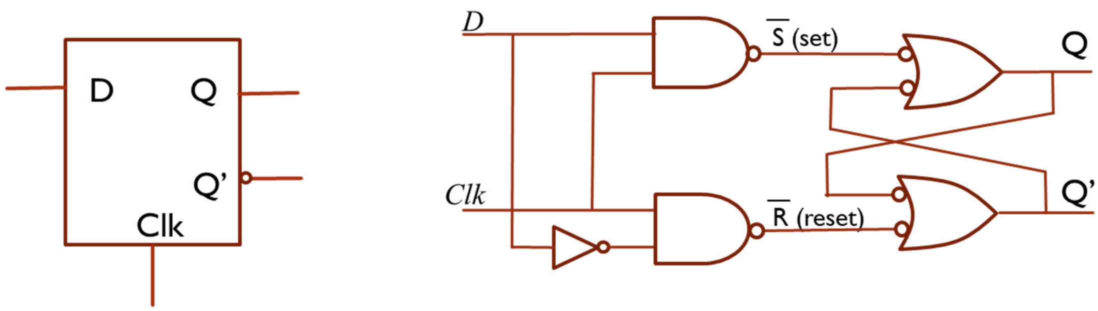
1. [*D-latch timing analysis*] Consider the following D-latch design, composed of an inverter and 4 NAND gates:



Assume that a NAND gate has a propagation delay of t_{NAND}, and the input/output signals can switch values (from 0 to 1, or from 1 to 0) instantaneously.

a. in terms of t_{NAND}, how long would it take for all outputs of a D-latch to stabilize after EN (CLK) is set to 1? Draw a timing diagram to show your analysis. The initial state of the D-latch is D=1, EN=0, Q=0, Q'=1.

   (Hint: With De Morgan's Law, you can create a D-latch that uses a minimum number of NAND gates and one inverter. Assume that an inverter has the same delay as a NAND gate. Your timing diagram may include internal signals, but make sure to label your signals on the NAND-based D-latch circuit.)

b. Assume the same setting as part (a). What would happen if the EN signal is set to 1 for only t_{NAND}? Use a timing diagram to explain your answer.

2. [*Finite State Machine*] Design a state machine that checks a data word received on a serial data line for even parity (i.e., even number of 1's received on the data line). The output signal displays the parity of the data word *up to the bit that has been latched so far* – 1 if even, 0 if odd. In addition to the CLK, the circuit has two inputs, SYNC and DATA. The number of bits in a data word is variable, but SYNC is always asserted while a word is being streamed into the machine (1 bit per clock period). While SYNC is off, the output holds the parity for the previously-streamed input word. When SYNC is asserted again, a new data word begins.

a. Is this a Mealy or a Moore state machine? Why?

b. Draw a state diagram and reduced state table for this machine.

c. Draw the logic diagram for this state machine.