NAME_____

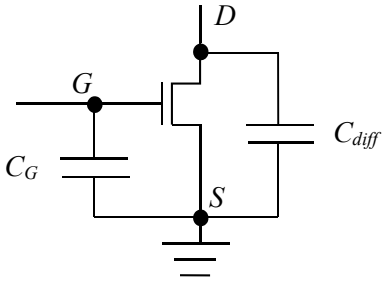
EN1600: Design and Implementation of VLSI Systems

Homework Assignment #2
Due **Friday, October 7, 2016, by 5pm**

1) Estimate the capacitances associated with the NMOS transistor shown in the figure below. Note that C_g and C_{diff} represent the full detailed capacitances for the gate and diffusion respectively. The dimensions of the device are as follows:

   W=150nm, L=50nm, $L_D = L_S$ =100nm, x_d (overlap) = 5nm, x_j (junction depth) = 30nm
   Also, assume $C_j = 5.9\times10^{-7}$ F/cm^2 and $C_{jsw} = 5.0\times10^{-7}$ F/cm^2 and the transistor is operating in the saturation region.

   In class, we discussed using S_iO_2 as the insulator between the gate and the channel. As device sizes scale down, so must the oxide thickness, which becomes a challenge since it would mean shrinking t_{ox} down to around 1nm, causing reliability concerns. Instead, the practice is to use a high-κ dielectric such as hafnium-oxide (hafnia, or HfO_2), which provides a permittivity 5 times greater than S_iO_2. (i.e., $\varepsilon_{SiO2} = 3.9\varepsilon_0$, $\varepsilon_{HfO2}=20\varepsilon_0$, where ε_0 is the permittivity in free space). This allows for t_{ox} =5nm. For this problem assume HfO_2 is used for the gate oxide.
   Show all your calculations.



2) Sketch a transistor-level schematic for a single-stage CMOS logic gate for each of the following functions. Size the transistors such that, as a first order approximation, the worst case rise and fall delays for the gate are the same as that of our reference inverter. **Size the shortest path first.**

   (a) $Y = \overline{((A\cdot B\cdot C)+D)\cdot E}$

   (b) $Y = \overline{((A+B)\cdot C)+D}$

   (c) $Y = \overline{AB+C(A+B)}$

3) For this problem, the term UNIT TRANSISTOR refers to either PMOS or NMOS device with size W = 150nm, and L = 50nm. A minimum sized inverter (i.e., our REFERENCE INVERTER) with roughly equal rise a fall delay will have W_{PMOS} = 300nm, L_{PMOS} = 50nm, W_{NMOS} = 150nm, and L_{NMOS} = 50nm. That is, for all problems, you may also assume that the resistance of the PMOS is twice the resistance of the NMOS *for the same width*. Assume also that the gate and diffusion capacitances of the *unit transistor* are both equal to C = 0.1fF

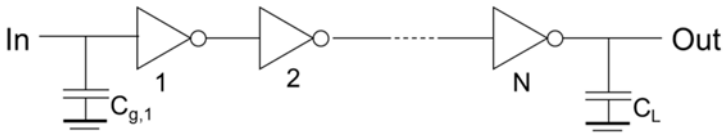
Consider again the function Y in problem 2(b). That is $Y = \overline{((A+B)\cdot C)+D}$

(a) Using the method of Euler paths, draw the **logic graph** and corresponding **stick layout** for the function. Show how your layout is derived from the Euler paths of pull-up and pull-down networks. Try to minimize output capacitance in your layout.
(b) Assume the sizing you chose in 2(b) gives a worst case effective resistance of 12kΩ for the worst case input pattern. When the output is transitioning from high to low, what is the worst-case input pattern for inputs $A-D$?
(c) What input pattern gives the lowest output resistance when the output is high? What is the value of that effective resistance? Explain your reasoning.
(d) What input patterns give the lowest output resistance when the output is low? What is the value of that resistance? Explain your reasoning.
(e) A 5.0 fF capacitance is connected at the output F of the complex gate. Assume the 5.0fF includes *all* components of the load capacitance (C_{int}, C_{ext}, C_{wire}). Ignoring all other internal capacitances, what is the worst case propagation delay (t_{pHL} and t_{pLH})?
(f) What is the best case propagation delay (t_{pHL} and t_{pLH})?
(g) Re-compute the worst case delay by repeating part (e), but this time consider internal capacitance when computing propagation delays. HINT: use the Elmore delay model and assume internal capacitance is composed entirely of diffusion capacitance. If diffusion capacitance is shared between two adjacent transistors without any contact in the diffusion strip, you only need to consider the diffusion capacitance for a single transistor. How do your results differ from part (e). **Please be sure to state all your assumptions when solving this part of the problem.**
(h) Using the Cadence layout tool, draw the layout for the complex function using the transistor sizes you chose for problem 2(b).
(i) Run DRC checks for your layout and show that your layout is free of design errors.

4) Design a layout for a 3-input NAND and a 3-input NOR gate using the Cadence layout tool. As with problem 3), assume a minimum sized NMOS transistor has dimensions L=50nm, W=150nm. If possible, keep it the same pitch as your inverter and 2-input NAND and NOR gates from homework #1.

(a) Before proceeding with the layout, draw a transistor representation of your NAND and NOR gate using the Virtuoso Schematic Editor. Size all the NMOS and PMOS transistors such that rise and fall delays are approximately equal under worst-case delay.
(b) Draw the layout for the NAND and NOR gates. Make sure your design is compact as possible and try to use the same pitch as the 2-input NAND, NOR and inverter gates you previously designed. Once you have completed the layout, run DRC and LVS.
(c) Comment on the difference in area between your NAND and NOR layouts.
(d) Extract the netlist from the layout of each gate using Calibre PEX and simulate each of them for all input combinations. **Explain any anomalies you may notice in the waveforms.**

5) In class, we discussed how to choose sizing values in order to minimize the total delay through a chain of inverters.



That is, given a chain of inverters with input capacitance of $C_{g,1}$ at the first inverter and load capacitance of C_L at the output of the last inverter, we can express the total propagation delay as:

$$t_p = t_{p0} \sum_{j=1}^{N} \left(1 + C_{g,j+1}/(\gamma C_{g,j})\right),$$

where $C_{g,N+1}=C_L$ and $f_j=C_{g,j+1}/C_{g,j}$. Given a fixed number of inverters, N, it turns out that in order to minimize t_p, $f_j=f_{j+1}$ for all $j=1,\ldots,N$. That is, the effective fanout f_j is the same for all inverters in the chain, so each inverter should be successively scaled up by the same factor relative to the previous inverter in the chain.

(a) Using calculus, prove that $C_{g,j+1}/C_{g,j} = C_{g,j}/C_{g,j-1}$ for $j=2,\ldots,N$ (Hint: minimize t_p w.r.t. each $C_{g,j}$)

(b) Prove that the effective fanout, f_j, evaluates to $f_j = \sqrt[N]{\frac{C_L}{C_{g,1}}}$.

Hand in printouts of your schematics, the circuit simulation input/output waveforms, results of DRC and LVS and answers to the questions. Please print the input/output waveforms as sub-plots. Finally, as with Homework #1, name your libraries according to the specific naming convention discussed in class and put them in the /gpfs/data/engn1600 directory for Marc to look over.

Comments on layouts:

- The goal is to create a minimum physical implementation of all the layout designs, using minimal wires, transistors, contacts, etc. Not doing so will decrease your homework grade, circuit speed and performance as well as increase circuit size. Be sure your design passes all design rules.
- Well organized layout is the best way to keep your circuits functioning correctly and quickly. Poorly organized layout is hard to debug and grade(!!!).
- Label your signals and your internal nodes so that your layout as well as your schematic is readable.