ENGN1600 – Design and Implementation of Very Large-Scale Integrated Systems

Designation: Required for Electrical Engineering concentrators in the Microelectronic Systems track; elective for Electrical Engineering concentrators in the Computer Engineering and Solid-State Electronics and Optoelectronics tracks

Instructor: Professor R. I. Bahar

Course Description: This course focuses on the design of complex digital systems. We will discuss such topics as CMOS devices and manufacturing technology, logic gates and their layout, propagation delay, reliability issues, and power dissipation. The goal of this course is to learn how to design and implement CMOS digital circuits and optimize them with respect to different constraints such as size, speed, power dissipation, and reliability. Using a complete VLSI design toolset, students will be required to complete a major course project that implements a particular functional design from specification down to layout. Students will be given the opportunity to fabricate their final designs using MOSIS technology.

Prerequisites: ENGN 1630, or permission from the instructor.

Textbook: *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Weste/Harris, Addison Wesley.

Class Schedule: 3×50 min lectures weekly, plus design laboratory exercises.

Topics:

1. The MOSFET transistor and the fabrication process
2. The CMOS inverter
3. Static and dynamic CMOS gates
4. MOS capacitance and resistance
5. Designing fast and/or energy efficient logic
6. Sequential CMOS circuits
7. Memory design
8. Arithmetic logic
9. Design for low power, test, margins, scaling, etc.
10. New frontiers in integrated circuit design

Relation to Program Outcomes:

Addresses ABET outcomes (a), (b), (c), (e), (g), (j), (k)

Course Goals: Students completing EN1600 should

1. Have the ability to synthesize static and dynamic logic cells based on knowledge of MOS device physics, modeling, and circuit topologies.
2. Be capable of designing and implementing combinational and sequential CMOS digital circuits and optimize them with respect to different constraints, such as area, delay, and power.
3. Be capable of implementing a complete design verification process using computer-automated tools for layout, extraction, simulation, and timing analysis.
4. Design and verify a prototype silicon integrated circuit suitable for fabrication using a 0.45 nm CMOS process.

Professionalism Component: Engineering Topics

Summary of improvements 2012-2013:

- Updated the libraries used for the laboratory assignments to use a 45nm technology node for the layout and SPICE simulation.
- Updated the lecture presentation to allow for more interactive discussion with the students.
- Updated the lab assignments to make them more challenging as well as more relevant to current practices in low power design.

Prepared By: R. I. Bahar, May 19, 2014.