EN1600
Design and Implementation of VLSI Systems
Fall 2016

Lecture 11, 12: Introduction to Dynamic Logic

Reading: Chap. 9, section 9.2 (esp. 9.2.4) — Weste & Harris

October 17, 19 2016 — Prof. R. Iris Bahar

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Technique #5 : Logical Effort

- The optimum effective fan-out for a chain of *N* inverters driving a load C_L is $f = \sqrt[N]{C_L / C_{in}}$
  - Set *N* such that the fan-out per stage is around 4, whenever possible (FO4)
- Can we generalize this approach (logical effort) to any gate?
  - The inverter equation is
    $t_p = t_{p0}(1 + C_{ext}/\gamma C_g) = t_{p0}(1 + f/\gamma)$
    we can generalize it to…

$$t_p = t_{p0}(p + g\,f/\gamma)$$

  - t_{p0} is the intrinsic delay of an inverter
  - *f* is the effective fan-out (C_{ext}/C_g) – also called the electrical effort
  - *p* is the ratio of the intrinsic delay of the gate relative to a simple inverter (a function of the gate topology and layout style): parasitic delay
  - *g* is the logical effort

Path delay (equation derivation)

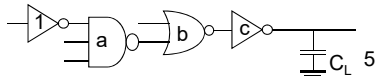
- The path logical effort, $G = \prod g_i$
- Path effective fanout (path electrical effort) is $F = C_L/C_{g1}$ [1]
- The branching effort accounts for fan-out to other gates in the network: $b = (C_{on\text{-}path} + C_{off\text{-}path})/C_{on\text{-}path}$
- The path branching effort is then $B = \prod b_i$
  …and the total path effort is then $H = GFB$ [1]
- The gate effort that minimizes path delay is $h = \sqrt[N]{H}$
- So, the minimum delay through the path is

$$D = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N\left(\sqrt[N]{H}\right)}{\gamma}\right)$$

[1] Note the textbook swaps the definitions of F,H and f_i, h

Path delay of logic gate network (cont.)

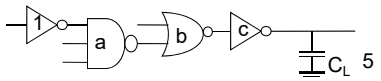
- For gate *i* in the chain, its size is determined by $h = f_i g_i b_i$



- For this network what do we need to compute h?
  - $F = C_L/C_{g1} = 5$
  - $G = 1 \times 5/3 \times 5/3 \times 1 = 25/9$
  - $B = 1$ (no branching)
  - $H = GFB = 125/9$, so the optimal stage effort is $h = \sqrt[4]{H} = 1.93$
  - Fanout factors are computed as $f_i = h/(g_i b_i)$. Since $b_i = 1$ we have:
    $f_1 = h/g_1 = 1.93$, $f_2 = 1.93 / (5/3) = 1.16$,
    $f_3 = 1.93/(5/3) = 1.16$, $f_4 = 1.93$

Path delay of logic gate network (cont.)

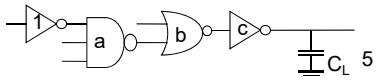
- Given f_i for each gate i in the chain, what is the final sizing?



- f_1=1.93, f_2=1.16, f_3 = 1.16, f_4 = 1.93
- So the gate sizes are (*working from outputs to inputs*):
  - c: $f_4=c_{ext,4}/c_{g,4} = c_L/c_{g,4}$ = 1.93 ➔ $c_{g,4}=5/1.93=2.59$
  - b: $f_3=c_{ext,3}/c_{g,3} = c_{g,4}/c_{g,3}$ = 1.16 ➔ $c_{g,3}=2.59/1.16=2.23$
  - a: $f_2=c_{ext,2}/c_{g,2} = c_{g,3}/c_{g,2}$ = 1.16 ➔ $c_{g,2}=2.23/1.16=1.93$
  - g_1: $f_1=c_{ext,1}/c_{g,1} = c_{g,2}/c_{g,1}$ = 1.93 ➔ $c_{g,1}=1.93/1.93=1.00$

Path delay of logic gate network (cont.)

- So what are the actually scaling sizes of the gates?

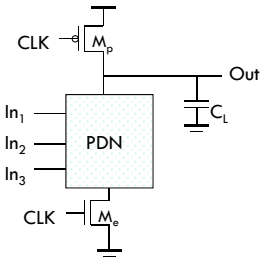


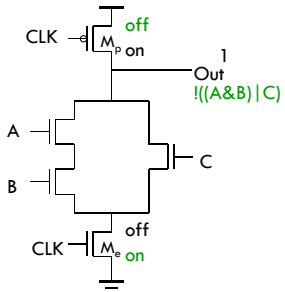
$$c_{g,i} = c_{g,i+1}\frac{g_i}{h}$$

$$\text{scale}_i = \frac{c_{g,i+1}}{h}$$

- Consider again the intrinsic capacitance values we calculated
  - $c_{g,4}$=5/1.93=2.59, $c_{g,3}$=2.59/1.16=2.23, $c_{g,2}$=2.23/1.16=1.93, $c_{g,1}$=1.93/1.93=1.00 relative to a *minimum sized inverter*
  - We need to adjust to the gate type:
  - $c_{g,4}$ = 2.59 ➔ gate c is 2.59X size of minimum sized inverter, so S_c=2.59 since gate c is an inverter as well.
  - $c_{g,3}$ = 2.23 ➔ gate b is 2.23X size of minimum sized NOR, which is 5/3 as big as min sized INV so S_b = 2.23 X 3/5 = 1.34
    - NOR is 1.34X size of minimum sized NOR
  - $c_{g,2}$ = 1.93 ➔ gate a is 1.93X size of minimum sized NAND3, which is 5/3 as big as min sized NAND so S_a = 1.93X 3/5 = 1.16
    - NAND is 1.16X size of minimum sized NAND3

Dynamic gate





Two phase operation

Precharge (CLK = 0)

Evaluate (CLK = 1)

Properties of dynamic gates

- Logic function is implemented by the PDN only
  - How many transistors are needed to implement an N-input function in dynamic logic?
  - What does this imply about total area and load capacitance, C_L?
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Faster switching speeds
  - Fewer transistors means reduced logical effort.

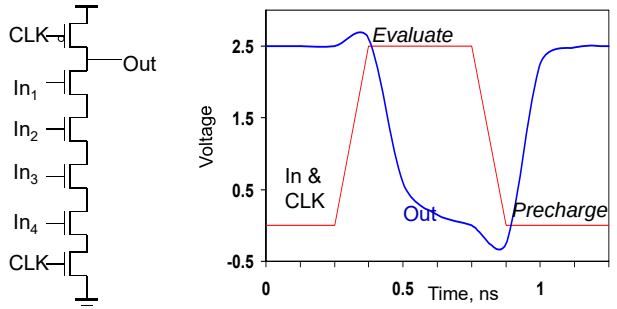
    What is the logical effort of a 2-input dynamic NOR gate?

  - no short circuit current, I_{sc}, so all the current provided by PDN goes into discharging C_L
  - We assume t_{pLH} = 0, but the presence of the evaluation transistor slows down the t_{pHL} (extra transistor in series).

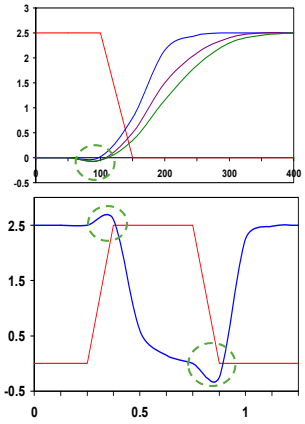
Conditions on output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
  - What does this imply about the inputs to the gate transitioning during evaluation?
- Output can be in the high impedance state during the evaluation stage if the PDN is turned off
  - → State is stored on C_L

Dynamic behavior



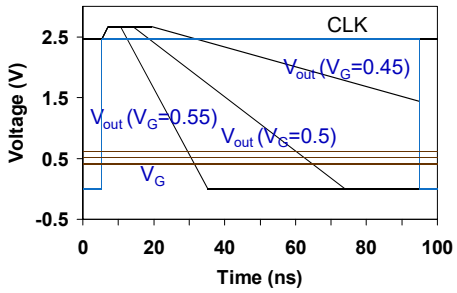
Input/Output Coupling: Bootstrapping



- What's with the overshoot and undershoot?
  - Notice input changes with steep voltage step
  - Takes a while for output to react to change in input value
  - Gate-drain capacitances of the transistors couple input directly to output in the short time before transistors have a chance to switch
  - Extra charge must be supplied to discharge the bootstrap capacitor
  - See section 4.4.6.6

Susceptibility to Noise

- The amount by which the output voltage drops is a strong function of the input voltage and the available evaluation time.
  - Noise needed to corrupt the signal has to be larger if the evaluation time is short



Power and energy

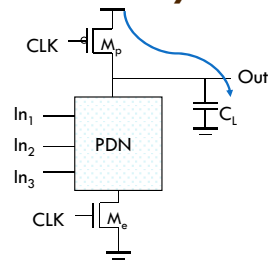
- Power dissipation: how much energy is consumed per operation and how much heat the circuit dissipates
- Two important components: static and dynamic

$$E\ (\text{joules}) = C_L V_{dd}^2 P_{0\to1} + t_{sc} V_{dd} I_{peak} P_{0\to1} + V_{dd} I_{leakage}$$

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P(\text{watts}) = C_L V_{dd}^2 f_{0\to1} + t_{sc} V_{dd} I_{peak} f_{0\to1} + V_{dd} I_{leakage}$$

Power dissipation of dynamic gate



Power only dissipated when previous Out = 0

$$E = C_L V_{DD}^2 P_{0\to1}$$

Probability the output transitions from 0 to 1

Dynamic power is data dependent

Dynamic 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$P_{A=1} = 1/2$

$P_{B=1} = 1/2$

Then transition probability

$P_{0\to1} = P_{out=0} \times P_{out=1}$

$= 3/4 \times 1 = 3/4$

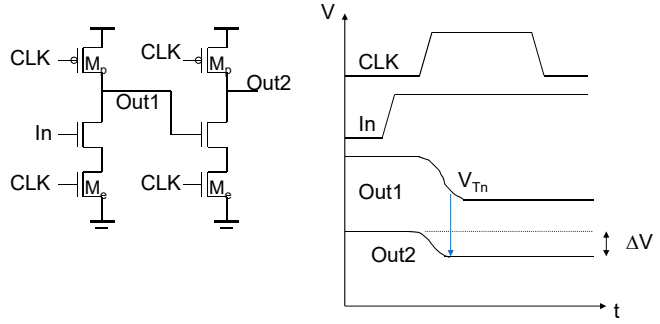
Switching activity can be higher in dynamic gates!

$P_{0\to1} = P_{out=0}$

Properties of dynamic gates (cont.)

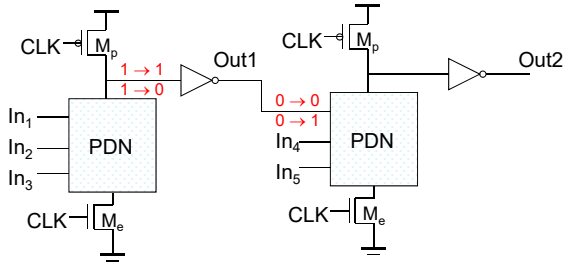
- Power dissipation should be better
  - no short circuit power consumption since the pull-up path is not on when evaluating
  - lower C_L
  - by construction can have at most one transition per cycle → no glitching
- But power dissipation can be significantly higher due to
  - higher transition probabilities
  - extra load on CLK
- Needs a precharge clock

Cascading dynamic gates

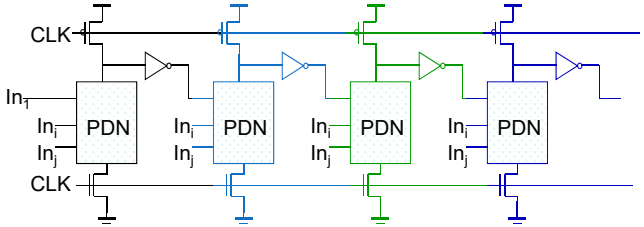


Only a single 0 → 1 transition allowed at the inputs during the evaluation period!

Domino Logic

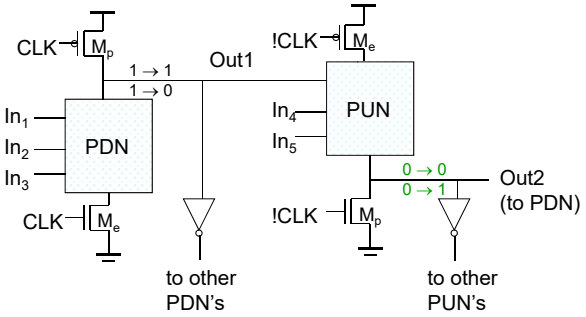


Why Domino?



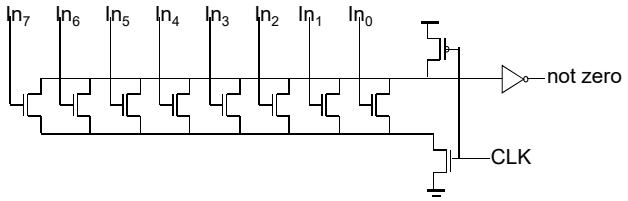
Like falling dominos!

NP-CMOS (Zipper)



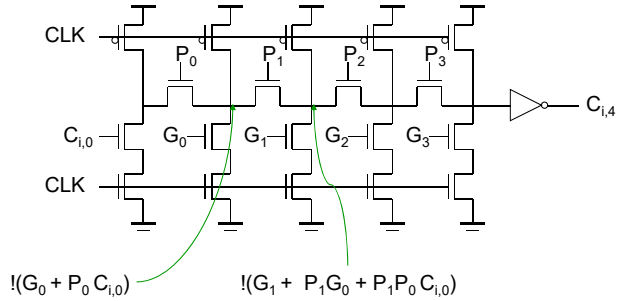
Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN

Dynamic Zero Detector



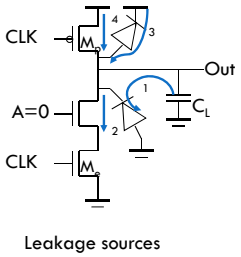
- Efficient use of a dynamic gate.
- Wide NOR gate that uses minimum sized gate
- Low logical effort

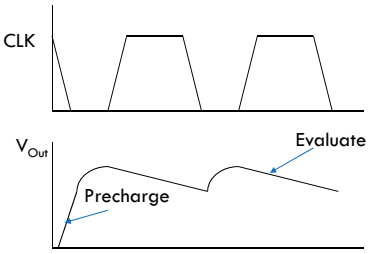
Dynamic Manchester Carry Chain



Charge leakage

- Ideally, if the PDN is off, the output should remain high (V_{DD}) for the duration of the evaluate stage
- Leakage currents cause charge to degrade over time

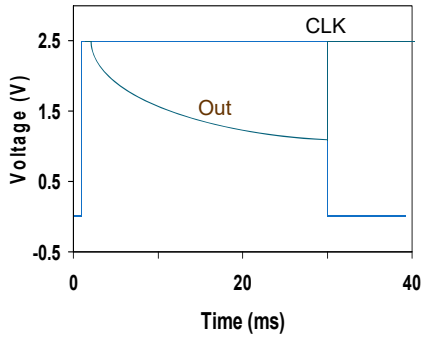




Minimum clock rate of a few kHz

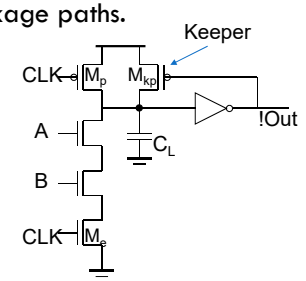
Impact of charge leakage

- Output settles to an intermediate voltage determined by a resistive divider of the pull-up and pull-down networks
  - If output drops below switching threshold, output interprets as low



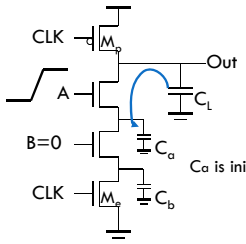
A solution to charge leakage

- Keeper compensates for the charge lost due to the pull-down leakage paths.



How should the keeper device be sized relative to the NMOS devices?

Charge sharing



Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to possible circuit malfunction.

C_a is initially discharged

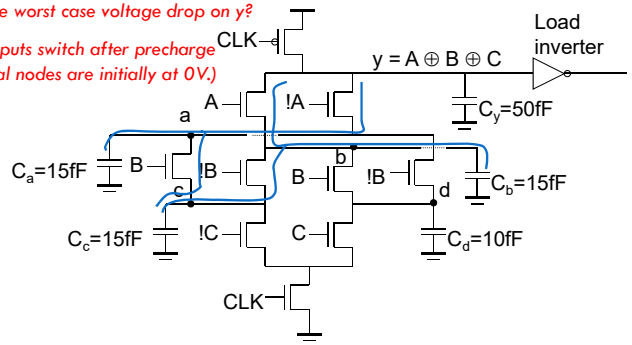
$$\text{If } \Delta V_{out} = V_{DD}\left(\frac{C_a}{C_a + C_L}\right) > V_{Tn},$$

this could cause the gate it drives to malfunction.

Charge sharing example

What is the worst case voltage drop on y?

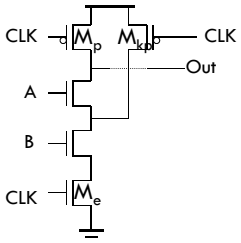
(Assume inputs switch after precharge and internal nodes are initially at 0V.)



ΔV_{out} = - V_{DD} ((C_a + C_c)/((C_a + C_c) + C_y))

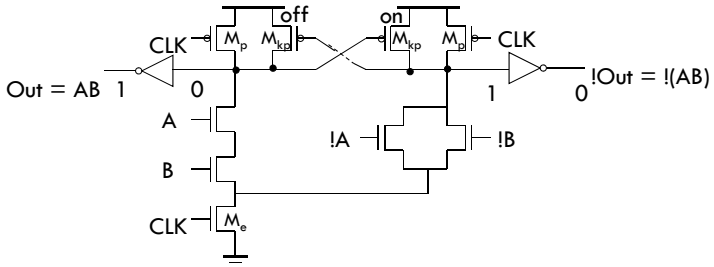
= - 2.5V*(30/(30+50)) = -0.94V

Solution to charge redistribution



Precharge internal nodes using a clock-driven transistor (at the cost of increased area and capacitance)

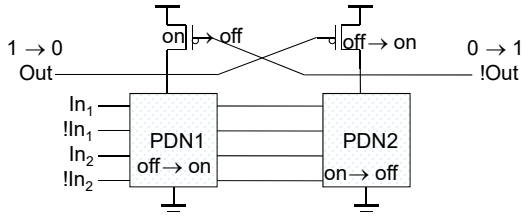
Differential (dual rail) domino



Due to its high-performance, differential domino has been very popular in the design of in several commercial microprocessors.

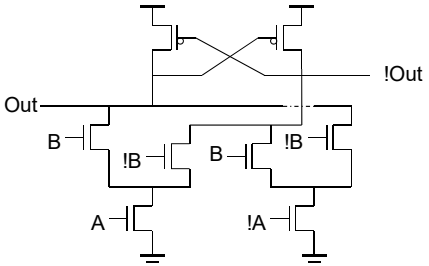
DCVS logic

- DCVS: Differential Cascade Voltage Switch logic



PDN1 and PDN2 are mutually exclusive

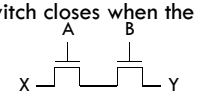
DCVS example



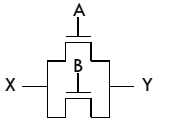
- Some transistors are shared between Out and !Out
- Overall lower transistor count

NMOS transistors in series/parallel

- So far we have assumed that primary inputs are only allowed to drive gate terminals of MOS transistors.
- Now assume primary inputs can drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



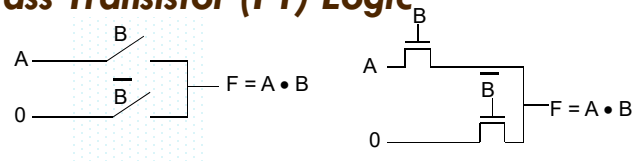
X = Y if A and B



X = Y if A or B

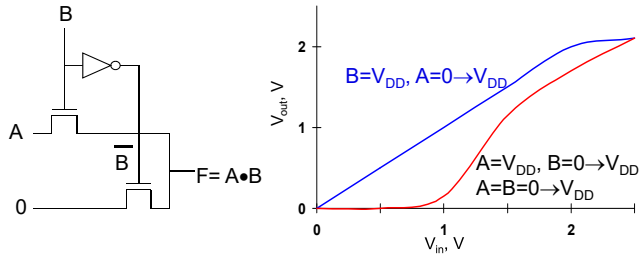
- Remember - NMOS transistors pass a strong 0 but a weak 1

Pass Transistor (PT) Logic



- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Bidirectional (versus non-directional)

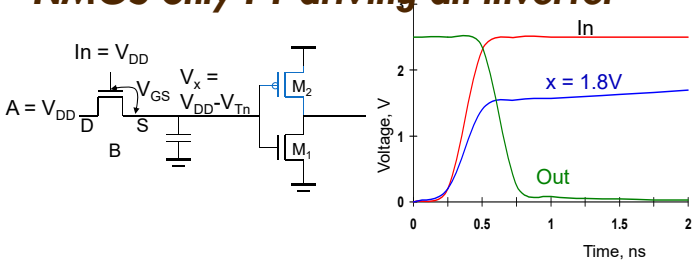
VTC of pass transistor AND gate



- Pure PT logic is not regenerative: signal gradually degrades after passing through a number of PTs

➡ fix with static CMOS inverter insertion

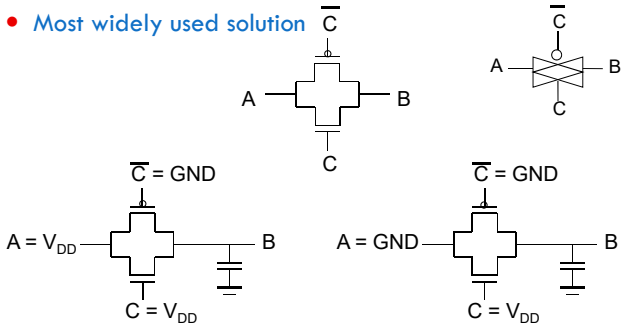
NMOS only PT driving an inverter



- V_x does not pull up to V_{DD}, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power dissipation (M_2 may be weakly conducting forming a path from V_{DD} to GND)

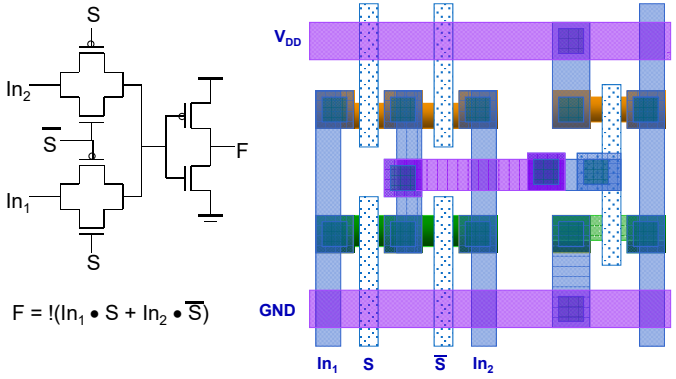
Transmission gates (TGs)

- Most widely used solution

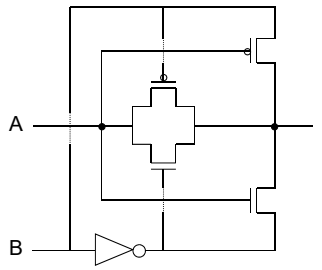


- Full swing *bidirectional* switch controlled by gate signal C: A = B if C = 1

TG multiplexer



Transmission gate example

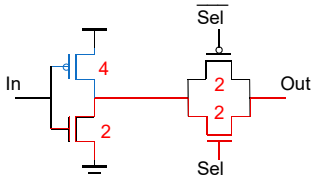


What is this function?

$F = A \oplus B$

Logical Effort and Transmission gates

- What is the logical effort for In and Sel?

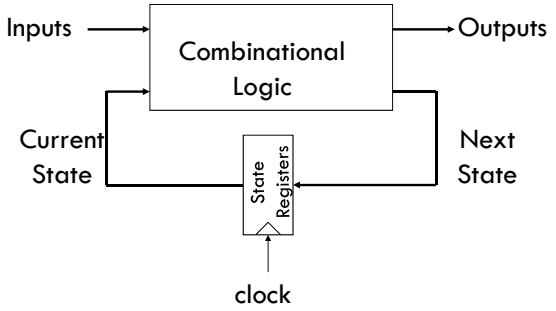


$g_{In} = 2$

$g_{Sel} = 2/3$

- Consider the NMOS pass transistor as part of the pull-down network
- In transmission gates the PMOS and NMOS have the same size since they conduct at the same time

Sequential logic



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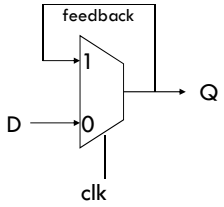
MUX based latches

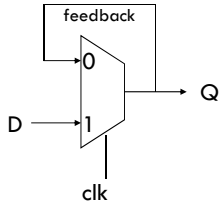
- Change the stored value by cutting the feedback loop



Negative Latch

Q = clk & Q | !clk & D

transparent when the clock is low



Positive Latch

Q = !clk & Q | clk & D

transparent when the clock is high

BROWN

TG MUX based latch implementation