EN1600
Design and Implementation of VLSI Systems
Fall 2016

Lecture 13: static latch design

Reading: Chapter 10, sections 10.1-10.3* October 24, 2016

Weste & Harris Prof. R. Iris Bahar

*includes extra material not discussed in class

BROWN

© 2016 R.I. Bahar
Portions of these slides taken from Professors J. Rabaey, J. Irwin, V. Narayanan, and S. Reda

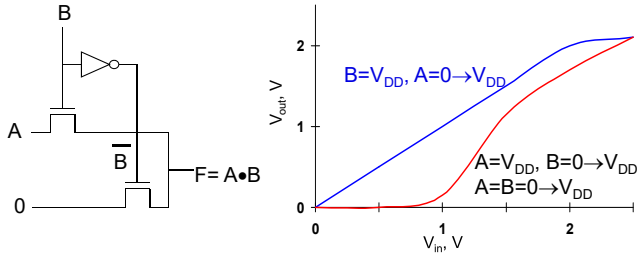
BROWN

Exam this Wednesday

- In class exam
  - Closed book, calculators OK
- Solutions to HW#3 will be posted later today.

BROWN

VTC of pass transistor AND gate

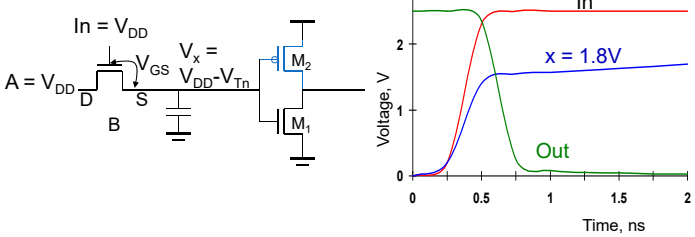


- Pure PT logic is not regenerative: signal gradually degrades after passing through a number of PTs

➡ fix with static CMOS inverter insertion

BROWN

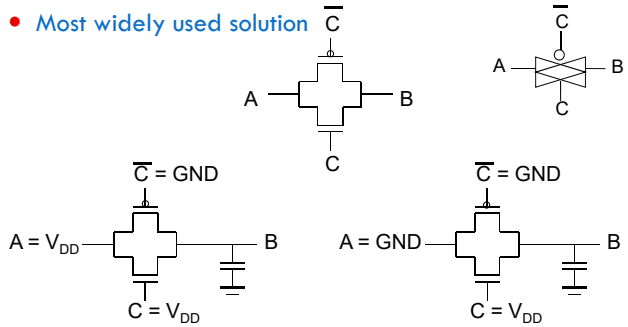
NMOS only PT driving an inverter



- V_x does not pull up to V_{DD}, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power dissipation (M_2 may be weakly conducting forming a path from V_{DD} to GND)

Transmission gates (TGs)

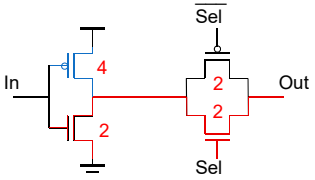
- Most widely used solution



- Full swing *bidirectional* switch controlled by gate signal C: A = B if C = 1

Logical Effort and Transmission gates

- What is the logical effort for In and Sel?

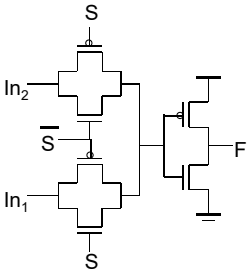


$g_{In} = 2$

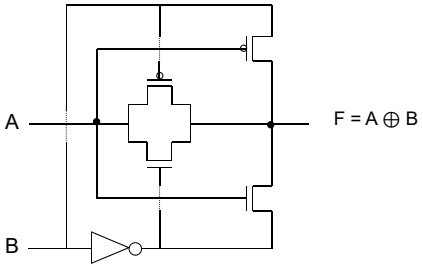
$g_{Sel} = 2/3$

- Consider the NMOS pass transistor as part of the pull-down network
- In transmission gates the PMOS and NMOS have the same size since they conduct at the same time

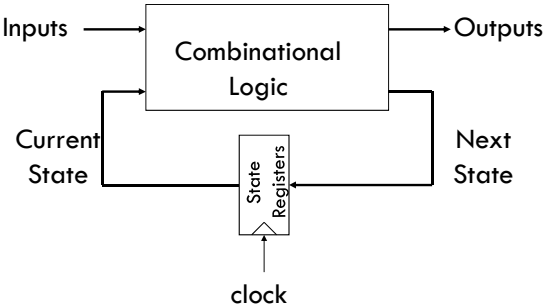
Common Functions with TGs



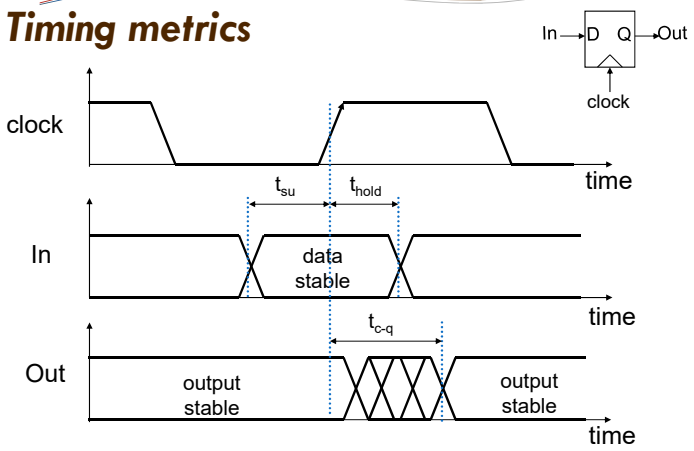
$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$



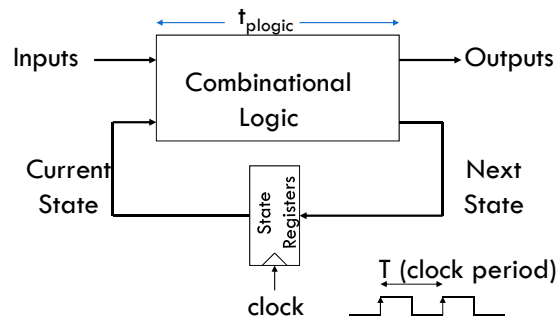
Sequential logic



Timing metrics



System timing constraints



$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$

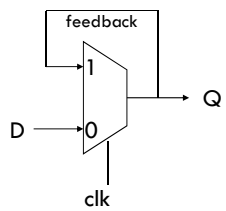
$t_{cdreg} + t_{cdlogic} \geq t_{hold}$

Latches vs. flip-flops

- Latches
  - level sensitive circuit that passes inputs to Q when the clock is high (or low) → *transparent* mode
  - input sampled on the falling edge of the clock is held stable when clock is low (or high) → hold mode
- Registers (edge-triggered)
  - edge sensitive circuits that sample the inputs on a clock transition
    - positive edge-triggered: 0 → 1
    - negative edge-triggered: 1 → 0
  - also called flip-flops
  - built using latches (e.g., master-slave flip-flops)

MUX based latches

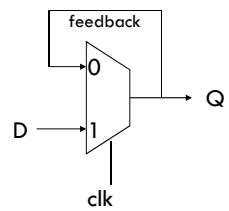
- Change the stored value by cutting the feedback loop



Negative Latch

Q = clk & Q | !clk & D

transparent when the clock is low

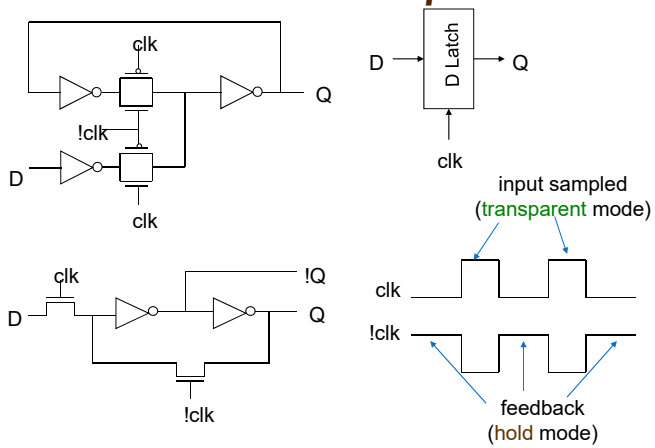


Positive Latch

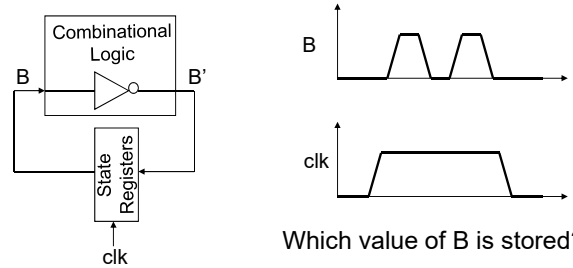
Q = !clk & Q | clk & D

transparent when the clock is high

TG MUX based latch implementation



Latch race problem



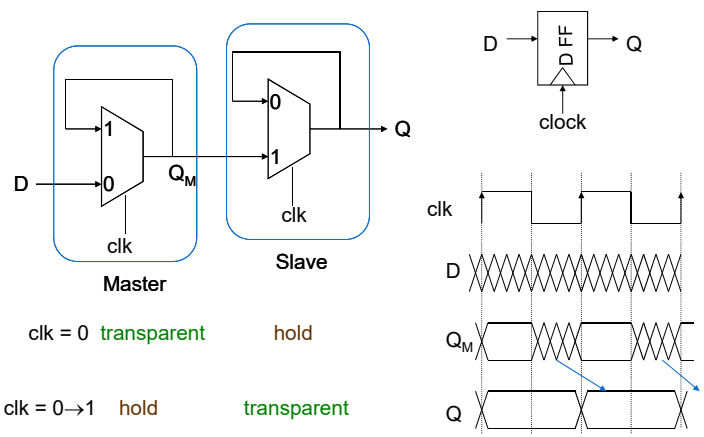
Which value of B is stored?

Two-sided clock constraint

$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

$$T_{high} < t_{c\text{-}q} + t_{cdlogic}$$

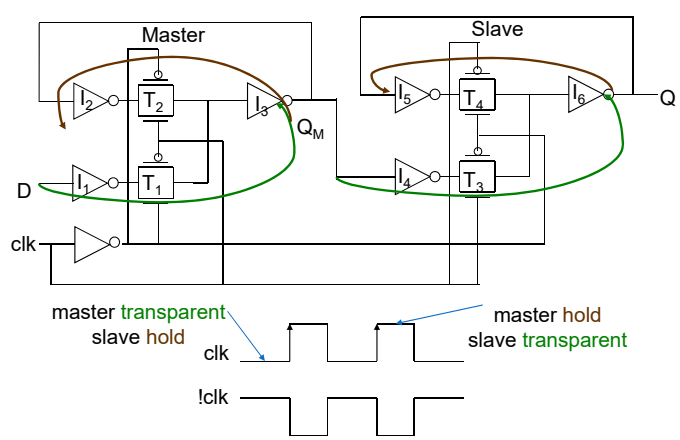
Master slave edge-triggered flip-flop



clk = 0 transparent hold

clk = 0→1 hold transparent

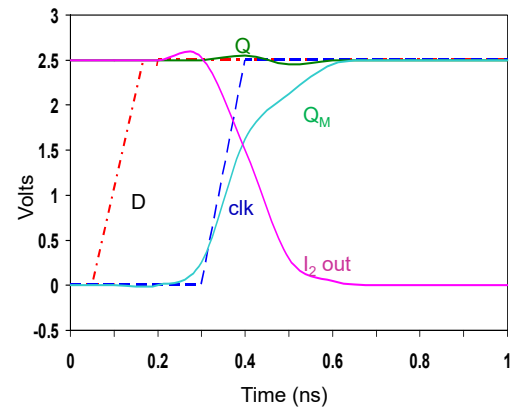
Master slave edge-triggered design



Master slave timing properties

- Assume propagation delays are t_{pd_inv} and t_{pd_tx}, that the contamination delay is 0, and that the inverter delay to derive !clk is 0
- Set-up time - time before rising edge of clk that D must be valid $3 * t_{pd_inv} + t_{pd_tx}$
- Propagation delay - time for Q_M to reach Q $t_{pd_inv} + t_{pd_tx}$
- Hold time - time D must be stable after rising edge of clk zero

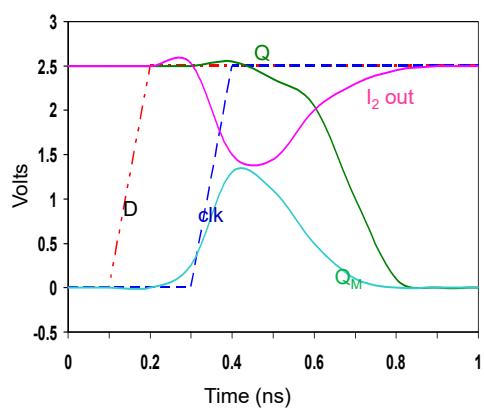
Setup time simulation



t_{setup} = 0.22 ns

works correctly

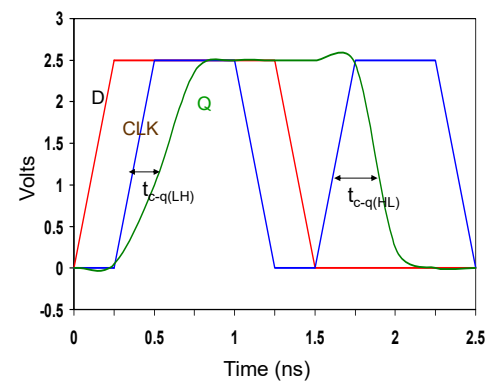
Setup time simulation



t_{setup} = 0.20 ns

fails

Propagation delay simulation



$t_{c\text{-}q(LH)}$ = 160 psec

$t_{c\text{-}q(HL)}$ = 180 psec