EN1600
Design and Implementation of VLSI Systems
Fall 2016

Lecture 22: Datapath Logic

Reading: Chapter 11, sections 11.8, 11.9
Chapter 1, section 1.10
Weste & Harris

November 28, 2016
Prof. R. Iris Bahar

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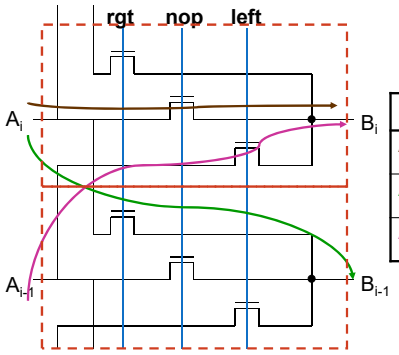
What's coming up?

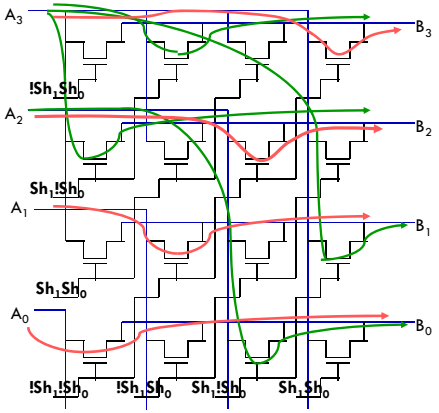
- Remaining lectures:
  - Datapath Logic
  - Design for reliability, low power circuits, emerging topics…
  - Process technologies beyond bulk CMOS
- Final exam: ***Wednesday, November 30 (in class)***
- Project status report: ***Wednesday, December 7, 5pm***
- Final Presentations: ***Tuesday, December 13, 9am-noon***
- Final Reports due by: ***Thursday, December 15, 5pm***
  - Include slides, proposal, progress reports in appendix

A Programmable Binary Shifter



A_i	A_{i-1}	rgt	nop	left	B_i	B_{i-1}
A_1	A_0	0	1	0	A_1	A_0
A_1	A_0	1	0	0	0	A_1
A_1	A_0	0	0	1	A_0	0

4-bit Barrel Shifter



Example:

$!Sh_1!Sh_0 = 1$
$B_3B_2B_1B_0 = A_3A_2A_1A_0$

$!Sh_1Sh_0 = 1$
$B_3B_2B_1B_0 = A_3A_3A_2A_1$

$Sh_1!Sh_0 = 1$
$B_3B_2B_1B_0 = A_3A_3A_3A_2$

$Sh_1Sh_0 = 1$
$B_3B_2B_1B_0 = A_3A_3A_3A_3$

Area dominated by wiring

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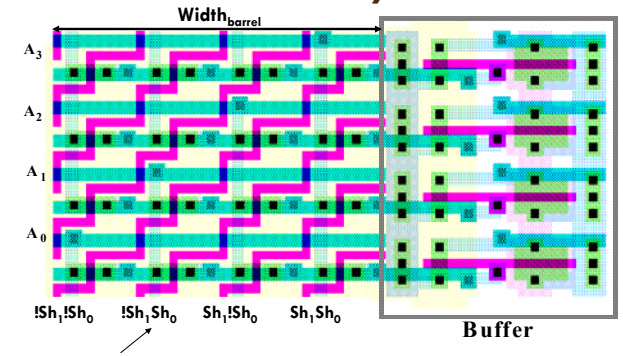
4-bit Barrel Shifter Layout



Only one Sh# active at a time

Width$_{barrel}$ ~ 2 p_m N

N = max shift distance, p_m = metal pitch

Delay ~ 1 device + N diff caps

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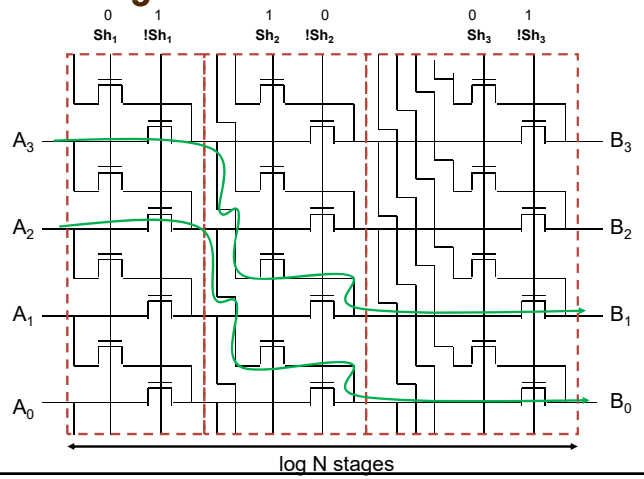
8-bit Logarithmic Shifter



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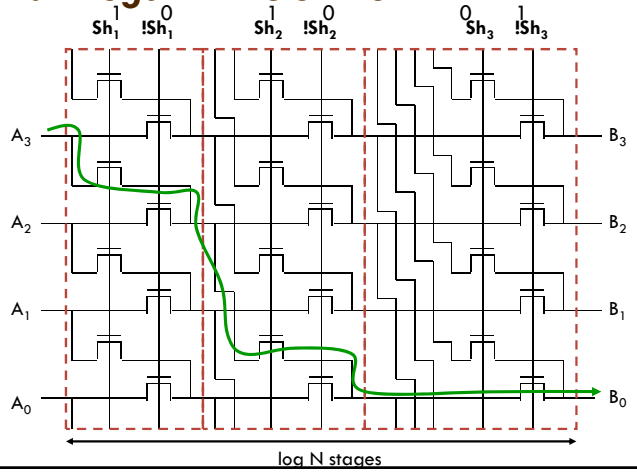
8-bit Logarithmic Shifter



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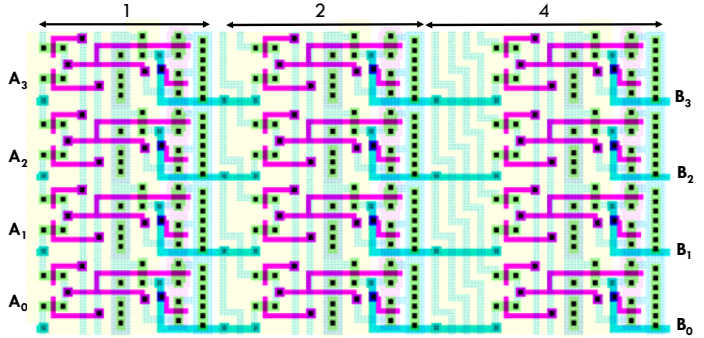
8-bit Logarithmic Shifter Layout Slice



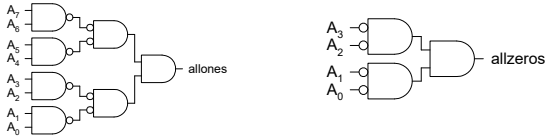
Width$_{log}$ ~ $p_m(2K+(1+2+…+2^{K-1})) = p_m(2^K+2K-1)$

K = $\log_2$ N

Delay ~ K devices + 2 diff caps

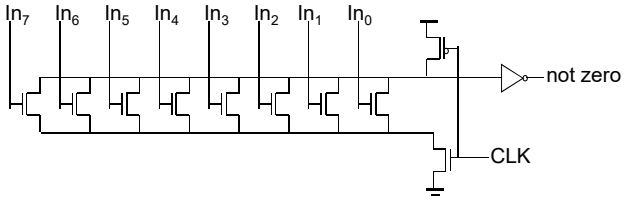
A. 1's and 0's detectors

- 1's detector: N-input AND gate
- 0's detector: NOTs + 1's detector (N-input NOR)



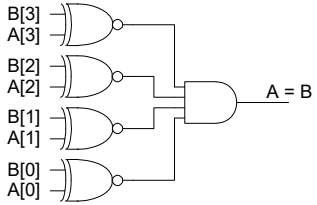
- *Is there a better/faster way?*

Domino Zero Detector



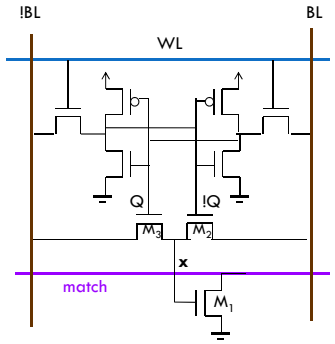
B. Equality comparator

- Check if each bit is equal (XNOR, aka equality gate)
- 1's detect on bitwise equality



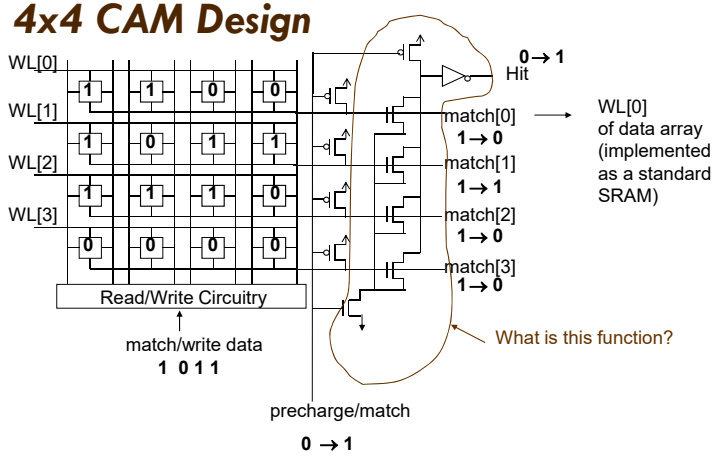
- *Where have you seen this function before?*

9-T CAM cell

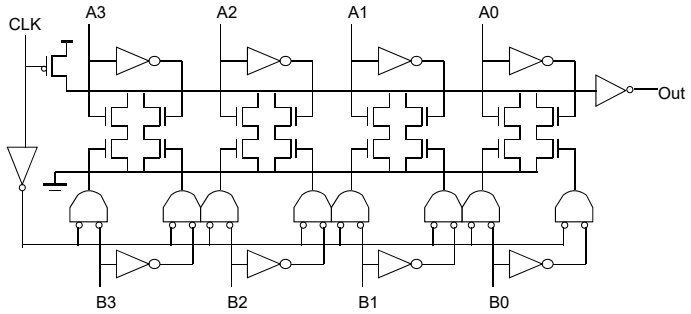


- Writes progress as in a standard SRAM cell
- Compares the stored data (Q and !Q) to the bit line data
  - Precharged match line ties to all cells in a row
  - If Q and BL match, **x** is discharged through M_2 or M_3 and thus M_1 is OFF keeping the match line high
  - Else if Q and BL don't match, **x** is charged to $V_{DD} - V_T$ and the match line discharges

4x4 CAM Design



Domino comparator



Floorplanning

- Plan at a high level before doing layout and allow for routing

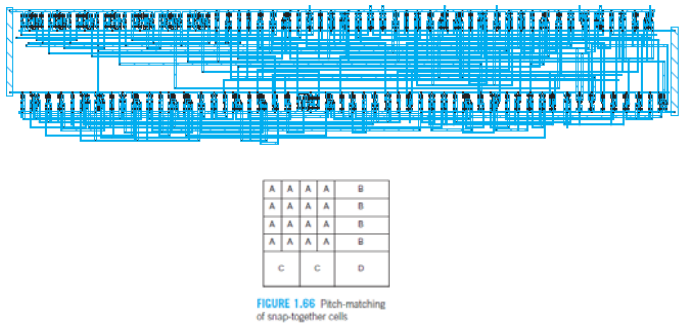
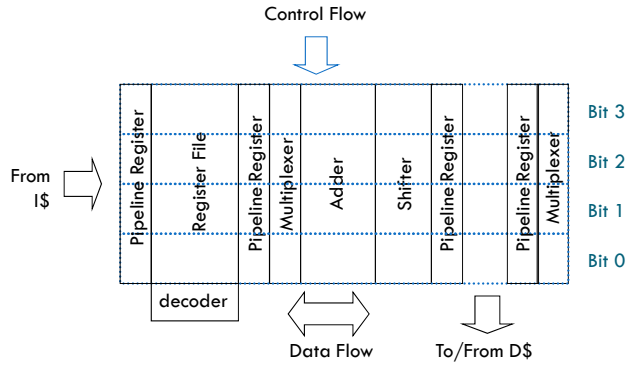


FIGURE 1.66 Pitch-matching of snap-together cells

Datapath Bit-Sliced Organization



Tile identical bit-slice elements

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Datapath Layout

- Pitch matching is very important

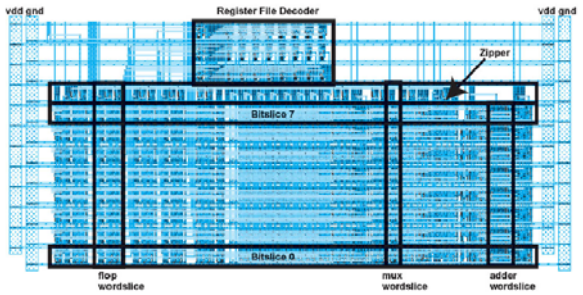

FIGURE 1.67 MIPS datapath layout

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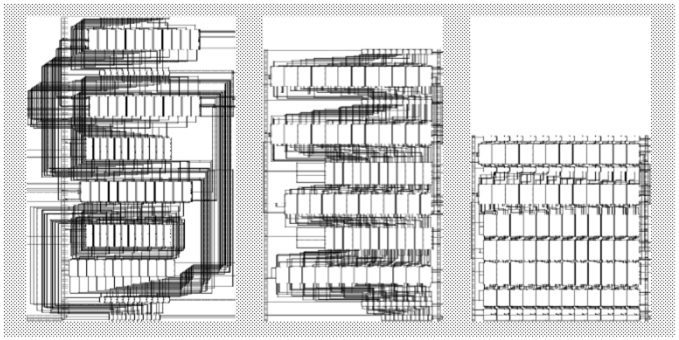
Layout of Bit-sliced Datapaths

Without feedthroughs or pitch matching (4.2μm²)

With feedthroughs (3.2μm²)

With feedthroughs and pitch matching (2.2μm²)



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Slice Plans

- Shows ordering of wordslices and wiring allocation
- Dots indicate that bus data is used in that cell

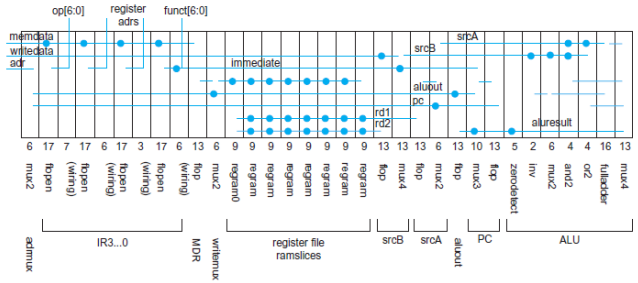

FIGURE 1.68 Datapath slice plan