ENGN1600 – Design and Implementation of VLSI Systems
Fall Semester 2016

CLASS TIMES:	MW 8:30 – 9:50 a.m.	Barus & Holley 155
INSTRUCTOR:	R. Iris Bahar 863-1430 OFFICE HOURS:	Barus & Holley 322 Iris_Bahar@brown.edu M 10:00am–12:00 p.m., or by appointment
TEACHING ASSISTANT:	Marc Powell 863-6178 OFFICE HOURS:	office: BERT 358 Marc_Powell@brown.edu Tu 2-4pm (@BERT), F 10am-noon (B&H 191) (Tuesday only when no homework is due)

COURSE DESCRIPTION: This course focuses on the design of complex digital systems. We will discuss such topics as CMOS devices and manufacturing technology, logic gates and their layout, propagation delay, reliability issues, and power dissipation. The goal of this course is to learn how to design and implement CMOS digital circuits and optimize them with respect to different constraints such as size, speed, power dissipation, and reliability. Using a complete VLSI design toolset, students will be required to complete a major course project that implements a particular functional design from specification down to layout. Students will be given the opportunity to fabricate their final designs using MOSIS technology.

PREREQUISITES: EN163 (may be taken concurrently) or permission from the instructor

REQUIRED TEXT: Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuit and Systems Perspective, 4th Edition,* Addison Wesley Publishers, 2011

RECOMMENDED *TEXT:* Jan Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits, 2nd Edition,* Prentice-Hall Publishers, 2003

COURSE WEBPAGE: http://www.brown.edu/Departments/Engineering/Courses/engn1600

TOPICS:

The MOSFET transistor and the fabrication process
The CMOS inverter
Static and dynamic CMOS gates
MOS capacitance and resistance
Designing fast and/or energy efficient logic
Sequential CMOS circuits
Memory design
Arithmetic logic
Design for low power, test, margins, scaling, etc.
New frontiers in integrated circuit design

HOMEWORK/LABS: Aside from the final project, there will be approximately 4-5 lab assignments given throughout the semester. The goal of these labs will be to familiarize students with SPICE circuit simulation and the Cadence schematic/layout tool suite as well to get some basic layout, transistor-level, and gate-level design experience.

PROJECT: Each student must complete a fully custom layout of a complex function for a final project. The project is to be completed by a team of 2-3 students. Progressive due dates will be assigned throughout the second half of the semester. Final project presentations will be scheduled according to the University's official exam schedule for group 03. More information about the project will be available later on in the semester.

GRADING:

Homework/Labs	40%
Final Project	20%
Midterm Exam	15%
Final Exam	20%
Class Participation	5%

The midterm exam is tentatively scheduled for **Wednesday, October 26**, and the final for **Wednesday, November 30**. Please let me know as soon as possible if you have a conflict with either of these dates. Presentations for the final projects will be held on **Tuesday, December 13, between 9am-12pm** (the officially scheduled time slot for the final). Attendance for all presentations is required by all students.

CODE OF ETHICS: It is expected that all work handed in for a grade will be of your own effort. It is fine to discuss with others general concepts regarding homeworks/labs; however, all assignments are to be done individually. Similarly, cheating will not be tolerated on exams. Finally, although the final project may be based on design concepts that have been previously developed, the actual implementation should be done from scratch by you and the rest of your team.

Tentative Schedule

Week	*Topic*	*Assignments*
1: Sept. 7	Introduction, metrics	
2: Sept. 12, 14	Design factors, fabrication and layout process for an inverter	Marc give tutorial 9/14 evening
3: Sept. 19, 21	the CMOS inverter and its static operation	**9/21/16: layout tutorial Due**
4: Sept. 26, 28	MOS capacitance and resistance, VTC curves	**9/28/16: HW#1 Due**
5: Oct. 3, 5	timing behavior in CMOS circuits	**10/5/16: HW#2 Due**
6: Oct. 12	*No class Oct. 10* timing in complex gates	
7: Oct. 17, 19	dynamic logic, introduction to latch design	**10/19/16: HW#3 Due**
8: Oct. 24, 26	Static and dynamic latches	**10/26/16: Midterm Exam**
9: Oct. 31, Nov. 2	power estimation	**11/2/16:**
10: Nov. 7,9	SRAM and cache design	**11/9/16: HW#4 Due**
11: Nov. 14, 16	Arithmetic logic	Final project description handed out
12: Nov. 21, 23	Other memory structures	**11/23/16: Project Proposal Due**
13: Nov. 28, 30	Design for low power and reliability	**11/30/16: Final exam**
14: Dec. 5,7	Emerging topics in VLSI design	**12/7/16: Project Status Report Due**
15: Dec. 13	**9am-12pm: Final Project Presentations**	