# **Cadence Virtuoso First CMOS Transistor Circuits** ENGN2912E Fall 2017

Last edited by Shanshan Dai, Sept.20, 2017.

### Introduction

This is a first introduction to using the NCSU freepdk 45nm CMOS design kit.

Note: you will need to launch the environment using "cadence\_freepdk45", for the appropriate libraries.

#### Make a new inverter schematic

In the Library Manager, go to File->New->Cell View, and create a new Schematic view in userlibrary, called first\_inverter.

🔲 🛛 Library Manager: WorkArea: /gpfs_home/guest490/freepdk45 👘 🕈 💶 🗙	New File	• X
<u>File Edit View Design Manager Help</u>	File	
New Library   Open Ctrl+O   Open (Read-Only) Ctrl+R   Category Category   Load Defaults St_inverter   Save Defaults St_inverter   Digen Shell Window Ctrl+P   Exit Ctrl+X   Chenny/sr demolib   sample sbal.ib   User/Ibrary User/Ibrary	Library userlibrary Cell first_inverter  View schematic Type schematic Application Open with Schematics L Always use this application for this type of fil Library path file /gpfs_home/guest490/freepdk15/cds.lib	e
Log file is "/gpfs_home/guest490/freepdk45/libManager.log".	OK Cancel H	elp

# Place a few symbols in your schematic

Pick and place symbol instances of analogLib/vdc, analogLib/gnd, NCSU\_Devices\_FreePDK45/PMOS\_VTH and NCSU\_Devices\_FreePDK45/NMOS\_VTH. Connect them like this:



Things to notice:

- The NMOS transistor has multiple properties, mostly importantly its width (W) and length (L). Make the device have W=90n and L=50n (default values).
- Connecting nodes can be done by going to Create->Wire(narrow), then clicking the nodes you want to connect.
- Add wire name: Create -> Wire Name, type the name and left-click the wire in schematic.
- Add pin: Create->Pin, type the name and put it in schematic.
- The wires with the same name are connected. For example, the plus node of the voltage source V2 and the nmos drain node are connected.

## Simulate your schematic

Objective: we want to plot the voltage transfer curve of an inverter (vin versus vout), by applying a DC sweep of vin.

#### Launch->ADE L

Since we started ADE L from the first\_inverter schematic, it will automatically refer to this design.

First, we need to assign the models for the transistors in the schematic

click on the Model libraries button then click on the browse button (Figure 19) and select the file at the following path:

/gpfs/runtime/opt/cadence/shared\_ccv/FreePDK45/ncsu\_basekit/models/hspice/hspice\_nom.include

This will select the nominal corner library. The other two available files are used for fast and slow corner libraries (where fast and slow refer to the relative threshold voltage variations).



Second, we need to setup the stimuli for our circuit:

- 1. Select dc from the Function menu;
- 2. Input Vin in the DC voltage field;
- 3. Check the Enable flag;
- 4. Apply changes;



For the simulator to recognize the variable vin, go to Variables->Edit and write vin in the Name field and assign 0 to Value (Expr) (this value will be overwritten during the DC sweep). Click on Add and OK.

ADE L (1) - userlibrary first_inverter schematic	↑ _ □ X	Editing Design Variables AD			• ×
Launch Session Setup Analyses Variables Outputs Simulation Results	cādence	Selected Variable		Design Variables	
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Name   Value     1   pSvonly   0		Add Dele	ar Find		
	*	Cellview Variat	Copy From Copy To	Apply & Run :	Simulation <u>H</u> elp

**Third**, set up a **dc** analysis and tell spectre to sweep the VDS voltage source "DC voltage" "Component Parameter" from 0V to 1V:



Tell ADE to plot **vout** by going to Outputs ->To Be Plotted -> Select on Schematic, and click on vout (highlighted in red as below).



Run the simulation to plot vin (x-axis) vs vout(y-axis):

