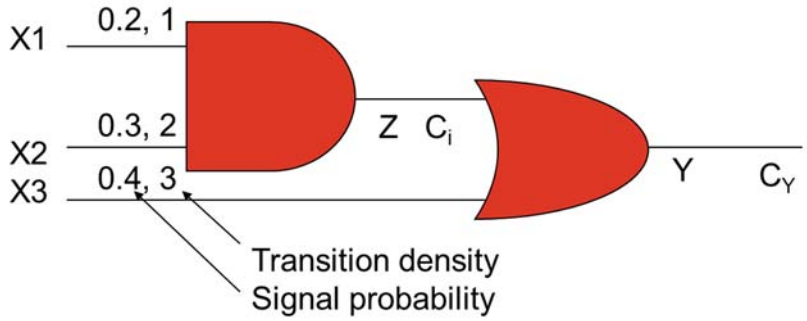
ENGN2912E: Low Power VLSI System Design

Homework Assignment #1

Due **Wednesday, September 20, 2017, in class**

1. Consider the following circuit with primary input signal probabilities and transition densities as show:
    a) What are the signal probabilities for signal nodes Z and Y?
    b) What are the transition densities for signal nodes Z and Y?
    c) What is the total power dissipated for the circuit due to switching activity?

    Note that we already computed *P*(Z) and *T*(Z) in class so you can check you calculation against those values. To compute P(Y) and T(Y) consider Y as a supergate containing both the AND and OR gates. The load capacitances at Z and Y are defined as C_Z and C_Y respectively.



2. Consider the following function $F = x_3' + x_1'x_2$
    Assume the following probability and switching values for the signals:
    $P(x_1)=0.5$, $P(x_2)=0.4$, $P(x_3)=0.6$, $T(x_1)=0.25$, $T(x_2)=0.75$, $T(x_3)=0.5$

    a) Draw a gate level implementation using only NAND and Inverter gates.
    b) Compute the signal probabilities for all the gates in the circuit.
    c) Compute the transition density for all the gates using the Boolean difference formulation.

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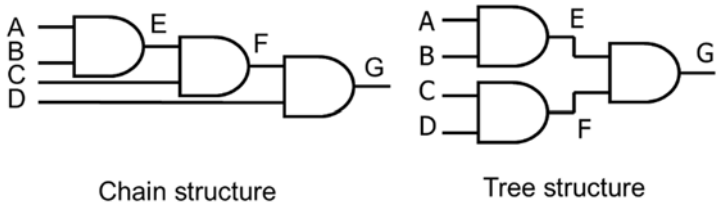
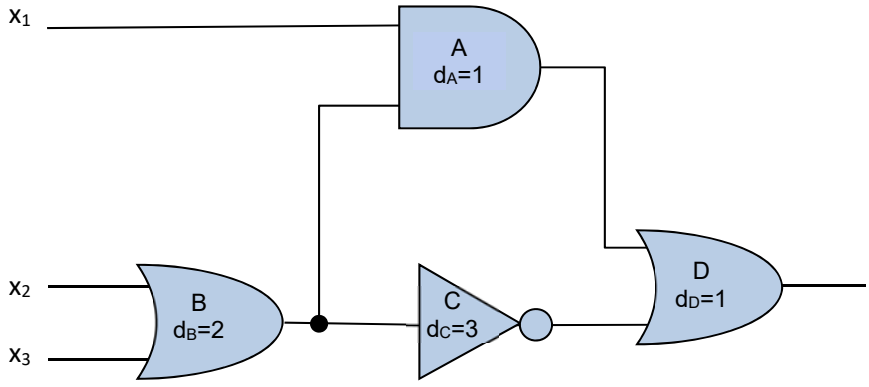
3. A 4-input AND function can be implemented with 2-input AND gates either using a chain structure or a tree structure, as shown below. Assume the following signal probabilities:
P(A)=0.4, P(B)=0.8, P(C)=0.5, P(D)=0.3



a) If the gates have zero delay values (i.e., their outputs switch instantaneously as a result of changes on the gates' inputs), which implementation will have higher switching activity? To answer this part of the problem, compute *p1* and *p01* for each gate.
b) Compare your answer to the solution we got in class when we assumed equiprobable signal values at the primary inputs.
c) If you are free to choose any input ordering you want for each of the two circuit implementations shown above, would that have any impact on the switching activity? That is, instead of ordering the inputs as A, B, C, D as is shown above you could choose a different order. If it does impact switching activity, suggest a new input ordering that may improve (i.e., reduce) dynamic power dissipation. Explain your reasoning.

4. Consider the circuit shown below:



a) Given our discussion in class this week regarding glitching, determine the worst case glitching activity for the circuit above, assuming all inputs transition from 0→1 or 1→0 at the same time. Note that the inertial delays for all gates A, B, C, D are given on the gate (eg., d_B = 2 means gate B has inertial delay of 2).
b) How would you suggest reducing the glitch activity in this circuit?