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Low Power VLSI System Design

Lecture 1: Introduction

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EN2912E
September 6, 2017

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Course Content

- Course focus
  - low power and thermal-aware design
  - digital design, from devices to architecture and system level issues
  - Assumes some basic knowledge of computer organization and circuit design
  - Learn basic ideas, concepts, theory and methods.
  - Gain experience with techniques and tools.
  - Learn about some of the latest research efforts in low-power, energy-efficient design

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Course Content

- Course focus
- Pre-requisites
- Goals

- Course webpage:
  http://www.brown.edu/Departments/Engineering/Courses/engn2912
  Note that this webpage has not been set up yet!

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Course Format

- "Regular" Lecture
  - Covers foundation topics in low power design
  - Expect 3 homework on topics from lecture

- Class discussion
  - Current papers in low power design
  - Discussion leader
  - Scribes
  - Paper summaries

- Final Project
  - Can relate to your own research interest (but can't duplicate it).

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Grading

- Homeworks (25%)
- Final Project (30%)
- Discussion Leadership (20%)
- Scribe Notes (15%)
- Class Participation (10%)

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Power Dissipation in VLSI Systems

Why should we care?

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ISSCC, Feb. 2001, Keynote

Patrick P. Gelsinger
Senior Vice President
General Manager
Digital Enterprise Group
INTEL CORP.

"Ten years from now, microprocessors will run at 10GHz to 30GHz and be capable of processing 1 trillion operations per second – about the same number of calculations that the world's fastest supercomputer can perform now.

"Unfortunately, if nothing changes these chips will produce as much heat, for their proportional size, as a nuclear reactor. . . ."

The power wall talk…

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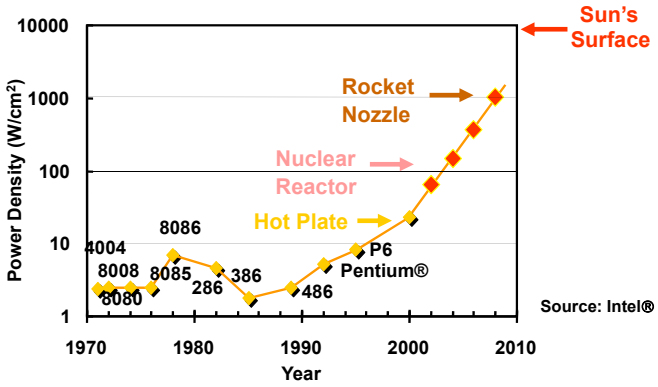
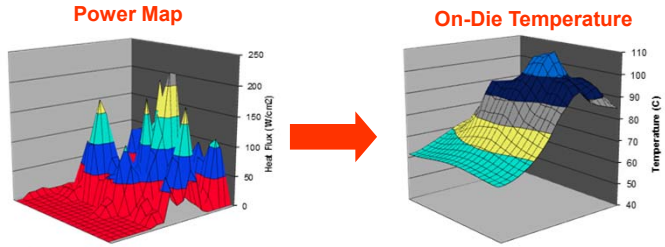
VLSI Chip Power Density



Why power matters

- Packaging costs
- Power supply rail design
- Chip and system cooling costs
- Noise immunity and system reliability
- Battery life (in portable systems)
- Environmental concerns

Chip power density distribution



- Power density is not uniformly distributed across the chip
- Silicon is not a good heat conductor
- Max junction temperature is determined by hot-spots
  - Impact on reliability and packaging, w.r.t. cooling

Historical Drivers of Low-Power Design

- Pocket calculators
- Hearing aids
- Implantable pacemakers and cardiac defibrilators
- Portable military equipment for individual soldiers
- Wristwatches
- Wireless computing

How have things changed?

Motivation for Low-Power Design Today

- Enabling higher performance & functionality via scaling
  - Higher functionality with smaller chips
  - Higher performance at lower cost
  - Portability
  - Can't arbitrarily shrink w/o accounting for heat density, power sources
- New portable compute-intensive applications
  - Video display and capture
  - Audio reproduction & capture
  - Drone navigation
  - Notebook computer
  - iPod, iPhone
  - Implantable medical electronics
- Need for satisfactory battery life span

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Sources of Power Dissipation

- Charging current (dynamic power)
  - Due to logic transitions causing logic gates to charge/discharge load capacitance
- Short-circuit current
  - Pull-up network and pull-down network momentarily shorted as logic gate changes state
- Leakage current (static power)
  - Diode leakages around transistors and n-wells
  - Increasing 20X for each new fabrication technology
  - Went from insignificant to a dominating factor

Stay tuned for more details…

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Design for Low-Power Techniques

This class will consider techniques at multiple levels…

- Reduced voltage
  - Lower V_{DD} → lower power (but at the cost of circuit speed)
  - Lower switching threshold, V_{th} → improves switching times to gain back performance loss
- Change your CMOS logic family
  - use a lower power one (static vs. dynamic logic)
- Transistor resizing
  - Optimize power-delay product of one gate driving another

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Design for Low-Power (cont.)

- Use parallelism and pipelining in system architecture
  - use more, but slower, hardware running at reduced V_{DD}
  - Increase throughput even though each circuit is slower
- Standby modes
  - clock disabling and power-down of selected logic blocks
- Structural transformations
  - Choose a logic implementation that reduced logical switching (e.g., ripple-carry adder vs. carry-look-ahead).
  - Use simplified logic that approximates exact computation.
- Software redesign to lower power dissipation
  - Alter memory access patterns and thus memory size requirements.
  - Simplify algorithm in software that provides an acceptable approximation

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SIA Roadmap for Processors (1999)

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Logic transistors/cm^2	6.2M	18M	39M	84M	180M	390M
Clock (GHz)	1.25	2.1	3.5	6.0	10.0	16.9
Chip size (mm^2)	340	430	520	620	750	900
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.5
High-perf. Power (W)	90	130	160	170	175	183

Source: http://www.semichips.org

Specific Topics in Low-Power

- Power dissipation in CMOS circuits
- Device technology
  - Low-power CMOS technologies
- Circuit and gate level methods
  - Logic synthesis
  - Dynamic power reduction techniques
  - Leakage power reduction
- System level methods
  - Microprocessors
  - Arithmetic circuits
  - Low power memory technology
- Power estimation

Low-Power Design

- One definition: Design practices that reduce power dissipation by at least by one order of magnitude.
- In practice 25-50% reduction is often acceptable.
- Low-power design methods:
  - Algorithms and architectures
  - High-level and software techniques
  - Gate and circuit-level methods

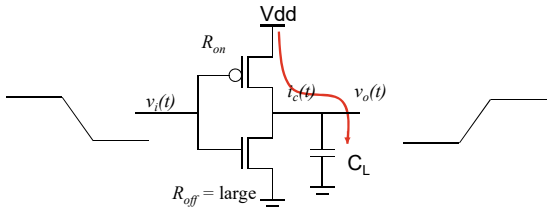
Which method will impact the power the most?

Components of Power

- Dynamic
  - Signal transitions
    - Logic activity
    - Glitches
  - Short-circuit
- Static
  - Leakage

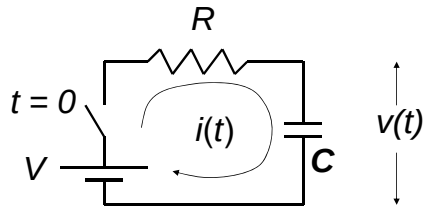
$$P_{total} = P_{dyn} + P_{stat}$$
$$= P_{tran} + P_{sc} + P_{stat}$$

Power of a Transition: P_{tran}



What goes into charging/discharging the capacitance C_L?

Charging of a Capacitor



Charge on capacitor, q(t) = *C v(t)*

Current, i(t) = *dq(t)/dt* = *C dv(t)/dt*

$$i(t) = C\frac{dv(t)}{dt} = \frac{[V - v(t)]}{R}$$

$$\frac{dv(t)}{dt} = \frac{V - v(t)}{RC}$$

$$\int \frac{dv(t)}{V - v(t)} = \int \frac{dt}{RC}$$

$$\ln[V - v(t)] = \frac{-t}{RC} + A$$

Initial condition, $t = 0$, $v(t) = 0 \rightarrow A = \ln V$

$$v(t) = V[1 - e^{\frac{-t}{RC}}]$$

$$v(t) = V[1 - e^{\frac{-t}{RC}}]$$

$$i(t) = C\frac{dv(t)}{dt} = \frac{V}{R}e^{\frac{-t}{RC}}$$

Total Energy Per Charging Transition from Power Supply

$$E_{trans} = \int_0^\infty Vi(t)dt = \int_0^\infty \frac{V^2}{R}e^{\left(\frac{-t}{RC}\right)}dt$$

$$E_{trans} = CV^2$$