ENGN2912E – Low Power VLSI System Design
Semester I, 2017
M, W 9:30am-10:50am

CLASS TIMES: MW 9:30 – 10:50 a.m. Barus & Holley 194 (studio lab)

INSTRUCTOR: R. Iris Bahar Barus & Holley 351
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Office Hours: F 9:00 – 11:00 a.m., or by appointment

COURSE WEBSITE: www.brown.edu/Departments/Engineering/Courses/engn2912E

COURSE DESCRIPTION: Up until the last few years, designers could rely on steady performance improvements in silicon-based electronic circuits, due largely to the continuous improvements in silicon fabrication technology. However, this improvement has slowed and even leveled off recently as power and thermal issues have come to dominate design constraints. To help overcome this slowdown in performance improvements, it is essential that designers integrate power- and thermal-aware techniques into every aspect of their designs. This course deals with the design of such digital systems. Issues that will be addressed include CMOS power dissipation, analysis and design tools used for lower power digital circuits, design methodologies for low power and thermal-aware CMOS circuits, low power architecture designs, and a discussion on future challenges in low power digital design. Class will include a mix of lectures and discussion on assigned readings of recent publications related to low-power design. Students will be responsible for leading and participating in these discussions. A course project will also be required.

Prerequisites: familiarity with basic digital circuit design structures and computer architecture principles; some circuit analysis helpful.

COURSE OUTCOMES: Students completing ENGN2912E should:

1. Understand sources of power dissipation in modern electronic circuits and be able to use a range of techniques to estimate power.
2. Understand how to apply techniques at the circuit-, logic-, architectural-, or algorithmic-level to reduce power dissipation in an electronic design.
3. Be able to critically read, analyze, and interpret the scientific literature in low power design of electronic circuits.
4. Be able to represent ideas clearly in written reports and oral presentations.

COURSE MATERIALS: **REQUIRED**: Reading materials will be made available from the course website throughout the semester.

RECOMMENDED: Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuit and Systems Perspective, 4th Edition,* Addison Wesley Publishers, 2011

RECOMMENDED: John Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach, 5th Edition,* Morgan Kaufmann Publishers, 2012

LECTURES: The first half of the course will be devoted to providing the class with a background in low power analysis and design. These will cover topics from circuit design, logic level implementation techniques, and architectural solutions.

DISCUSSION: The second half of the semester will consist of a discussion of various topics in low power system design. Each class will focus on one or two papers selected from recent publications. All students are expected to read the papers and prepare a short summary with 2-3 questions ***before class***. There will be one discussion leader and two scribes assigned for each class. The discussion leader is responsible for keeping the discussion going and/or preparing a formal presentation of the material. The scribes will jointly create notes summarizing key aspects of the papers and interesting discussions brought up during class. The scribe notes are due within a week of lecture and will be posted on the course webpage. It is expected that ***all*** students be involved in active discussion of the papers (not just scribes and/or discussion leaders).

HOMEWORK: There will be 3 homework assignments in the first half of the course intended to help reinforce understanding of various techniques used in low power digital system design.

PROJECT: The project will involve investigating some aspect of low power or thermal aware design in integrated circuits. Typically, a project will investigate one of the areas discussed during class; however, students are free to propose any appropriate research topic. I encourage choosing projects on topics related to students' own research focuses; however, the specific projects must be distinctly different from a previously established projects. Group projects (typically groups of two) are encouraged.

GRADING: Following is a tentative breakdown for the course grading:

Discussion Leadership	20%
Scribe Notes	15%
Class Participation	10%
Homework	25%
Final Project	30%

CODE OF ETHICS: It is expected that all work handed in for a grade will be of your own effort. For homework, it is fine to discuss with others general concepts regarding the assignments; however, all work is to be done individually. Finally, although the final project may be based on design concepts that have been previously developed, the actual implementation should be done from scratch by you and the rest of your team.

TIME COMMITMENT: Total time expected for this course is ~184 hours. This estimate is based on the following breakdown for work:

Weekly class meetings: 3hrs. X 14 weeks = 42 hrs.
Readings: 6hrs. X 7 weeks = 42 hrs.
Homework Assignments: 10hr. X 3 assignments = 30 hrs.
Presentation preparation: 10hrs. X 1 assignment = 10 hrs.
Scribe Notes preparation: 5hrs. X 2 assignments = 10 hrs.
Final Project research: 20 hrs.
Final project implementation: 30 hrs.
Total hours: 184 hours

Tentative Schedule for Lectures

Week	*Topic*
1: Sept. 6	Introduction, sources of power dissipation in CMOS circuits
2: Sept. 11, 13	Logic level power estimation and optimization
3: Sept. 18, 20	Threshold voltage and multi-threshold CMOS design
4: Sept. 25, 27	Low power memory design
5: Oct. 2, 4	Low power architectural techniques for the single processor
6: Oct. 9, 11	Low power multiprocessor techniques
7: Oct. 19, 20 (note makeup dates)	Low power through approximation techniques (in HW and SW)
8-14: Oct. 23-Dec. 11	Student-led class discussions on current research papers in low power design
15: Tuesday, Dec. 19, 9am-noon	**Final Project Presentations**