Cascaded resonant tunneling diode quantizer for analog-to-digital flash conversion

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(Received 5 December 2000; accepted for publication 8 April 2001)

We propose and model an application of cascaded resonant tunneling diodes to flash analog-to-digital conversion. We connect diodes of linearly increasing area in series, with separate contacts to interconnecting doped layers between the diodes. When a voltage is applied to the structure, the linearly changing diode size determines which of the diodes switch to the valley current, while the interconnecting contacts allow for a differential voltage measurement that accomplishes the signal quantization. The resulting flash quantizer has an estimated frequency operating limit in the gigahertz range. © *2001 American Institute of Physics.*
[DOI: 10.1063/1.1377622]

The advantages of digital signal processing are considerable noise reduction as well as data compression for reduced transmission bandwidth requirements. The increasing trend towards the use of digital logic for signal processing has resulted in increased need for high-speed analog-to-digital converters (ADC). They find application in video processing, radar signal processing, and high-speed data communications.

It has been long known that the fastest way to implement an ADC is with an assembly of comparators, one per quantization threshold, whose results are combined to yield the desired digital word.[1] The flash (parallel) ADC has a more complex structure, in which 2^N-1 comparators are used to convert an analog signal to N bits of binary information.[2] An alternative to the parallel flash technique has been the proposal to use a folding or sawtooth current–voltage ($I-V$) characteristic to achieve high speed.[3] This approach requires a high circuit complexity if one uses standard transistor-based devices. However, with resonant tunneling diodes (RTDs) available to the circuit designer, more compact and faster comparators can be made. Kuo *et al.*[4] have proposed to use a series of RTDs in a vertically integrated heterostructure to achieve the required multiple folding characteristic in a single device. With such a multipeak RTD characteristic, a multithreshold digitizer can be formed, further reducing the circuit complexity.[5] Recently, using the combination of individual RTDs and heterostructure field-effect transistors, a monolithic flash ADC integrated circuit has been reported.[6] In that circuit, the RTDs are used as current comparators, with the nonlinear RTD behavior making the comparator self-latching, obviating the need for circuit-level regenerative feedback.

Here, we suggest an alternative approach in which the multipeak $I-V$ characteristic of series-connected RTDs of linearly increasing area is used as a flash quantizer, which is a basic element of any ADC. Unlike the previous publications on RTD-based ADC devices, our proposed device takes advantage of the order in which the diodes switch. The latter is achieved by linearly increasing the area of our series-connected RTDs. The design presented in the letter aims at significant reduction of the number of elements in the flash ADC.

The simplest, albeit not the most technologically efficient, vertically integrated RTD we propose is schematically shown in Fig. 1(a). It consists of $N=7$ double-barrier RTDs decoupled with highly doped connecting layers. These layers are assumed to be relatively thick (~50–100 nm) to render the transfer of electrons across different RTDs an uncorrelated process and also to allow for a low-access-resistance output terminal in between the RTDs. The main characteris-

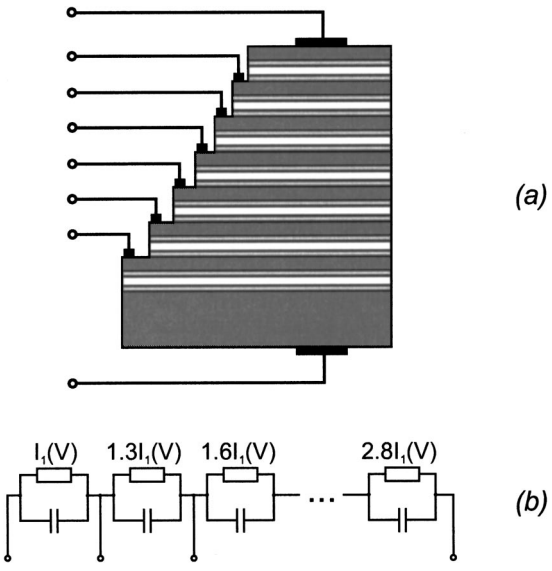

FIG. 1. Schematic cross section (a) and equivalent circuit (b) representing the vertically integrated RTD cascade where the RTD area changes linearly from stage to stage. Each RTD is represented by a parallel combination of a (nonlinear) resistance element and a capacitor, the small series resistance due to the doped layers in between the RTDs is ignored.

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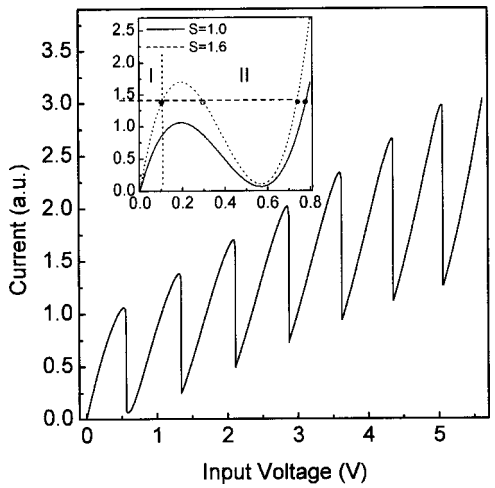

FIG. 2. Simulated current–voltage characteristic of the vertically integrated $N=7$ RTD cascade with linearly changing RTD area. Inset shows the $I-V$ characteristics of individual RTDs, where S is the RTD area. Operating regions I and II correspond to source–drain voltages below and above V_p. Intersections with $I=$const correspond to possible voltage drops across a RTD for a given current: stable RTD biasing configurations are marked by solid circles, the open circle is unstable.

tic feature of the device is that the size of the active area for each RTD in the series increases linearly, leading to the simple equivalent circuit shown in Fig. 1(b). Clearly, the same effective device structure could be accomplished from a smaller number of double-barrier active regions (or, indeed, from a single double-barrier heterostructure) by fabricating adjacent diodes of varying size side by side—the device designer would be free to decide on the resulting trade off between the device footprint and the number of epitaxial layers as well as mask levels. The extension to a larger number of diodes N for additional quantization bits is obvious.

Now let us consider the operation of our device. We will assume that our individual double-barrier RTD structure provides a $I-V$ characteristic with a current peak at a source–drain bias $V_p=0.2\,\mathrm{V}$, a peak-to-valley ratio (PVR) of 10, and a smooth transition through the valley current region, shown in the inset of Fig. 2. The PVR is comparable to the best room-temperature RTD results obtained in n-InGaAs/InAlAs material,[7] but our device could be operated at the lower PVR as well. Clearly, increasing the RTD area simply changes the peak current I_p proportionally. We can divide the voltage axis into two regions, $V<V_p$ (region I) and $V>V_p$ (region II), as shown in the inset of Fig. 2.

Now, consider the $I-V$ characteristic of N diodes of linearly increasing area connected in series. The operation of the device can be easily understood if one superimposes a line of constant current on the $I-V$ characteristics of different RTDs. The intersections show possible voltage drops across each individual RTD for a given current I. As the input voltage V_{in} is increased from zero, all the RTDs are initially in region I of their $I-V$ curves. When the current level reaches the I_p of the smallest RTD, this RTD switches into region II, momentarily causing the current to drop and then reaching the stable point with a large voltage drop, as shown in the inset of Fig. 2. The same process then repeats itself with the next smallest RTD, and so on. The physical picture is not at all different from a cascaded RTD structure with N identical diodes in series proposed for multivalued memory by Seabaugh, Kao, and Yuan.[8] What makes our proposed device efficient for flash quantization is precisely the predictable sequence of RTD switching that arises because of the linearly changing size illustrated in Fig. 1. It should be noted that in ideal case when the cascade structure consists of the identical RTDs the switching of the diode is also predictable, since it is governed by the self-consistent dynamical space-charge buildup due to tunneling carriers.[9] The electric field is higher at the anode, so the last RTD is the first to switch, and the high-field domain propagates sequentially towards the cathode (the same effect governs the switching in superlattices).[10,11] However, in real life there is always some dispersion in the epitaxial and geometrical parameters of the nominally identical RTDs, leading to unpredictable switching order determined by the scatter in the I_p of individual diodes.[12] The central idea of our device is to control diode switching by progressively changing the RTD area, as illustrated in Fig. 1. While no experimental data have been reported on the switching of cascaded RTDs of intentionally varied size, the dependence of the switching order on device area is clear cut and has been invoked to explain the switching of series-connected RTDs that were nominally of the same size (see Refs. 10–12).

The simplest way to model the $I-V$ characteristics of the vertically integrated RTD is by means of an equivalent circuit, shown Fig. 1(b). The circuit includes a series of $N=7$ subcircuits, each consisting of a nonlinear resistor and a capacitor in parallel (the small series resistance of the doped layers between the RTDs is ignored). Such a representation has been already used in the past for description of current instabilities and the formation of a high-field domain in superlattices.[13] The dynamics of the circuit is described by the following system of equations:

$$C_i\frac{dV_i}{dt}+J_i(V_i)=I,\quad i=1,2,\ldots,7,\quad \sum_{i=1}^{7}V_i=V_{\mathrm{in}},$$

where V_i is the voltage drop across the ith diode; V_{in} is the input voltage; $J_i(V_i)$ is the $I-V$ response of the ith diode; I is the current passing through the device; and C_i is the capacitance of the ith diode. We take the curves presented in the inset of Fig. 2 as $J_i(V_i)$ inputs to our model (our results do not depend qualitatively on the exact shape of the $I-V$ curves). Figure 2 shows the simulated $I-V$ characteristics of the vertically integrated RTD we propose. There are, indeed, seven regularly spaced current peaks. The peak amplitude successively increases, reflecting the order in which the diodes switch. Thus, by proper sizing of the area it becomes possible to define the sequence for the independent RTDs to enter the negative differential resistance region at a given input voltage V_{in}. The device designer is free to set the smallest diode area to provide with the required current drive. Below we will show that a RTD cascade with area ratios varying as 1:1.3:1.6:...:2.8 and the smallest diode area $S_1=1\ \mu\mathrm{m}^2$ can yield device operation in GHz range.

To achieve the quantizer function, we simply need to take the differential voltage measurements across all the RTDs at the output terminals, as shown in Fig. 1(b). In this case, the transfer curves for all the seven digital outputs are demonstrated in Fig. 3. For a given input V_{in} the differential voltage exists in two possible states: if a given RTD has

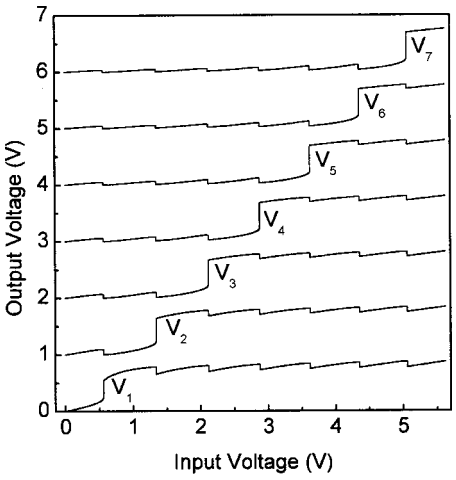

FIG. 3. Simulated transfer curves of the quantizer based on the vertically integrated RTD. The curves are shifted for clarity. The voltage ripple observed arises from the transient total current switching when one of the other RTDs switches from region I to region II.

switched, the voltage across it is high ($\sim$0.75 V, given our $I-V$ RTD characteristic); if it has not, the voltage is low ($<V_p\sim 0.2$ V). The transition from low to high is steep and the separation between the two voltage regimes is evident. The ripple observed on each differential voltage transfer curve arises from the transient total current switching when one of the other RTDs switches between regions I and II. The available noise margin depends on the PVR of the RTD $I-V$ curve, as can be seen from Fig. 3.

It is worth noting that the $I-V$ curve of Fig. 2 and the resulting quantizer operation of Fig. 3 correspond to an input voltage V_{in} swept up from zero. If V_{in} is swept down from a high value, the current peak positions would shift due to the series resistance arising from the nonswitching RTDs in the cascade. This would not impact the quantizer performance, however, because the usual ADC architecture includes a sample-and-hold circuit and a buffer amplifier to isolate the input signal and furnish a suitable output impedance to drive the RTD quantizer.[4–6] After each quantization, V_{in} is returned to zero for the duration of time necessary to bring the quantizer into its zero state.

According to the above, our device outputs an eight-level (7-bit) thermometer code, demonstrating thereby the ability of the vertical-integrated RTD proposed to function as a quantizer. One can see that to achieve N-bit resolution for thermometer code, N RTDs should be integrated in one structure. Clearly, in order to have a binary coded word an additional encoding scheme is required. Still, by using the flash quantizer of Figs. 1–3, ADC circuit complexity could be much reduced compared to that of the RTD-based flash ADC proposed so far.[6]

Finally, we would like to discuss the operating speed of our device. As usual, the frequency limit of the proposed quantizer is determined by the capacitance of the switching RTD combined with the series resistance arising from all the other RTDs in the structure. A simple estimate for this process can be derived by considering a *RC* delay for charging a capacitor of one RTD, as originally proposed by Luryi.[14] In arriving at the series resistance due to the nonswitching RTDs, let us assume that, on average, half are in region I of their $I-V$ curve and the others are in region II.[15] The other necessary ingredient is the peak current density J_p, for which we shall use 10^5 A/cm^2 in accordance with the n-InGaAs/InAlAs RTD results by Brown *et al.*[7] This corresponding resistance per unit area for the two possible diode states is around 2.0 and 7.5 $\mu\Omega\,\text{cm}^2$, respectively. If we assume that the double-barrier heterostructure between the highly-doped cladding layers is $\sim$15 nm thick, the resulting capacitance per unit area is about 0.8 μF/cm^2. Taking the area of the smallest RTD to have an area of 1 μm^2, we obtain a *RC* delay time τ to be of 40 ps, leading to a cutoff frequency $f_{\max}=1/(2\pi\tau)$ of about 3.5 GHz. Taking into account the access resistance of the output terminal [where the current flows horizontally through the $\sim$50–100 nm doped layer, similarly to the base contact of a bipolar transistor, see Fig. 1(b)] would reduce $f_{\max}$ somewhat. Heavy doping of the interconnecting layer can reduce the per-square resistivity below 1 kΩ, which is smaller than the total resistance of the cascaded RTDs. As a result, our quantizer can be expected to operate at gigahertz frequencies.

In conclusion, our letter describes a simple concept for analog-to-digital flash conversion performed by a series connection of RTDs with linearly increasing area. Unlike proposed devices utilizing nominally identical RTDs,[8] our structure results in a predictable sequence of RTD switching. Differential voltage measurements between the output electrodes at the source and drain of each RTD produce high- and low-voltage values corresponding to digital zero and one states. The resulting flash quantizer is predicted to operate at gigahertz speeds at room temperature. Our concept could reduce the circuit complexity for flash ADC.

The authors acknowledge useful discussions with Professor S. Luryi and Dr. A. L. Danilyuk. This work has been supported by the French Ministry of Foreign Affaires (A.K.) and the National Science Foundation Career Award program, Grant No. DMR-9702725 (A.Z.).

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