A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration

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Abstract—We demonstrate experimentally a capacitor-less one-transistor dynamic random access memory (DRAM) based on fully depleted silicon-on-insulator substrate. In our device, the charges are directly stored in front gate capacitor \((C_G)\) and read out through a fast feedback regeneration process. The simulated read/write times of our device reach below 1 ns, much faster than conventional 1T-1C DRAM. The read/write biasing voltages can be scaled down to 1.1 V, achieving long retention time \((t_{re}>5\ s)\).

Index Terms—Capacitor-less, dynamic random access memory (DRAM), feedback, high speed.

I. INTRODUCTION

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he capacitor-based 1T-1C dynamic random access memory (DRAM) has been the prevalent dynamic memory device in recent decades, exhibiting high integration density and good reliability, but suffering from low access speed [1]. The conventional 6-T static random access memory, on the other hand, provides high access speed but low density [2]. Memory devices that can provide both high integration density and high speed are thus of great interest, and several devices have been proposed during the past decade [3]. One example is the thyristor-based RAM (T-RAM) [4]–[6], which is compact and fast, but requires accurate control of the bipolar transistors and precise doping control to achieve stable characteristics [5]. Another example is the field effect diode (FED) with two front gates, which has shown sharp switching and hysteresis properties [7]–[9]. This FED, based on field effect-controlled barrier modulation, was originally proposed for electron static discharge protection [7] and then as a memory device with good simulated scaling capability [9].

In this letter, we demonstrate experimentally the use of a simplified field effect-controlled device (Z\(^2\)-FET, for zero-slope, zero-impact ionization FET [10]) as a fast, compact, and refreshable memory. Our fully depleted silicon-on-insulator (FD-SOI) device has only one front gate \((V_G)\) which together with the backgate bias \((V_{BG})\) forms two adjacent carrier injection barriers. The device also works with fixed oxide charge \((Q_S)\), similar to feedback FET (FB-FET) [11], [12]. The Z\(^2\)-FET shows sharp switching and \(V_G\)-controlled hysteresis [10] and has fast DRAM functionality without any external capacitor.

II. DEVICE STRUCTURE AND DC CHARACTERISTICS

Our device is a lateral \(pin\) diode in the FD-SOI channel, where the intrinsic channel is partially covered by the front gate \((L_G)\) and partially uncovered \((L_{IN})\) as in an asymmetric tunneling TFET [13]. The device operates with either backgate \((V_{BG})\) or fixed oxide charge \(Q_S\) in the CVD-deposited SiO\(_2\) in the \(L_{IN}\) region only (the SiO\(_2\) gate insulator under \(L_G\) is thermally grown and contains negligible trapped charge). When the \(pin\) source-drain diode is forward biased, as shown in Fig. 1(a), the drain current initially remains low because of the injection barriers to electrons (due to front gate \(V_G<0\) and holes (due to \(V_{BG}>0\) or positive \(Q_S\) on the intrinsic region \(L_{IN}\)). As \(|V_D|\) is increased, the drain current \(I_D\) increases sharply at a point \(V_{ON}\) determined by \(V_G\), as shown in Fig. 1(b), and the \(I_D-V_D\) curve exhibits pronounced hysteresis when \(|V_D|\) is swept back to zero. Note that our device is fabricated in a standard FD-SOI process with metal gate and raised source/drain technology [13].

The surface potential [see Fig. 1(c)] shows the electron and hole injection barriers formed by \(V_G\) and \(V_{BG}\) (or \(Q_S\)) under low \(|V_D|\), respectively. As \(|V_D|\) increases close to \(|V_G|\), the channel under the gate is depleted and the electron injection barrier is lowered. This causes electron injection from \(n^+\)-doped drain into the channel; the electrons flow to the \(p^+\)-doped source and induce a potential change at the source junction, thereby reducing the hole injection barrier. As the \(V_D\) reaches \(V_{ON}\), the hole barrier is sufficiently reduced to permit hole flow from source to drain, causing positive feedback [7], [10], [11] that turns on the device and eliminates the injection barriers, see the simulated surface potential at \(V_D=-2\ V\) in Fig. 1(c). Since the process does not involve impact ionization [10] or bipolar transistor action and the carrier injection is controlled by the field effect-induced barrier, the device characteristics are relatively insensitive to the temperature. Fig. 1(d) shows the simulated relation between \(V_{ON}\) and the amount of \(Q_S\), revealing that \(V_{ON}\) is only sensitive to the \(Q_S\) over a small range of densities. With enough surface charge, \(V_{ON}\) saturates and becomes independent of \(Q_S\); so precise control over \(Q_S\) is not required. A value of \(Q_S \sim 10^{12} \text{ cm}^{-2}\) is enough for our devices with \(L_{IN} \geq 200\ \text{nm}\). For devices with shorter \(L_{IN}\), higher surface charge density is needed [see Fig. 1(d)]. This can
The device returns to the hold state (to charge the spacer, as in the FB-FET [11]). Leakage current in the reverse-biased drain junction that limits the retention time be achieved by tuning the CVD process or using high voltage to charge the spacer, as in the FB-FET [11].

III. Capacitor-Less DRAM Operation

The logic states of the device are represented by the mobile charge stored on the front gate capacitor \( C_G \) formed by the gate oxide, with logic “1” corresponding to high charge storage, as shown in Fig. 2. The hold state corresponds to \( V_G = -1.7 \text{ V} \) and \( V_D = 0 \). The logic state readout uses a \( V_D \) pulse with short fall/rise time (15 ns in the experiment, limited by our equipment): for logic “1,” the negative \( V_D \) pulse discharges the holes stored on \( C_G \) and generates a transient drain current \( I_D \) high enough to initiate the feedback process and turn on the device. When the device returns to the hold state \( (V_G = -1.7 \text{ V}) \), the holes available in the body recharge the capacitor, enabling intrinsic charge regeneration. Logic “0” corresponds to no charge on \( C_G \) and hence no response to the \( V_D \) pulse (the device remains turned off).

The write procedures for logic “0” and “1” are illustrated by the equivalent circuit in Fig. 2. Since the body-source junction is reverse biased, blocking the flow of transient current, only drain and gate need be considered. The writing of logic “0” is shown in Fig. 2(a), where \( V_G \) is pulsed from \(-1.7 \text{ V} \) to 0, while \( V_D = 0 \). This discharges the \( C_G \) through the forward-biased drain diode, overwriting the former “1” state. As \( V_G \) decreases back to \(-1.7 \text{ V} \) in the hold state, \( C_G \) is basically not recharged; parasitic recharging occurs via the small leakage current in the reverse-biased drain junction, giving logic “0” a finite but long retention time \( t_{re} \).

Conversely, to write logic “1” from logic “0,” \( V_G \) is pulsed from \(-1.7 \text{ V} \) to 0 and \( V_D \) is simultaneously pulsed from 0 to \(-1.3 \text{ V} \), shown in Fig. 2(b). This turns on the device, corresponding to the \( |V_D| > |V_G| \) situation in Fig. 1(b): the current goes high, and electrons and holes are injected into the channel. As the device switches back to the hold state, \( V_G = -1.7 \text{ V} \) and \( V_D = 0 \), holes are stored on \( C_G \). This represents the equilibrium configuration, so logic “1” has an infinite retention time \( t_{re} \) and requires no refreshing.

This DRAM functionality is demonstrated experimentally in Fig. 3. Fig. 3(a) shows the writing of logic “0” by pulsing \( V_G \) from \(-1.7 \text{ V} \) to 0 and then returning to the hold state. Subsequently, using the \( V_D \) readout pulse, the correct “0” value is read out after a delay \( t_0 = 1 \text{ s} \), but not after 1.5 s. Fig. 3(b) shows the writing of logic “1,” as well as the correct readout after both \( t_0 = 1 \text{ s} \) and 10 s (as explained earlier, logic “1” has an infinite \( t_{re} \)).

The retention \( t_{re} \) of logic “0” is determined by the leakage in the reverse-biased drain junction and thus strongly affected by the bias. With the writing and reading waveforms as in Fig. 3, the experimentally measured \( t_{re} \) decreases as \( |V_G| \) in the holding stage and \( |V_D| \) in the reading stage increase—see Fig. 4(a). Experimentally, our DRAM prototype works down to \( |V_D| = |V_G| = 1.1 \text{ V} \), which is competitive with conventional 1T-1C DRAM and lower than floating-body DRAMs. This is helpful for prolonging \( t_{re} \).

IV. Modeling and Reliability

Fig. 4(b) shows the TCAD simulation in Atlas [14], reproducing the operating procedure in Fig. 3. In simulation, the read/write times reach below 1 ns, easily outperforming conventional DRAM. In a conventional 1T-1C DRAM, the capacitance needs to be large to store enough charge to reliably distinguish logic “1” and “0” states. This increases read/write time and dynamic power consumption. In our \( Z^2 \)-FET DRAM, only a few charges need to be stored on \( C_G \). Instead of directly reading out the stored charge, as in a 1T-1C DRAM, in our device the charged charge seeds the positive feedback that is activated with the fast reading pulse. Additional simulations (not shown) demonstrate that both \( L_G \) and \( L_{IN} \) are scalable below 40 nm.

Preliminary reliability tests performed on our capacitorless DRAM show no significant degradation after \( 6 \times 10^{10} \) cycles. Also, as mentioned previously, the device characteristics are relatively insensitive to temperature \( T \): increasing \( T \) by \( 80 \degree C \) decreases the \( |V_{ON}| \) for \( V_G = -2 \text{ V} \) in Fig. 1(b) by only \( \sim 0.12 \text{ V} \).

Our device exhibits similar performance with \( V_{BG} \sim 2 \text{ V} \) or with surface charge [10]. The use of \( V_{BG} \) instead of \( Q_S \)
may be advantageous in terms of process control and variability issues. Finally, the voltage waveforms, shown in Fig. 3 for a single memory device, can be easily adapted for array application [15].

V. CONCLUSION

We have presented a compact, capacitor-less DRAM device in FD-SOI utilizing the field effect-controlled barrier modulation and charge regeneration mechanism. The read and write procedures use fast $V_C$ and $V_D$ pulses for manipulating the charges stored on the front gate capacitor. Experimentally, the gate and drain biasing can be scaled down to 1.1 V, lower than charges stored on the front gate capacitor. Experimentally, the Z$^2$-FET device has the advantages of compact, single front gate footprint, undoped channel, and no impact ionization or bipolar action.

REFERENCES


Fig. 3. Experimental results show the DRAM operation waveforms. (a) The logic “0” is written by $V_C$ pulse and read out correctly by $V_D$ pulse after a delay of $t_0 = 1$ s, but not after $t_0 = 1.5$ s, due to limited retention time $t_{ret}$. (b) The logic “1” is written by simultaneous $V_C$ and $V_D$ pulses and read out correctly by $V_D$ pulse after $t_0 = 1$ and 10 s ($t_{ret}$ is unlimited in logic “1”).

Fig. 4. (a) Experimental logic “0” retention time $t_{ret}$ versus $V_C$ bias under different $V_D$ reading pulses at room temperature. The longest $t_{ret}$ is over 5 s, achieved under the lowest bias $V_C = V_D = -1.1$ V. (b) The TCAD simulation shows that the read/write time can reach below 1 ns.