A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection

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Abstract

We experimentally demonstrate a field-effect transistor with a single front gate built on fully-depleted silicon-on-insulator substrate that possesses extremely steep switching slope (<1 mV/decade) and gate-controllable hysteresis. The mechanism for the sharp switching, confirmed by simulations, involves the positive feedback between the gate-modulated charge injection barriers and the electron and hole components of the source-drain current. The transistor is named Z²-FET as it features zero impact ionization (unlike thyristors) and zero subthreshold swing.

Keywords:
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Positive feedback

Solid-state switching devices are of great interest to overcome the switching limitations of standard MOSFETS and achieve low subthreshold swing (SS). A number of such devices achieve sharp switching through the use of positive feedback. The thyristor uses two parasitic bipolar transistors triggered by impact ionization and is widely used in power electronics due to its sharp switching and high current drive [1]. A variant known as the thin capacitively-coupled thyristor (TCCT) has been built in fully-depleted silicon-on-insulator (FD-SOI) substrates and successfully demonstrated for SRAM and DRAM memories [2–4], but requires precise doping engineering to obtain reliable performance [5]. The field effect diode (FED) with two front gates, showing sharp switching and hysteresis, was originally used for electrostatic discharge (ESD) protection and then proposed for memory applications [6–8]. Recently, the feedback field effect transistor (FB-FET) has been shown to possess a small subthreshold slope (SS) and high hysteresis [6]. The operation of the FB-FET involves the interaction between the electron and hole source-drain currents and the injection barriers arising from surface charges trapped in the gate spacers.

In this letter, we present a simple device that uses positive feedback similar to the FED and FB-FET except that no trapped surface charge or the fabrication of adjacent gates is required. The gate voltage is directly controlled by the front gate (V_G), whereas the other barrier is controlled by the back gate (V_BG). The device exhibits sharp switching at low 1–2 V operating voltages (Fig. 1b), as well as a large controllable hysteresis in the drain current–voltage (I_D–V_D) domain (Fig. 1c), where the turn-on voltage (V_ON) varies linearly with V_G. Our simulations confirm the gate control of electron and hole injection barriers (V_n and V_p) and show excellent agreement with the experimentally measured V_ON and I_D–V_D hysteresis values. They also confirm that while both electron and hole current flows are essential to the operation of our bipolar device, neither impact ionization nor channel doping is involved; front and back gate control alleviates the control of the surface charge or the fabrication of adjacent gates.

The schematic view of the Z²-FET is presented in Fig. 1a. The fabrication process is described in detail elsewhere [9], here it suffices to mention that the device is built in FD-SOI with a 20 nm thick Si active layer and 140 nm buried oxide (BOX). The channel is undoped and partially covered by the gate in the region denoted by L_D = 400 nm, with a remaining ungated region L_W = 500 nm between the gate and the source. The gate oxide is 3 nm HfO2 deposited by atomic layer deposition (ALD). As in the TFET, the source and drain (S/D) have different dopants, but the resulting p–i–n junction is forward-biased rather than reverse-biased. For the measurement of transfer characteristics, V_G is swept from negative to positive and V_BG is kept at 2 V, see the n-type device in Fig. 1b. The electron and hole barriers are created by the front and back gates without the need for channel doping or surface charges.
The transfer $I_D$-$V_G$ characteristics of the $Z^2$-FET in Fig. 1b are extremely abrupt: $I_D$ or $I_S$ increase by eight decades within $\Delta V_G = 1 \text{ mV}$, i.e. zero swing. The switching point is determined by the biased terminal (source or drain, defining whether the injection barriers for hole or electron is modified first) and corresponding voltage. This flexibility is very attractive for adjusting the switching voltage in practical CMOS circuits, which combine n-type and p-type devices (complementary p-type $Z^2$-FETs have also been demonstrated [12]).

Fig. 1c shows the $I_D$-$V_B$ characteristics, with the source grounded and $V_D$ swept from zero to negative values and then back to zero, for several values of $V_G$. When $|V_G| > 0.5 \text{ V}$, the device remains in the $I_{OFF}$ state as $|V_D|$ is increased from zero until $I_{ON}$ is reached, at which point the current increases sharply to $I_{ON}$ that corresponds to a forward-biased diode with a high current drive. The $I_{ON}/I_{OFF}$ ratio is as high as $10^8$ in a narrow range of $\Delta V_D < 20 \text{ mV}$, see Fig. 1c. As $|V_D|$ is swept back down to zero, the current remains high until $|V_{OFF}|$ is reached. The size of the hysteretic loop is controlled by $V_C$, since $|V_{ON}|$ increases approximately linearly with $|V_C|$. The mechanism of operation is understood via Silvaco TCAD simulations [13].

The corresponding simulation of $I_D$-$V_B$ is shown in Fig. 3 for $V_C = 0$, $-1$, $-1.5$, and $-2 \text{ V}$, in good agreement with the experimental results shown in Fig. 1c. The $I_D$ remains low until $V_{ON}$ is reached, at which point it jumps to the large $I_{ON}$ value, indicated by the dashed line (as usual, the negative resistance zone is not observed, leading a hysteretic $I_D$-$V_B$ characteristic). The added dots in the $V_C = -2 \text{ V}$ curve correspond to the same simulation with the impact ionization model turned on. As expected for our range of $V_C$ and $V_D$, impact ionization is not a factor in the device operation.

In detail, the working mechanism of our device can be explained by the evolution of $V_D$ and $V_B$ as $V_D$ decreases towards $V_{ON}$, see Fig. 4. At low $|V_D|$, the channel under the gate is strongly accumulated with holes due to $V_C = -2 \text{ V}$, forming a high $V_D$ barrier and thus blocking the electron injection. The channel potential under the gate ($\varphi_{GC}$) decreases with $V_D$, since the channel–drain junction is forward biased. As $V_D$ decreases below the clamping voltage ($V_C$), holes are depleted under the gate and the $\varphi_{GC}$ is clamped by the gate voltage, $\varphi_{GC} \sim V_C$, because the BOX is much thicker than the top oxide. Thereafter, the $V_D$ drops linearly with $V_D$, since $V_D = \varphi_{GC} - (V_B + V_{BD})$, where $V_{BD}$ is the channel-drain built-in potential. Accordingly, the electrons are injected into the channel and flow to the source. The electron current induces a potential of the device in Fig. 1a as a function of $V_D$ for fixed $V_C = -2 \text{ V}$ and $V_{BG} = 2 \text{ V}$. As $|V_D|$ is increased, the electron injection barrier $V_B$ is reduced, increasing injection, until at $V_D = V_{ON}$ $\sim 1.84 \text{ V}$, a sufficiently high electron current is injected to reduce $V_B$, thereby permitting hole injection and establishing the positive feedback, leading the device to switch sharply to the $I_{ON}$ state. This feedback markedly reduces the electron and hole barriers, as shown in Fig. 2 for $V_C = -2 \text{ V}$. As compared to FB-FET [9,10], the barriers in our device are determined by $V_C$ and $V_{BG}$, without recourse to surface charge storage in the gate spacers.

![Simulated band-diagram of the Z²-FET under constant Vg = -2 V](image)

Fig. 2. Simulated band-diagrams of the $Z^2$-FET under constant $V_G = -2 \text{ V}$ with $V_C = 0$, $-1.5 \text{ V}$ and $-2 \text{ V}$. The electron and hole injection barriers are indicated by the double arrows, which block the carriers flow at low $|V_D|$, and are eliminated at $V_D = -2 \text{ V}$ due to strong feedback.

![Experimental I_D-V_G transfer curves](image)

(a) Shows the schematic view of the n-type $Z^2$-FET. (b) Measured $I_D$-$V_G$ transfer curves (solid curves: grounded source; dashed curves: grounded drain; $V_{BG} = 2 \text{ V}$) showing $I_{ON}/I_{OFF} > 10^8$, $SS < 1 \text{ mV/dec}$ and $I_{ON} > 500 \mu A/\mu m$. (c) Experimental $I_D$-$V_B$ curves vs. $|V_D| = 0$ to $2 \text{ V}$ in 0.5 V steps, showing large $I_D$-$V_B$ hysteresis as $V_B$ is swept from zero through $V_{ON}$, where the current switches to a large $I_{ON}$. Device parameters are $L_G = 400 \text{ nm}$, $W_{IN} = 500 \text{ nm}$, $W = 10 \mu m$, with $V_{BG} = 2 \text{ V}$. The transfer $I_D$-$V_C$ characteristics of the $Z^2$-FET in Fig. 1b are extremely abrupt: $I_D$ or $I_S$ increase by eight decades within $\Delta V_C = 1 \text{ mV}$, i.e. zero swing. The switching point is determined by the biased terminal (source or drain, defining whether the injection barriers for hole or electron is modified first) and corresponding voltage. This flexibility is very attractive for adjusting the switching voltage in practical CMOS circuits, which combine n-type and p-type devices (complementary p-type $Z^2$-FETs have also been demonstrated [12]).

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drop at the source junction and thus lowers the $V_D$. As $V_D$ approaches $V_{ON}$, the $V_D$ shrinks, enabling the injection of holes, which flow to the drain and lower $V_D$. The resulting positive feedback toggles the device to the ON state with high $I_D$.

The active silicon layer needs to be thin enough for the gate-controlled injection barriers to block the carrier flow throughout the Si substrates with thin silicon and BOX is scalable down to $L_{IN} = 30$ nm without degrading significantly the $I_{ON}$. Also, in a $Z^2$-FET with ultra-thin BOX ($\sim 10$ nm), a heavily-doped ground plane with appropriate polarity, currently used in advanced MOS-FETs [14], can induce enough potential in the undoped channel to form the injection barrier even without $V_{BG}$ [12]. Finally, our device can also function using surface charge ($Q_S$) in the $L_{ON}$ region instead of $V_{BG}$ to form one of the barriers [15], similar to FB-FET [9,10].

In conclusion, we have presented a device possessing gate-controllable hysteresis and a sharp switching property. The structure of the $Z^2$-FET is similar to asymmetrical TFET with the fabrication process fully compatible with the complementary MOS technology on FD-SOI. From simulations, the operating principle of the $Z^2$-FET is confirmed to involve positive feedback which is triggered by gate-controlled carrier injection. The $Z^2$-FET has the advantages of compact, single front gate footprint, undoped channel, no surface charges, no impact ionization and CMOS process compatibility. Thanks to its large hysteresis, where $V_{ON}$ is almost linearly dependent on $V_C$, steep slope and scalability, the $Z^2$-FET can find applications as a sharp current switch, electrostatic discharge protection and memory device. We have recently demonstrated [12,15] that the hysteresis in Fig. 1c can be utilized to design fast and low-voltage capacitor-less, single-transistor dynamic memory (1T-DRAM).

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