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Sharp-Switching SOI Devices

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We will present and discuss two related classes of sharp-switching SOI devices: tunneling FETs (TFETs) and feedback transistors. The TFET is a reverse-biased *pin* gated diode: gate voltage V_G controls the electric field in the interband p^+/n^+ tunneling junction. In principle, the TFET current can be switched faster than the subthreshold current of a MOSFET. We will review technological solutions for improving the I_{ON} current and subthreshold swing. The recently proposed feedback transistor has a similar gated-diode configuration, but operated in forward bias. Electrostatic gate-controlled barriers prevent carrier injection into the channel until the gate bias reaches a turn-on value, at which point the device switches abruptly (< 1 mV/decade) to a high I_{ON} current. We will discuss the device physics, architecture, and outstanding performance of a double-gated variant we have named the Z^2-FET, with applications in CMOS-compatible memories, sensors, logic and protection circuits.

Introduction

The scaling of MOSFETs is limited by short-channel effects and unscalable subthreshold swing (*SS*). Sharp-switching devices are needed to overcome the CMOS limits in terms of scaling and power reduction. The *SS* is a key parameter that determines the off current (*i.e.,* leakage power) and operating voltage (*i.e.,* dynamic power). In a MOSFET in weak inversion, an increase of the inversion charge by one decade requires 60 mV variation of the surface potential. This implies at least 60 mV increase in the gate voltage, leading to a minimum *SS* = 60 mV/decade of current at room temperature. Only fully depleted (FD) transistors, such as planar FDSOI, FinFETs or nanowire FETs, can reach this minimum *SS*, which is still insufficient for scaling ultimate CMOS below 0.5 V operating voltage. The solution is to develop transistors based on different physical principles.

In this paper, we concentrate on tunneling FETs (TFETs) and feedback FETs, motivated by their performance, compatibility with standard silicon processing, and relatively low operating voltage. In Section 2, recent developments in SOI-based TFETs are reviewed. Section 3 is devoted to a more recent transistor, the Z^2-FET, which uses band modulation and positive feedback. This device exhibits extremely attractive characteristics (abrupt switching, high I_{ON}, low leakage, gate-controlled hysteresis, *etc*.), which make it suitable for a variety of applications including DRAM and SRAM memory, sensing, fast logic, and ESD protection.

TFETs

The TFET is composed of a reverse-biased *pin* diode ($V_D > 0$) and a control gate, see Fig. 1(a). The body is thin and undoped, hence the leakage current is very low. At $V_G = 0$, carriers cannot tunnel between the conduction and valence bands because the source and drain terminals are far apart, whereas band-to-band tunneling (BTBT) requires adjacent highly-doped n^+/p^+ regions with a large junction field. At sufficiently high $V_G > 0$, electrons are accumulated in channel and form a field-effect-induced n^+ region, creating a source-channel p^+/n^+ junction where BTBT occurs at the source corner of the gate, giving rise to a significant tunneling current I_{ON}. A *p*-type TFET has identical configuration with negative bias applied to the gate and the p^+ contact.

The BTBT current is not subject to the 60 mV/decade limit (1-4). The transfer characteristic of an *n*-type TFET is shown in Fig. 1(b), where the current ramps rapidly as V_G increases (3). There is a limited bias range where $SS < 60$ mV/dec for $V_D = 1$ V. In principle, since tunneling occurs in a narrow localized region, the TFET is more scalable and has better short-channel immunity than a MOSFET. Furthermore, TFETs are compatible with Si technology and well suited to thin-body SOI, where leakage currents are low. Several types of Si-based TFETs with (3,4) and without (2) an intrinsic channel have been demonstrated. A general problem is that the I_{ON} of Si-based TFETs is very low, typically 3–5 decades lower than in MOSFETs, and the abrupt *SS* is only obtained over small current range due to the low BTBT rate. Thus, Mayer *et al*. (4) have reported an SOI-based TFET with *SS* = 42 mV/decade over 2 decades of current but $I_{ON} < 1$ μA/μm.

Another issue in symmetric TFETs as in Fig. 1(a) is that characteristics are nearly symmetric for positive and negative gate bias. Although the I_{OFF} current (at $V_G = 0$) is low, the leakage current at $V_G < 0$ may become unacceptably high as holes accumulate in the body and a tunneling occurs at the drain-channel junction. The problem can be solved with asymmetrical architectures: unequal source/drain doping, lateral heterojunctions or asymmetric strain (5–10). The simplest solution consists in an intrinsic region L_{IN} (gate underlap) as shown in Fig. 2(a) (9). Under $V_G > 0$ (I_{ON} state), the tunneling occurs at source side. The maximum field hardly depends on L_{IN}, where the potential drop is negligible, so the current remains high – see Fig. 2(b). In contrast, for negative gate bias (I_{OFF} state), tunneling occurs at the drain side. As L_{IN} increases beyond 20 nm, the junction electric field and BTBT tunneling rate fall rapidly. For $L_{IN} = 50$ nm, the ambipolar tunneling is turned off, completely suppressing the leakage current.

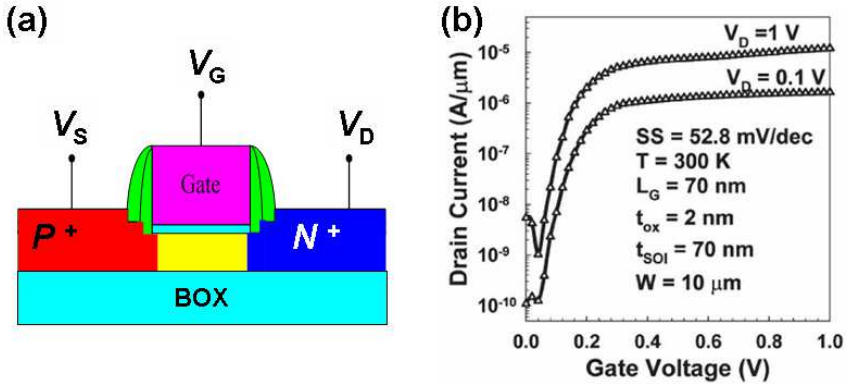

Figure 1. (a) Configuration of *n*-type TFET on SOI and (b) typical transfer characteristics reported by Choi *et al.* (3).

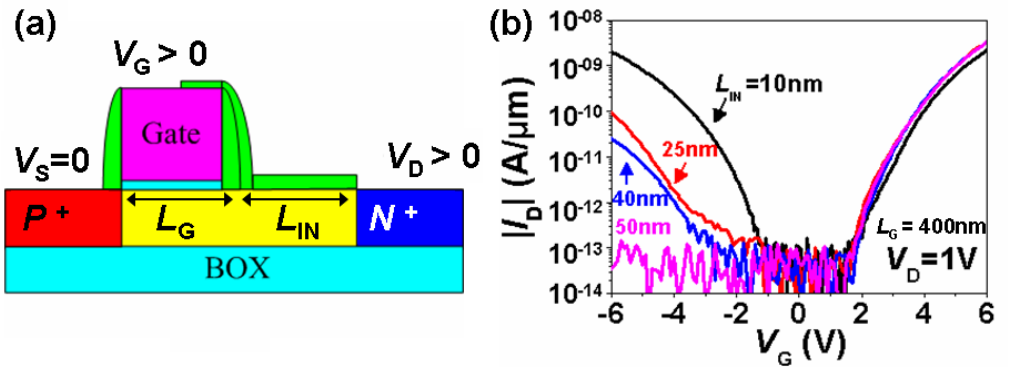

Figure 2. (a) Asymmetric *n*-type TFET on SOI with undoped L_{IN} spacer on the drain side and (b) transfer characteristics showing the suppression of the leakage current by L_{IN} (9).

The I_{ON} current can be increased by enlarging the area of the tunneling junction. An interesting idea is to expand simultaneously the p^+ and n^+ regions into the body of the TFET in Fig. 1(a), with a positive gate bias inducing a surface electron channel and a negative back-gate bias bringing holes into the back channel. Interband tunneling is expected to occur in the vertical p^+/n^+ virtual junction, which covers the whole body area instead of the narrow region at the source (11). However, BTBT requires the field-induced p^+/n^+ layers very close to each other, meaning an ultrathin film. Unfortunately, our experiments show that this attractive concept does not work. Sub-10-nm thick films cannot accommodate electron and hole channels facing each other. According to the super-coupling effect, an ultrathin transistor with reasonable front/back gate biasing tends to contain only one type of carriers (12).

The tunneling rate increases exponentially by reducing the semiconductor bandgap and increasing the junction field (13,1). The implementation of high-κ dielectric oxide reduces the effective oxide thickness, which translates in stronger effective field at the tunneling junction. SOI TFETs with similar architectures, featuring either SiO_2 or HfO_2 gate dielectrics, have been fabricated and compared, with the latter exhibiting much higher I_{ON}, as well as reduced *SS* (9).

Bandgap engineering is another avenue for improving TFET performance. Germanium-based materials are fully compatible with SOI technology. The Ge content can be locally enriched in SGOI devices by the condensation technique, producing pure GeOI islands. Various reports indicate an increase in the tunneling rate and I_{ON} current, including both planar GeOI TFETs (6,14) and Ge-containing nanowires (10,15,16).

Record I_{ON} performance was recently achieved with a TFET combining advanced technology steps: high-κ dielectric, metal gate and raised SiGe source and drain terminals. Since tunneling is enhanced in ultrathin body, the device featured 5-nm-thick channel stack composed of Si cap, strained SiGe and Si layers. Typical characteristics are shown in Fig. 3. Compared to Si TFETs with identical configuration, these new devices exhibited impressive I_{ON} = 0.4 mA/μm in *p*-TFET and 0.04 mA/μm in *n*-TFET (17). The *SS* > 100 mV/decade of these devices needs further optimization.

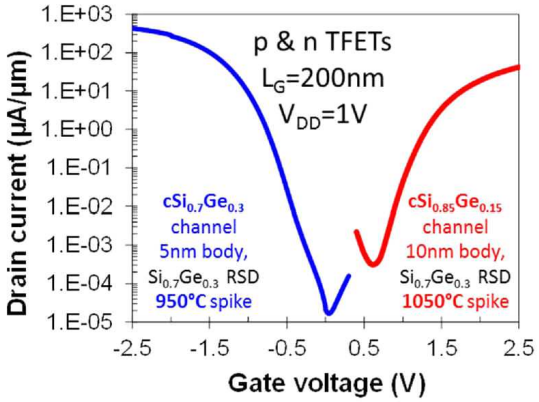

Figure 3. Transfer characteristics of *n*-type and *p*-type TFETs featuring high I_{ON} current [after Villalon *et al*. (17)].

None of the TFETs fabricated to date have exhibited high I_{ON} and sub-60 mV/dec swing simultaneously. A pertinent question is whether the current is entirely governed by BTBT. Low-temperature measurements showing a weak temperature dependence of TFET characteristics have been used to corroborate the tunneling model (16). Low-frequency noise measurements are equally informative. In MOSFETs, the carrier trapping–detrapping in slow oxide traps causes 1/*f* noise. In ultra-small MOSFETs, only a few slow traps exist in the entire device, leading to a random telegraph signal (RTS) noise with a $1/f^2$ Lorentzian spectrum. As shown in Fig. 4, the noise behavior is totally different in TFETs, where $1/f^2$ spectra and RTS signals with discrete trapping-detrapping events are observed even in large devices (18). This indicates that the effective noise-generating area of the TFET, corresponding to the ~10 nm tunneling junction, is much shorter than the L_G and includes only a discrete numbers of traps, just like a very small MOSFET. Hence, low-temperature and noise data tend to confirm that BTBT acts as the primary mechanism in TFETs.

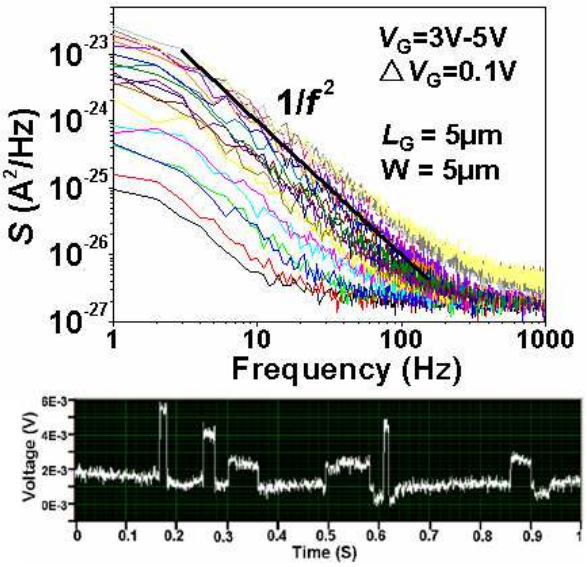

Figure 4. Low-frequency noise measurements in a large SOI TFET showing $1/f^2$ spectra (upper panel) and the RTS signal with trapping-detrapping events (lower panel) (18).

Z^2-FET: Configuration and Operation Mechanisms

The feedback-based Z^2-FET features *zero* subthreshold swing (< 1 mV/decade) and *zero* impact ionization, which explains the acronym (19). It is a compact SOI device, shown in Fig. 5(a), that experimentally demonstrates a current I_{ON}/I_{OFF} ratio > 10^8 at low supply voltage below 2 V as well as gate-controlled hysteresis.

The Z^2-FET is a forward biased *pin* diode with undoped channel partially covered by the front gate (L_G) and the rest ungated (L_{IN}). The configuration is similar to that of the TFET shown in Fig. 2(a), but the biasing and operation principles are totally different. The device is fabricated in an advanced FD-SOI process with high-κ/metal gate and raised source/drain (19). For the *p*-type Z^2-FET, the p^+ source is grounded and the n^+ drain is negatively biased ($V_S = 0$, $V_D < 0$). The device is maintained in blocked mode by negative bias on the front gate ($V_G < 0$) and positive bias on the back gate ($V_{BG} > 0$), which form electron and hole injection barriers in L_G and L_{IN} regions, respectively. These biases actually emulate a virtual *pnpn* thyristor-like structure.

The $I_D(V_G)$ characteristics show abrupt switching with 8 decades of current gain in a narrow ΔV_G = 1mV range and for reasonable bias, see Fig. 5(b). The Z^2-FET outperforms other sharp-switching devices reported to date, including the IMOS (20,21), and feedback-based FED (22) and FB-FET (23) devices. The switching threshold can be tuned by adjusting the drain ($V_D < 0$) or source ($V_S > 0$) bias.

The corresponding $I_D(V_D)$ curves are shown in Fig. 6(a). The device is initially off, but switches on sharply as $|V_D|$ increases beyond the turn-on voltage $|V_{ON}|$. As $|V_D|$ sweeps back to 0, the device remains in the high I_{ON} state until $|V_D|$ = 0.8 V. The value of V_{ON} is linearly dependent on V_G, leading to a large V_G-controlled hysteresis window. Figure 6(b) shows simulated curves, which reproduce the experimental data and indicate that the $I_D(V_D)$ characteristics are actually S-type. Impact ionization has no effect on the simulated curves (dots), as opposed to a real *npnp* thyristor.

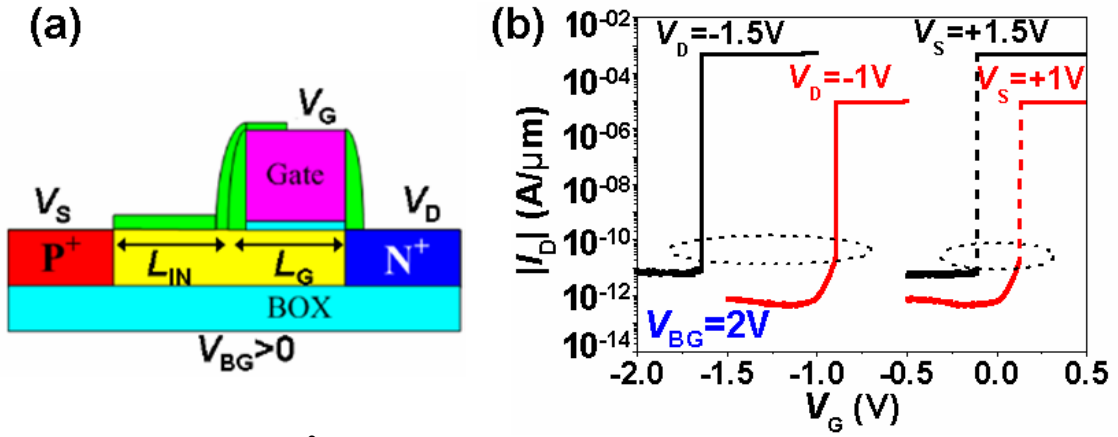

Figure 5. The *p*-type Z^2-FET: (a) configuration and biasing; (b) experimental transfer characteristics at V_{BG} = 2 V, 20 nm thick Si film, 145 nm thick BOX, L_G = 400 nm and L_{IN} = 500 nm [adapted from Wan *et al.* (19)].

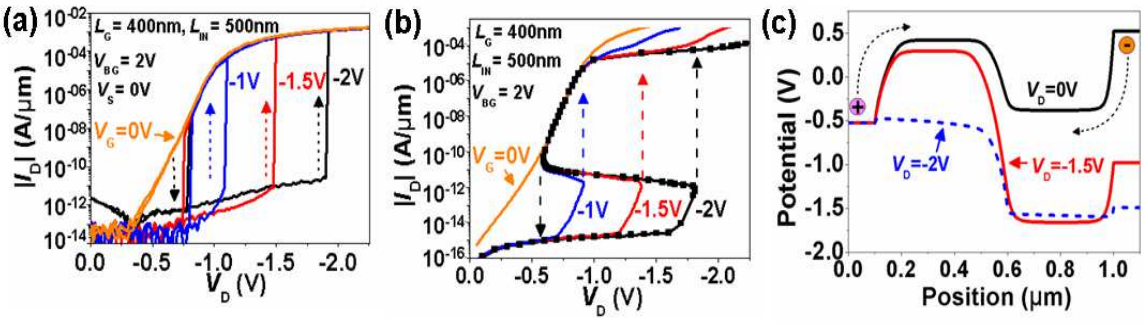

Figure 6. Output characteristics of a *p*-type Z^2-FET: (a) experiment; (b) simulations; (c) evolution of the electron and hole barriers [adapted from Wan *et al.* (19)].

The band modulation by injected carriers is the key mechanism of operation. Electron and hole barriers are formed by V_G and V_{BG} biases, inhibiting the carrier flow at low drain bias, see the $V_D = 0$ and –1.5 V potential diagrams in Fig. 6(c). As $|V_D|$ approaches V_{ON}, the drain injection barrier is sufficiently lowered to enabling the injection of a few electrons from the n^+ drain into the channel. These electrons flow to the p^+ source, where they reduce the hole barrier, permitting the injection of holes into the channel. The holes flow to the n^+ drain, further reducing the electron barrier and initiating an efficient positive feedback. For $V_D = –2$ V, both injection barriers are totally suppressed, as shown in Fig. 6(c) and the current reaches the high I_{ON} typical of a forward-biased *pin* diode.

This operation mechanism is similar to that of FED (22) and FB-FET (23) feedback-based devices, where the bands are modulated by either two adjacent front gates (22) or surface charges deposited on the gate spacers (23). The Z^2-FET configuration is simpler and more compact, as well as fully compatible with SOI technology because it has a single front gate and can use the ground plane bias, common in FD devices, for generating the second potential barrier.

The scaling of the Z^2-FET depends on the control of the relevant injection barriers by the two gates. As a general trend, when the length decreases, V_{ON} drops when V_G and V_{BG} lose control of the injection barriers in the L_G and L_{IN} regions, respectively. Ultrathin gate dielectric (1 nm), BOX (15 nm) and film (5 nm) result in better scaling capability, down to $L_G = L_{IN} = 30$ nm. It is worth noting that Z^2-FETs with ~8 nm BOX and ground plane can even be operated without a back-gate bias. The potential difference between the highly-doped ground plane ($N_D \sim 10^{20}$ cm^{-3}) and the intrinsic channel is strong enough to form the carrier injection barrier in the L_{IN} region. Scalability down to $L_G = L_{IN} = 20$ nm is possible if the Z^2-FET is designed with non-overlapping front and back gates (ground plane localized under the L_{IN} region only).

The discussion above can be transposed to *n*-type Z^2-FET, where the gate is adjacent to the p^+ doped drain. The gate and drain are positively biased, whereas the back gate is negatively biased. The operation mechanism and switching characteristics are unchanged. Finally, preliminary reliability tests show that the Z^2-FET hysteresis window is marginally affected ($\Delta V_{ON} \sim 0.1$ V) by increased temperature (up to 105 °C) or by repeated cycling for 50 hours.

Z^2-FET: Applications

Capacitorless 1T-DRAM

The conventional dynamic random access memory (DRAM) using an external capacitor for charge storage suffers from mediocre access speed and difficult capacitor scaling. The Z^2-FET hysteresis offers a new paradigm for the development of single-transistor DRAM (1T-DRAM) (24). The idea is to store the charge Q_G at the front gate of the device in Fig. 6 by setting $V_G = -1.7$ V, as illustrated in Fig. 7(a).

The biasing sequence for writing and reading the memory is shown in Fig. 7(b). The memory is programmed by pulsing V_G to zero. For state '1', a simultaneous drain pulse of V_D from zero to –1.3 V is applied: this turns on the Z^2-FET, leading to carrier injection into the channel, with the holes maintained at the front gate when V_G returns to the –1.7 V hold voltage. For state '0', no simultaneous V_D pulse is applied when V_G is pulsed to zero, so no current flows and no holes accumulate under the front gate.

The logic states are read out by a short negative V_D pulse (from zero to –1.3 V) smaller than V_{ON}. For the '1' state, the discharge of stored holes through the forward-biased drain junction triggers the feedback to turn on the device. This results in a high (~100 μA/μm) signal. By contrast, for state '0', not only is $|V_D| < |V_{ON}|$ but also there is no discharge current since the channel is empty, so the device remains blocked.

The current difference between '1' and '0' states is many orders of magnitude, offering an excellent memory margin. Since state '1' is stable, the retention time is limited by the '0' state to about 1 s, due to the gradual recharging of the accumulation layer under the gate. Note that readout automatically refreshes the '0' state by eliminating the parasitic hole charges. Frequent reading of the memory prolongs the retention time to over 5 s.

The Z^2-FET 1T-DRAM requires a much lower supply voltage than other types of SOI 1T-DRAMs (25), which explains the excellent retention capability. Further, it has a fundamental advantage that the memory state is defined by the transient current $\Delta Q_G/\Delta t$, not by the stored charge ΔQ_G as in other 1T-DRAMs (or standard DRAM). The stored hole charge Q_G is no longer a critical limitation and the DRAM trend of reducing the access time to $\Delta t \sim 1$ ns means that a relatively small Q_G is sufficient for state discrimination using the internal feedback amplification.

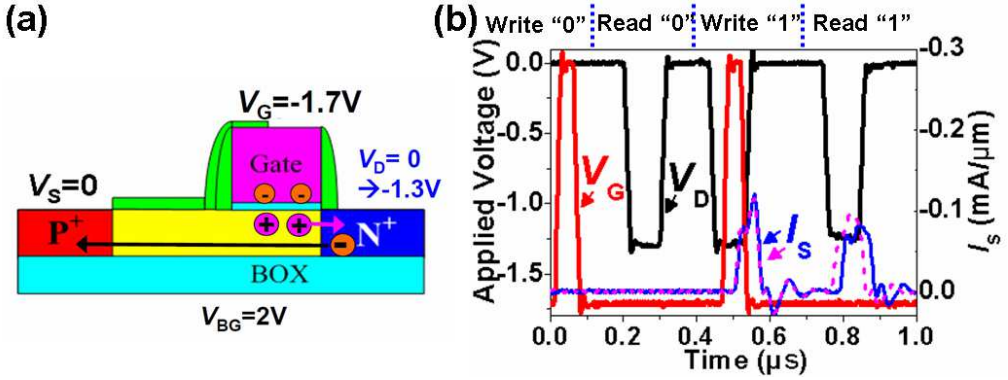

Figure 7. (a) Schematic illustration of the Z^2-FET 1T-DRAM; (b) biasing sequence and read current [adapted from Wan *et al.* (24)].

Single-Transistor SRAM

The static random access memory (SRAM), composed of six transistors, has high access speed but low integration density. The Z^2-FET can be operated as SRAM using the hysteresis in $I_D(V_D)$ domain, as shown in Fig. 8(a). The memory is programmed with $V_G = 0$ and either $V_D = 0$ (logic '0') or $V_D = –2.5$ V (logic '1'). Negligible '0' current and high '1' current are maintained in the hold state at $V_G = –1.7$ V and $V_D = –0.9$ V. To further increase the '1' current the memory is read by pulsing V_D to –1.3 V. Both logic '0' and '1' have an infinite retention time and are read out correctly after 100 s.

An obvious disadvantage of this 1T-SRAM is the significant static current and power consumption for holding logic '1'. The solution is to use a heterojunction device. Simulations show that when the channel is made of $Si_{0.7}Ge_{0.3}$ and source/drain regions are Si, the static current can be markedly reduced.

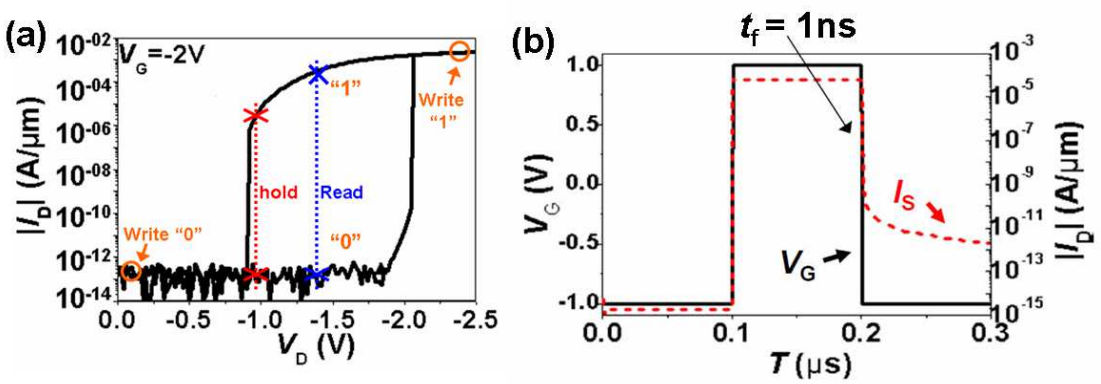

Fig. 8: (a) Operation of the Z^2-FET 1T-SRAM. (b) Transient current in Z^2-FET after pulsing the gate from –1 V to 1 V and back: a very fast fall time can turn the device off.

Logic Circuits and ESD Protection

The sharp switching of the Z^2-FET can serve for fast logic circuits. The static transfer characteristics shown in Fig. 5(b) exhibit abrupt turn-on. However, for reverse V_G scan, the device cannot be turned off because it remains latched by the high electron-hole plasma, which is almost insensible to the lowering of the gate bias.

Our simulations show that this problem is alleviated when the gate pulse has a very short fall time, as illustrated in Fig. 8(b). For 1 ns fall time, the current also switches from I_{ON} to the I_{OFF} state, with a current variation of 7 orders of magnitude. In other words, the Z^2-FET can replace MOSFET as the building block for logic circuit design, but only for extremely fast operation V_G switching, which is actually very good news.

The protection of integrated circuits against electrostatic discharges (ESD) is not a simple issue in SOI due to the presence of a thin Si film and BOX. An ideal protection device is expected to feature S-type characteristics with low I_{OFF} (to limit power dissipation) and fast switching to a high-current I_{ON} state at voltages exceeding the supplying voltage by 10%. The Z^2-FET has all these attributes and appears as a strong candidate. A distinct advantage is that the turn on voltage V_{ON} can be fine-tuned according to the application simply by adjusting the gate bias. The potential of Z^2-FETs

has recently been demonstrated with devices fabricated in advanced 28 nm FDSOI technology. Thanks to ultrathin film (< 10 nm), thin BOX and ground plane architecture, the Z^2-FET can be operated with low voltages (1.5–2 V on both gates), showing suitable triggering capability: $I_{OFF} \sim 1$ fA and $V_{ON} > 1.1$ V (26).

Surface-Charge Sensor

The Z^2-FET can also operate with surface charge (Q_S) replacing the V_{BG} action. In Fig. 9(a), the injection barrier in the underlap region L_{IN} is established by positive Q_S, whereas the other barrier is still controlled by the front-gate bias V_G. In our devices, the surface charge ($Q_S \sim 10^{12}$ cm^{-2}) was set during the chemical vapor deposition of SiO_2. The measurements show similar $I_D(V_D)$ and $I_D(V_G)$ characteristics to the V_{BG}-operated device of Figs. 5 and 6, featuring sharp switching and V_G-controlled hysteresis (24).

Figure 9(b) shows the impact of Q_S density on the turn-on voltage V_{ON}. There is a well-defined region where V_{ON} depends sensitively on Q_S, before reaching saturation. This sensitivity may prove interesting for sensing charges attached to the surface (DNA, liquids, gold nanoparticles, *etc*.). The Z^2-FET appears to be a more flexible and high-performance alternative to standard ISFETs. The sensitivity region can indeed be tuned by design, such as varying L_{IN} as shown Fig. 9(b), or by modulating the barriers with V_{BG} and V_G.

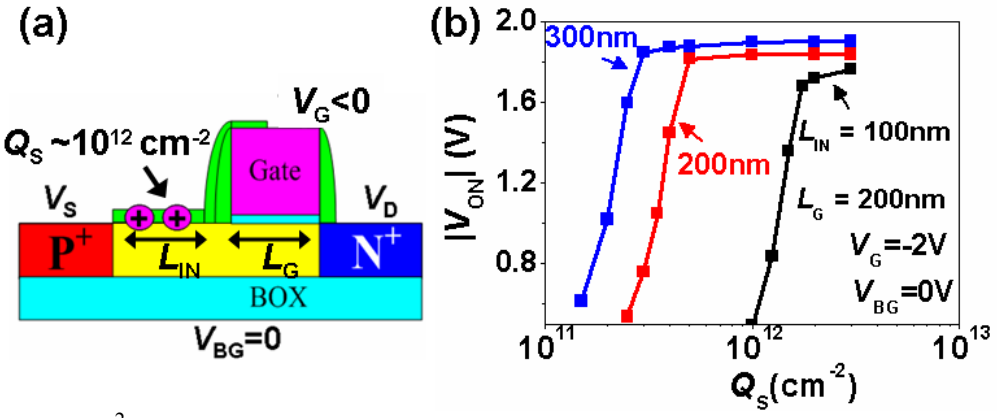

Figure 9. (a) Z^2-FET operated with positive surface charge Q_S and grounded back gate (L_G = 200 nm). (b) Simulated variation of the turn-on voltage as a function of Q_S.

Conclusions

In the first part of this paper, we reviewed the status and future trends of tunneling transistors. Recent solutions based on ultrathin films, nanowires, and heterostructures enable increasing I_{ON} current from unacceptable to reasonable values. More effort is needed for concomitantly achieving sub-60 mV/decade *SS* over a wider range of gate bias. An attractive concept is to add internal amplification of the tunneling current, as in the recently proposed BET-FET device (27).

On the other hand, extremely sharp-switching characteristics are offered by feedback-based band-modulation transistors. We have discussed in detail the Z^2-FET, which is the most compact and practical variant. The Z^2-FET is fully compatible with

SOI-CMOS fabrication, has a single front gate, and can be operated with either back-gate bias or a charge stored on the surface. The modulation of injection barriers by injected electrons and holes results in "vertical" switching with near-zero subthreshold swing $SS <$ 1mV/decade and very high $I_{ON}/I_{OFF} > 10^8$ ratio. The device also exhibits voltage-controlled hysteresis in $I_D(V_D)$ domain with the switching voltage V_{ON} linearly controlled by V_G. The Z^2-FET is scalable down to at least 20 nm and shows good temperature stability and cycling endurance. We presented a variety of applications, including a high-speed 1T-DRAM with low operating voltage, long retention (seconds), and fast access time (1 ns). The Z^2-FET can also serve as an ultra-compact 1T-SRAM, ESD protection device, charge sensor and building block for high-speed logic circuits. Since the Z^2-FET is based on a different mechanism from standard MOSFETs and exhibits outstanding performance, we believe it deserves careful examination by circuit designers.

Acknowledgments

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