Top-Gated Indium–Zinc–Oxide Thin-Film Transistors With In Situ Al2O3/HfO2 Gate Oxide

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Abstract—We report on top-gated indium–zinc–oxide (IZO) thin-film transistors (TFTs) with a 3-nm layer of aluminum between the IZO active layer and high-k HfO2 gate insulator. A series of anneals at 300 °C was used to convert the Al metal into Al2O3, resulting in high-performance top-gated TFTs. The 8-h-annealed TFT with Al layer has a threshold voltage $|V_T| < 0.5$ V, an on/off ratio of $1 \times 10^7$, a subthreshold slope (SS) of 0.14 V/decade, and a saturation mobility $\mu_S \sim 115$ cm$^2$/V·s in devices with $L_G = 50$ μm gate length. For smaller devices with $L_G = 5$ μm, the threshold voltage and SS are similar, but the on/off ratio and mobility are lower. Cross-sectional TEM images and C–$V_G$ characteristics with little hysteresis confirm that the thin Al layer, converted in situ into Al2O3, can protect the IZO channel during processing and produce a good high-k gate-stack.

Index Terms—Indium zinc oxide, thin film transistors, in-situ process, top gate, aluminum oxide.

I. INTRODUCTION

WITHIN the last decade, after the initial report by Nomura et al. in 2004 [1], oxide semiconductors have become one of the main materials for high-performance TFTs. Indium- and zinc-oxide based amorphous TFTs—such as In-Zn-O (IZO) [2], In-Ga-Zn-O [3], [4], Zn-Sn-O [5]—have been widely studied for display applications [6]. The requirements of TFTs to be used in active matrix liquid crystal displays include: a field effect mobility $\mu > 1$ cm$^2$/V·s, an on/off ratio $> 10^6$, low temperature processing, and low fabrication costs [7]. The field effect mobility of indium- and zinc-oxide compounds easily meets the mobility requirement, and many of the amorphous oxide TFTs can be fabricated at low temperature on arbitrary substrates. Besides the application in displays, the same advantages of amorphous oxide materials, such as high mobility and arbitrary substrate capability, make them potentially suitable for top-gated high-current low-cost radio frequency (RF) transistors [8]. To make such RF devices, one must obtain an appropriate dielectric gate stack with low leakage, high dielectric constant and good interface with amorphous oxide channel material. In this letter, we demonstrate a way to form a dielectric gate stack by using an in-situ metal oxidation process.

Our top-gated IZO TFTs, with channel material deposited by sputtering a 90 wt.% In2O3-10 wt.% ZnO target, feature an in-situ formed Al2O3 interlayer between the IZO channel and the HfO2 high-k gate insulator. A schematic of the as-deposited TFT structure is shown in Fig. 1(a), with a thin layer of Al metal (2-3 nm) between the IZO and the HfO2 that confers two advantages. First, the Al layer serves as a protective layer to minimize the bombardment from O and Ar ions during the atomic layer deposition (ALD) of HfO2, and thus minimize the damage to the IZO channel, which has been reported as a failure mode in top-gated oxide TFTs [9]. Second, when the TFTs are annealed, the Al layer is converted into Al2O3, and this Al2O3 can suppress the charge trapping at the IZO/HfO2 interface [10], [11]. Compared to the sputter-deposition of the Al2O3 interlayer reported by Chang et al. [11], our in-situ oxidation of Al into Al2O3 is advantageous because it can protect the oxygen-sensitive IZO from oxygen-containing deposition environment.

The in-situ formation of dielectric oxide is a consequence of the thermodynamic instability of many metals (Al, Ti, Hf, and others) in contact with In2O3 (and ZnO). As discussed in [12], this instability can be predicted from the free energy of formation values of the oxides to calculate the free energy of the overall reaction. In this case, the direction (forward or reverse) of the reaction $2\text{Al} + \text{In}_2\text{O}_3 = \text{Al}_2\text{O}_3 + 2\text{In}$ is predicted by subtracting the free energy of formation of In2O3 from Al2O3: $\Delta G = \Delta G_{\text{Al}_2\text{O}_3} - \Delta G_{\text{In}_2\text{O}_3}$. At 200 °C, the result is reported [12] to be negative (–752.6 kJ/mol) which indicates that, in the absence of kinetic constraints, Al metal will oxidize by chemically reducing In2O3 to produce...
Al₂O₃. In our TFTs, the Al metal layer is thin (2–3 nm, of which ~1 nm would be consumed by the native oxide formed on the Al surface prior to ALD of HfO₂) and was deposited on a ~10 nm IZO layer sputtered in an oxygen-rich ambient to produce fully oxidized stoichiometric In₂O₃. The IZO thickness was chosen to ensure that the underlying IZO was not fully consumed. Instead, the oxygen extracted by the Al oxidation is expected to create an oxygen vacancy-rich substoichiometric oxide, effectively doping the IZO channel [13].

II. EXPERIMENT

The fabrication sequence for the TFTs shown in Fig. 1(a) ran as follows. We started with a Si wafer coated with 500 nm of thermal SiO₂. The source and drain electrodes, active layer and top gate electrode were all patterned using conventional lift-off process. First, 10 nm Mo was deposited on source/drain areas at room temperature via DC magnetron sputtering. Then a ~10 nm IZO channel layer was deposited using DC magnetron sputtering with an 86/14 Ar/O₂ gas volume ratio and a power density of 0.22 W/cm² at a 280 V dc bias. Then a 2–3 nm Al layer was sputter-deposited onto the IZO layer. The sample was transferred into a metallization tool, where we deposited 10 nm of sputtered Mo (contact metal), 10 nm Cr (adhesion layer) and 70 nm Au (probing metal) by e-beam evaporation. Then 25 nm of HfO₂ was deposited in-situ a layer of Al₂O₃ of ~5 nm thickness. The HfO₂/Al₂O₃ dielectric stack can be modeled as two capacitors in series. In accumulation, V_G > 1 V, C reaches a constant C_MAX that decreases slightly from the as-deposited value as the Al layer turns into Al₂O₃. Conversely, in depletion, V_G < −1 V, the annealed devices exhibit a minimum capacitance (C_MIN ~ 3.7 pF) corresponding to the total capacitance of the serially connected gate insulator, fully depleted IZO layer, and the buried SiO₂ layer (together with parallel capacitance from the 150 × 150 μm gate contact pad directly on the buried SiO₂ layer). The hysteresis observed in the C-V_G curves of annealed devices is very small in 2-hour-annealed TFTs and larger in 8-hour-annealed TFTs, see Fig. 1(c). Estimating the interface trapped charge density N_TC as C_MAX × ΔV_G/q, where ΔV_G ~ 0.2 V is the width of the hysteresis loop and q is the electron charge, yields N_TC ~ 3.6 × 10¹² cm⁻², comparable to reported results on HfO₂ gate insulators on IZO [14] or IGZO [15]. The trapped charge may result from the formation of vacancies or vacancy clusters due to the Al/IZO reaction. Further study of the in-situ Al₂O₃/IZO annealed interface is needed to explain our C-V_G data and the observed TFT threshold shift.

The corresponding TFT characteristics are shown in Fig. 2, measured with the substrate grounded. Fig. 2(a) shows the I_D-V_D output curves of as-deposited TFTs with the Al layer. As a result of the Al, there is no gate control for the as-deposited device even at large V_G = −6 V, in agreement with the constant C-V_G curves. When the devices are annealed, the Al layer is converted to Al₂O₃, resulting in gate-controlled TFTs. As shown in Fig. 2(b), the devices annealed for 2 hours exhibit transistor characteristics; after an 8 hour anneal the TFTs show fully saturating output characteristics and can be pinch off at low V_G < −1 V, see Fig. 2(c).

For comparison, Fig. 2(d) shows the output curves of control TFTs fabricated in the same process without the thin Al interlayer. These TFTs show some gate control, but they cannot be fully pinched off (even when V_G ≤ −9 V) and their characteristic are not improved by annealing. The inferior performance of control TFTs is likely due to the damage...
compared to IZO channel mobility during HfO$_2$ deposition and the inferior for the larger transistor is also shown.

Transfer characteristics of Al-layer-containing TFTs with $W/L_G = 250/50$ and $15/5$ μm after an 8-hour anneal are compared in Fig. 3. All the transfer curves were measured with $V_G$ swept from positive to negative with negligible gate leakage ($< 10^{-10}$ A for the large transistor, see Fig. 3(a), and $< 5 \times 10^{-11}$ A for the small transistor). In the $L_G = 50$ μm TFT in Fig. 3(a), the on/off current ratio exceeds $10^7$, and $SS \sim 0.14$ V/decade, with no measurable threshold shift as $V_D$ is changed from 0.1 to 1 V. One can estimate the saturation mobility $\mu_S$ and threshold voltage $V_T$ by the standard $I_D^{1/2}$ vs. $V_G$ technique [16].

$$I_D = \mu_S \times C_{ox} \times (W/2L_G) \times (V_G - V_T)^2,$$

to obtain $\mu_S \sim 115 ~\text{cm}^2/\text{V} \cdot \text{s}$ at $V_D = 1 \text{ V}$ and $V_T \sim 0.06 \text{ V}$, which matches the threshold voltage from $C_VG$ curves – see inset in Fig. 3(a). In the smaller $L_G = 5$ μm TFT shown in Fig. 3(b), the saturation mobility, on/off ratio, $V_T$ and subthreshold slope are estimated at $6.7 ~\text{cm}^2/\text{V} \cdot \text{s}$, 0.13 V, 2.6 $\times 10^6$ and 0.14 V/decade.

The mobility of $L_G = 50$ μm TFTs is high, but similar values were recently reported in large top-gated IZO-based TFTs [17] (and Al-doped ZnO TFTs [18], although those devices had crystalline channel material). The estimated $\mu_S$ of $L_G = 5$ μm TFTs is much lower, possibly due to source contact resistance or increased scattering due to interface diffusion of metal from the contacts (which is still under investigation), but even so the $L_G = 5$ μm TFTs provide similar maximum $I_D$ and a slightly better subthreshold slope compared to $L_G = 50$ μm TFTs. In both large and small TFTs, the SS and on/off ratio are very good, comparable to the best reported values.

The measurements on the annealed Al-layer-containing TFTs were taken within two weeks after fabrication, as the device characteristics then begin to degrade in these non-encapsulated prototype devices.

IV. CONCLUSIONS

We fabricated top-gated IZO TFTs with 3 nm Al metal layer between IZO channel and high-k HfO$_2$ gate dielectric. We have shown that annealing at 300 °C converts the Al layer into Al$_2$O$_3$, resulting in TFTs that show good characteristics with a low $|V_T| < 0.5$ V, on/off ratios larger than $10^7$, and a subthreshold slope of 0.14 V/decade. The estimated saturation mobility $\mu_S$ of large $L_G = 50$ μm TFTs is very high at 115 cm$^2$/V·s, whereas $\mu_S$ in small $L_G = 5$ μm TFTs is lower, possibly due to contact resistance. Our in-situ approach to producing a thin Al$_2$O$_3$/HfO$_2$ high-k stack with low leakage and trapped charge is promising for high-performance submicron oxide TFTs.

REFERENCES