Channel scaling and field-effect mobility extraction in amorphous InZnO thin film transistors

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A B S T R A C T

Amorphous oxide semiconductors (AOSs) based on indium oxides are of great interest for next generation ultra-high-definition displays that require much smaller pixel driving elements. We describe the scaling behavior in amorphous InZnO thin film transistors (TFTs) with a significant decrease in the extracted field-effect mobility $\mu_{FE}$ with channel length $L$ (from 39.3 to 9.9 cm$^2$/V$\cdot$s as $L$ is reduced from 50 to 5 $\mu$m). Transmission line model measurements reveal that channel scaling leads to a significant $\mu_{FE}$ underestimation due to contact resistance ($R_C$) at the metallization/channel interface. Therefore, we suggest a method of extracting correct $\mu_{FE}$ when the TFT performance is significantly affected by $R_C$. The corrected $\mu_{FE}$ values are higher (45.4 cm$^2$/V$\cdot$s) and nearly independent of $L$. The results show the critical effect of contact resistance on $\mu_{FE}$ measurements and suggest strategies to determine accurate $\mu_{FE}$ when a TFT channel is scaled.

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1. Introduction

Amorphous oxide semiconductors (AOSs) based on In$_2$O$_3$ are technologically promising due to high carrier mobility [1–3] and excellent optical transmittance [1] in the visible. Therefore, AOS materials have been integrated as active layers [2,4] and electrodes [2,5,6] into a variety of electronic devices, such as high performance thin film transistors [2,7] (TFTs) and fast photodetectors [8,9]. This class of materials has been gaining particular attention in next generation displays due to their much higher TFT field effect mobility $\mu_{FE}$ (>10 cm$^2$/V$\cdot$s vs. 1 cm$^2$/V$\cdot$s) [1–3] and low temperature ($T$) processability (RT–100 °C vs. ~300 °C) [1–4] compared to conventional amorphous Si (a-Si)-based TFTs. Additional advantages of AOSs include isotropic wet etch characteristics [7] and compatibility with mass production [10], all of which make this material suitable for large area, flexible, and transparent devices on inexpensive polymer substrates [11].

To date, many researchers have extensively contributed to the development of high-performance and stable AOS TFTs. These efforts include studies of thermal [12] and bias stress [13,14] stability, the elucidation of doping mechanisms [15,16], threshold voltage stability [12–14,17], the investigation/improvement of channel/metallization contact properties [2,18,19], and amorphous phase stability [12,20]. Therefore, some AOS materials such as InGaZnO (IGZO) are now being deployed in high performance and flexible active-matrix liquid crystal displays and active-matrix organic light emitting diode technologies [10]. Compared to industrialized IGZO TFTs, IZO TFTs have shown markedly higher field-effect mobility [4,12], making them promising for high-current devices in future technologies.

An important future technological challenge is the downscaling of AOS TFTs for ultra-high-definition (UHD) displays. Since these next-generation technologies utilize much smaller pixel sizes for UHD resolution, AOS TFTs employed as pixel driving elements must be scaled down as well. When the dimensions of TFT devices (e.g., channel length $L$ and width $W$) are reduced, important device characteristics such as the field-effect mobility $\mu_{FE}$, threshold voltage $V_T$, and device saturation behavior are expected to be affected by scaling, like conventional metal-oxide-semiconductor field effect transistor (MOSFET) devices. Previous studies by Jeong et al. [21] and Barquinha et al. [22] reported that the field-effect mobility of sputter-processed amorphous IGZO TFTs decreased from ~10 cm$^2$/V$\cdot$s to 3.5 cm$^2$/V$\cdot$s (IZO source/drain or S/D) and...
\( \text{~24 cm}^2/\text{V s} \) to 10 \( \text{cm}^2/\text{V s} \) (IZO, Ti/Mo S/D) as channel length \( L \) was downscaled. They attributed these \( \mu_{FE} \) decreases to the effect of increasing parasitic resistance. Hu et al. [23] found a similar behavior in solution-processed ZnSnO TFTs, where \( \mu_{FE} \) decreased from 8 to 6 \( \text{cm}^2/\text{V s} \) (Mo S/D) and from 6 to 1 \( \text{cm}^2/\text{V s} \) (Ti/Au S/D) as \( L \) was scaled down from 300 \( \mu m \) to 3 \( \mu m \), again attributing the decrease in \( \mu_{FE} \) to contact resistance. In the reports by Jeong [21] and Barquinha [22], the difference between Mo and Ti/Au metallized devices was attributed to the formation of TiO\(_2\) in the Ti/Au S/D case. These reports are in basic agreement with our previous study [12] that suggested metallization strategies for AOS-based TFTs to ensure lower contact resistance. However, while the previous reports [21–23] described the channel scaling-induced \( \mu_{FE} \) reduction, a method to correctly evaluate \( \mu_{FE} \) in downscaled AOS-based TFTs was not provided.

In this study, we report on the effect of channel downsizing in amorphous InZnO (a-IZO) TFTs on the device performance. Back-gated devices with various \( L \) and \( W \) were fabricated, and the output and transfer characteristics were compared as a function of \( L \). We have found that the extracted \( \mu_{FE} \) decreases strongly with \( L \): from 39.3 \( \text{cm}^2/\text{V s} \) (\( L = 50 \mu m \)) to 9.9 \( \text{cm}^2/\text{V s} \) (\( L = 5 \mu m \)) while the threshold voltage \( V_T \) became more negative in small \( L \) devices and, furthermore, smaller devices required a larger drain bias \( V_D \) to achieve drain current saturation and show higher off-state currents. Transmission line model (TLM) measurements and a modified extraction procedure were used to evaluate the effect of contact resistance at the channel/metalization interface and its subsequent impact on the extraction of \( \mu_{FE} \) in a-IZO TFTs with channel scaling.

2. Experimental details

In our a-IZO TFTs, the channel, source/drain (S/D), and gate contact electrodes were deposited at room temperature using dc magnetron sputtering with a target-to-substrate distance of 10 cm. Before all depositions, the sputter chamber was pumped down to a base pressure lower than \( 6 \times 10^{-6} \) Torr and the target was pre-sputtered for 1000 s to remove surface contamination and to ensure homogeneous distribution of process gas in the sputter chamber. To investigate the channel IZO and the channel scaling behavior without the added complications due to the processing of gate dielectric layers, a bottom-gated device structure was used. We note that top-gated devices with near-zero threshold voltage using the same IZO channel material were reported by Song and co-workers previously [24]. The a-IZO TFTs were fabricated on heavily-doped single-crystal n-Si substrates (0.003–0.005 \( \Omega \) cm) covered with a 50 nm thermally grown SiO\(_2\) layer that was used as gate dielectric. The 10 nm thick IZO films were sputtered from a commercially available 90 wt% In\(_2\)O\(_3\)-10 wt% ZnO target (Idemitsu Corp., Japan) using a dc power density of 0.22 \( \text{W/cm}^2 \) at 280 V with deposition power of \( 0.035 \) \( \text{nm/s} \), a chamber pressure of 2 mTorr, and an Ar/O\(_2\) gas volume fraction of 86/14. For S/D contact pads (100 \( \mu m \times 100 \mu m \)) Mo metal films (\( \sim 100 \) nm) were deposited at 0.88 \( \text{W/cm}^2 \) at 350 V at a deposition rate of 0.09 \( \text{nm/s} \). The channel and S/D regions were defined using a conventional photolithography and a lift-off with positive photo-resist (S-1818). The back side of the wafer was wet-etched with buffered HF to remove any oxides and then a Mo contact metallization was sputter-deposited at the same condition as for the S/D electrode metallization. Transistor transfer and output characteristics were measured using an Agilent 4155C semiconductor parameter analyzer in a light-tight probe station. To minimize the effect of photoconductivity in the IZO channel, the device performance was evaluated after resting at least 10 min in the light-tight probe station.

3. Results and discussion

The drain current–voltage (\( I_D-V_D \)) output characteristics were measured by sweeping \( V_D \) from 0 to 15 V at fixed \( V_G \) that ranged in 2 V steps from −10 to 10 V. An inset in Fig. 1(a) shows a top view schematic (not to scale) of IZO TFTs used in the present study, where the Mo S/D electrode length is 100 \( \mu m \). Fig. 1(a)–d presents the typical \( I_D-V_D \) plots of the a-IZO TFTs with \( W/L = 100/50, 100/20, 100/10 \) and 100/5 \( \mu m \), respectively, showing the significant effect of the channel downsizing on the output characteristics. It is evident in Fig. 1 that the drain current increases for shorter \( L \) due to a decrease in the channel resistance and, therefore, \( I_D \) saturation behavior is not observed for \( V_D < 15 \) V when \( L = 10 \) and 5 \( \mu m \). Further, the devices with \( L < 50 \mu m \) cannot be fully turned off by the application of the relatively large \( V_C \) of −10 V.

The transfer characteristics of these a-IZO TFTs are presented in Fig. 2. The transfer \( I_D-V_C \) plots, measured at \( V_D = 0.2 \) V are plotted in Fig. 2(a) as a function of channel length \( L \). While on- and off-state drain currents both slightly increase with decreasing \( L \), the on/off \( I_D \) ratio is similar (\( \sim 10^5 \)) regardless of TFT channel length. The field effect mobility \( \mu_{FE} \) and threshold voltage \( V_T \) of the IZO TFTs were determined in the linear regime using the conventional MOSFET equation for \( V_D \ll (V_C - V_T): \)

\[ I_D = \mu_{FE} \frac{C_{ox}}{L} \frac{W}{2} \left( \frac{V_C - V_T}{V_D} - \frac{V_D^2}{2} \right) \]  

\[ \approx \mu_{FE} \frac{C_{ox}}{L} \frac{W}{2} (V_C - V_T) V_D \]  

where \( C_{ox} \) is the oxide capacitance (6.90 \( \times 10^{-8} \text{F/cm}^2 \) for 50 nm-thick SiO\(_2\)) used in our IZO TFTs. In Fig. 2(b), the extracted field effect mobility decreases as the channel length decreases from 39.3 \( \pm 2.6 \) \( \text{cm}^2/\text{V s} \) (\( L = 50 \mu m \)) to 9.9 \( \pm 2.3 \) \( \text{cm}^2/\text{V s} \) (\( L = 5 \mu m \)). Since the devices were fabricated simultaneously on the same Si substrate, the changes observed in the transfer characteristics and field effect mobility are solely attributed to channel downsizing. Additional backgated TFT devices were fabricated with the channel width \( W \) scaled down together with the channel length \( L \). We investigated the TFT aspect ratio of 20 (i.e., TFTs with \( W/L = 100/50, 50/25, 200/10, \) and 100/5 \( \mu m \)). Those devices exhibited the same trend in extracted \( \mu_{FE} \) as shown in Fig. 2. A similar decrease in \( \mu_{FE} \) with decreasing \( L \) was also observed in top-gated a-IZO TFTs [24].

To examine the performance variation in our IZO TFTs with channel length, TLM measurements were made on more than 48 IZO TFTs as a function of \( L \) and \( W \). The TLM analysis allows the determination of both the channel resistivity and contact resistance through the equation [2,25] \( (R_{total} W) = (2R_{C} W) + (R_{C} L) \), where \( R_{total} W \) is the total resistance measured in the Ohmic (linear) regime of the output curve (at \( V_D = 0.2 \) V in this study), \( R_C \) is the channel sheet resistance, and \( R_L \) is the metallization/channel contact resistance. Detailed principles and procedures to extract contact resistances and the channel resistivity can be found elsewhere [2,27,25]. The total resistance normalized to channel width \( (R_{total} W) \) is displayed in Fig. 3 as a function of \( L \). The contact resistance is determined from the y-axis intercept (2\( R_{C} W \)), whereas the channel resistivity is calculated from the slope of the linear plot and the thickness (10 nm) of the IZO channel. The channel resistivity \( \rho \) of all IZO TFTs in this study is determined by the single slope of the plot in Fig. 3 and is found to be nearly identical as 2.03 \( \times 10^{-4} \Omega \) cm, as expected since the devices were fabricated simultaneously using the same processing sequence. Therefore, we conclude that the changes in the TFT performance shown in Fig. 2 with decreasing channel length is not associated with the alteration in channel conductivity, but rather the contact resistance. The inset in Fig. 3 shows a magnified \( (R_{total} W) \) vs. \( L \) plot...
for $W = 100 \, \mu m$ devices. From the y-axis intercept of the IZO TFTs with $W/L = 100/5, 100/10, 100/20$ and $100/50$ \( \mu m \), the specific contact resistance ($\rho_c$) of the devices is found to be $6.26 \times 10^5 \Omega \, cm^2$. This $\rho_c$ is significantly lower than those of our previous studies of approximately $0.1 – 100 \, \Omega \, cm^2$, which is attributed to the much larger carrier density of $7.7 \times 10^{18}/cm^3$ in the present study than $4.6 \times 10^{16}/cm^3$ of the TFTs with higher $\rho_c$, where the carrier density was estimated applying $\rho_c = (\xi n \mu_{FE})^{-1}$. 

Continuing with the TLM analysis, Fig. 4(a) plots the ratio of $2\rho_c$ to $R_{Total}$. It should be emphasized that the $2\rho_c/R_{Total}$ ratio increases with decreasing $L$: for instance, at $V_G = 0$, the $2\rho_c/R_{Total}$ ratio in the $L = 5 \, \mu m$ is 16.4%, roughly a factor of 8 higher than the 2.1% value in the $L = 50 \, \mu m$ device. This trend is obviously explained by the reduction in channel resistance with $L$ and hence an increase of the $2\rho_c$ component of $R_{Total}$. We also observe an effect of the gate bias magnitude on the $2\rho_c/R_{Total}$ ratio, which increases as $V_G$ becomes more positive (e.g., at $V_G = 10 \, V$, $2\rho_c/R_{Total} = 4.5\%$ and $31.0\%$ for $L = 50$ and $5 \, \mu m$, respectively). This is due to the $V_G$-controlled injection of electrons into the IZO channel that leads to a decrease in channel resistance and consequently $R_{Total}$. The results shown in Fig. 4(a) clearly show that the effective (not the absolute value applied on drain) source-drain $V_D$ decreases significantly as channel scales down. Defining the contact resistance-corrected effective drain voltage $V_{D0}$ as follows:

$$V_{D0} = V_D[1 - (2\rho_c/R_{Total})]$$

we can use the plots shown in Fig. 4(a) to recalculate the corrected output characteristics, shown in Fig. 4(b) and (c) for the IZO TFTs with $L = 50 \, \mu m$ (longest in this study) and $5 \, \mu m$ (shortest), respectively. The dotted lines represent the corrected curves, showing an increase of $I_D$ compared to the measured characteristics that are affected by contact resistance. Since the $2\rho_c/R_{Total}$ ratio increases strongly as $L$ decreases, the correction is much more prominent for $L = 5 \, \mu m$ IZO TFTs. Note that the validity of the corrected curves is limited to the linear regime (i.e., $V_D < 5 \, V$ for...
In order to consider the effect of contact resistance on \( \mu_{FE} \) and \( V_T \) as channel scales down and to determine the corrected values, Eq. (1) should be rewritten in terms of the contact-resistance corrected drain voltage \( V_D^0 \) and \( V_G^0 \), where \( V_G^0 \) is the actual gate-to-source bias defined as \( V_G^0 = V_G - V_D(R_C/R_{Total}) \). In the linear regime, Eq. (2) becomes:

\[
I_D = \mu_{FE}C_ox \frac{W}{L}(V_G^0 - V_D) \]

\[
= \mu_{FE}C_ox \frac{W}{L} \left[ V_G - V_D \left( \frac{R_C}{R_{Total}} \right) \right] - V_T \left[ V_D \left( 1 - 2 \frac{R_C}{R_{Total}} \right) \right] \quad (4)
\]

Eq. (4) can be rewritten by combining relevant terms as:

\[
I_D = \left\{ \mu_{FE} \left( 1 - 2 \frac{R_C}{R_{Total}} \right) \right\} C_ox \frac{W}{L} \left[ \left[ V_G - V_D \left( \frac{R_C}{R_{Total}} \right) \right] - V_T \right] V_D \quad (5)
\]

According to this analysis and Eq. (5), the experimentally extracted field-effect mobility shown in Fig. 2(b) is actually \( \mu_{FE}(1 - 2R_C/R_{Total}) \), which clearly underestimates the true \( \mu_{FE} \). Further, when correcting \( \mu_{FE} \), \( V_G^0 \) needs to be recalculated as well, additionally increasing the corrected resistance particularly for shorter channel devices because the \( (R_C/R_{Total}) \) factor is significantly higher, see Fig. 4(a). Unlike the underestimation of the extracted field effect mobility, no significant changes are expected for the threshold voltage after modification of the MOSFET equation: \( V_T(R_C/R_{Total}) \) is as small as \( -0.002 \)–\( -0.03 \) V at the small \( V_D = 0.2 \) V used to measure the transfer characteristics. Instead, the change in threshold voltage visible in Fig. 2(a) is likely due to the instability of IZO TFTs under dc gate voltage bias: it has been reported that the \( V_T \) of IZO TFTs changes after stressing [26–28].

The corrected field-effect mobility and the threshold voltage values, extracted from Eq. (5) and the corrected \( I_D-V_D \) plots in the linear regime at small \( V_D = 0.2 \) V, are plotted in Fig. 5(a) and (b), respectively. The uncorrected \( \mu_{FE} \) and \( V_T \) values are also presented for comparison. The corrected mobility of \( L = 50 \) \( \mu \)m TFTs is only slightly higher (45.4 ± 1.4 cm²/Vs) than the uncorrected \( \mu_{FE} \) value of 39.3 ± 2.6 cm²/Vs. On the other hand, significant \( \mu_{FE} \) differences are observed in shorter channel TFTs: corrected \( \mu_{FE} \) values are much higher than uncorrected values and nearly identical (46 cm²/Vs) for all \( L \). Therefore, the apparent collapse of the measured field-effect mobility in the shorter channel TFTs is mainly due to the larger contribution of contact resistance to the total resistance and the resulting decrease in effective \( V_D \) and \( V_G \) (a similar mobility collapse was noted in top-gated IZO TFTs and attributed to contact resistance [24], but no experimental validation was possible due to the lack of TLM patterns). Clearly, the modified Eq. (5) is useful in accurately analyzing the field-effect mobility of oxide TFTs, particularly as \( L \) is scaled down.
The comparison of the $V_t$ between the corrected and uncorrected results is presented in Fig. 5(b). As theoretically discussed in connection with Eq. (5), recalculated threshold voltages are similar to the experimentally measured uncorrected $V_t$ values. Therefore, threshold voltage shifts cannot be attributed to contact resistance issues, but rather to intrinsic voltage stress instabilities of the IZO TFTs [26–28].

4. Conclusion

In conclusion, as the channel length $L$ of IZO TFTs is scaled down, direct experimental extraction of the field-effect mobility severely underestimated it due to increasing series contact resistance effects. The increasing $R_s/R_{total}$ ratio leads to a decrease in effective $V_D$ and $V_C$. The TLM measurements and theoretical analysis provide the corrected $I_D-V_D$ curves, from which the corrected field-effect mobility can be extracted. In our backgated IZO TFTs, this corrected field effect mobility is as high as $-46 \text{ cm}^2/\text{V s}$ and nearly identical regardless of channel length $L$. No significant contact-resistance-induced correction in threshold voltage is observed. Our findings regarding the channel scaling may be useful in the analysis of other amorphous oxide TFTs, especially since future ultra-high definition displays will require downscaled TFTs with high current drive.

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References

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