Unijunction Transistor on Silicon-On-Insulator Substrate

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Abstract

A unijunction transistor based on fully-depleted silicon-on-insulator substrate is proposed. The device structure is similar to a junction field effect transistor. By conducting the TCAD simulation, we observe sharp switching and large hysteresis in emitter current-emitter voltage curves with the turn-on voltage linearly controlled by the second base voltage. The operation of the device is mainly determined by the emitter-channel PN junction, which is induced by the backgate voltage. The impact of the backgate voltage on the electrical characteristics is analyzed by changes in the channel potential.

1. Introduction

The unijunction transistor (UJT) is a unique type of semiconductor device originally demonstrated in bulk silicon substrates several decades ago [1, 2]. It had shown interesting electrical characteristics, such as sharp switching and a large hysteresis window modulated by the applied bias. The bulk UJT device was employed in compact oscillators, light dimmers, motor controllers, sensors and artificial neural networks [1-5].

This work presents an implementation of UJT on a fully-depleted silicon-on-insulator (FD-SOI) substrate. Compared to bulk Si, the SOI substrate has numerous advantages, such as low parasitic capacitance and low leakage current. It has been used extensively for low-power and high-frequency integrated circuits [6-8]. The circuits built on SOI substrates also have better resistance to high energy radiation, and can operate at higher voltages and temperatures than their bulk Si counterparts [9]. Besides, the backgate voltage (V_{BG}) provides an extra knob to tune the electrical characteristics of the transistor [10, 11]. In this work, we investigate the operation of the FD-SOI UJT through TCAD simulation. The device structure is presented, followed by electrical characteristics and corresponding operation principles. We also examine the impact of V_{BG} on the electrical characteristics.

2. Device structure and electrical characteristics

Figure 1 shows the schematic structure of the UJT on an FD-SOI substrate used in our TCAD simulations. The SOI substrate has 145nm buried oxide layer (BOX) and 100nm top Si layer. Both Si substrate and top Si layer are lightly P-type (10^{15} cm^{-3}), whereas the two base electrodes are heavily N-type (10^{20} cm^{-3}) and situated on both sides of the channel. The heavily P-type (10^{20} cm^{-3}) emitter is placed at the middle of the channel. The gaps between emitter and the base electrodes are both 2μm, whereas the length of the emitter is 1μm. The structure is similar to a junction field effect transistor (JFET), but here the P-N junction in the middle of the channel is forward-biased rather than reverse-biased.

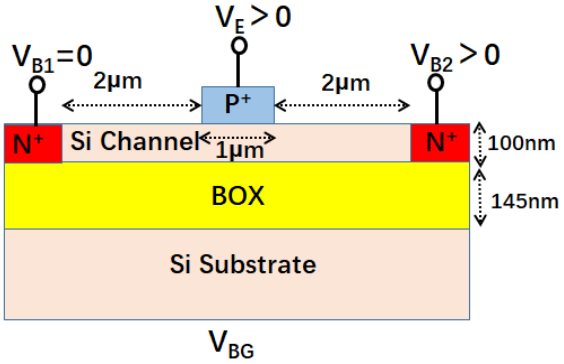

Figure 1. Schematic view of the UJT on FD-SOI substrate.

The TCAD simulation was performed with Synopsys Sentaurus (Version H-2013.03). Figure 2 shows the emitter current-voltage (I_E-V_E) curves as a function of V_{B2} ranging from 3V to 5V, with the first base grounded (V_{B1} = 0) and V_{BG} = 20V. As V_E increases from zero, the emitter current starts increasing exponentially as in a regular PN diode. Then, the device is sharply turned on and the emitter current ramps up from about 1 μA/μm by 3-4 orders of magnitude. The turn-on voltage (V_{ON}) is almost linearly modulated by V_{B2}. During the reverse sweep, the device remains in the high-current state until

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V_E is reduced to ~1.2V, at which point it turns off sharply, see Fig. 2. This results in a large V_{B2}-controlled hysteresis, similar to that reported in bulk Si UJTs.

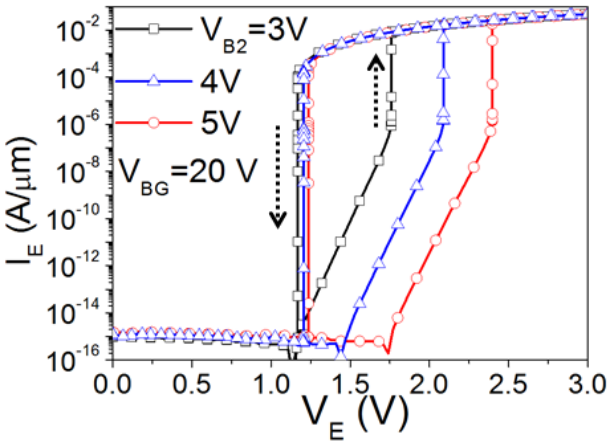

Figure 2. I_E-V_E characteristics *vs.* V_{B2} with V_{B1} grounded.

The sharp switching and hysteresis effects in the UJT are due to its unique operating mechanism. The V_{BG} = 20V induces an electron layer in the channel, which forms a PN junction with the emitter in the middle of the channel. As the emitter voltage gets higher than the channel potential, the PN junction becomes forward-biased. As the forward bias increases, large densities of minority carriers (holes) are injected from the emitter into the channel and flow to ground (the first base electrode). This reduces the resistance and the potential drop in the channel between the first base and emitter. Thus, the forward bias of the PN junction increases and further promotes the injection of minority carriers, resulting in positive feedback that turns on the device sharply. After being turned on, the channel between the first base and the emitter remains filled with minority carriers and hinders the turn-off of the device. This results in the large hysteresis window.

3. Impact of backgate voltage on the device

Unlike the UJT in bulk Si, the backgate voltage V_{BG} plays a vital role in the operation of the SOI-based UJT. Figure 3(a) shows the simulated I_E-V_E characteristics of the device with V_{BG} ranging from 0 to 20V for fixed V_{B2} = 4V. The V_{BG} affects the I_E-V_E characteristics significantly. At V_{BG} = 0, neither sharp switching nor hysteresis is observed, see Fig. 3(a). But at sufficiently high V_{BG}, sharp switching and hysteresis are restored. The value of V_{BG} also modulates the turn-on voltage of the device: compare V_{ON} at V_{BG} = 20V and V_{BG} = 10V in Fig. 3(a).

The impact of V_{BG} on the device characteristics can be explained by changes in the channel potential, see Fig. 3(b). As discussed above, the operation of the device is mainly determined by the emitter-channel PN junction. The potential V_C at the midpoint of the channel determines the forward voltage of the PN junction as $V_{PN} = V_E - V_C$. At V_{BG} = 0, the channel is depleted and most of applied V_{B2} drops in the channel near the second base. Thus, V_C remains very low and cannot block the turn-on of the device. If V_{BG} is increased to 10V, an electron layer is created in the channel and V_C increases to about 1.5–2V, which restores the sharp-switching behavior and increases the V_{ON} of the device.

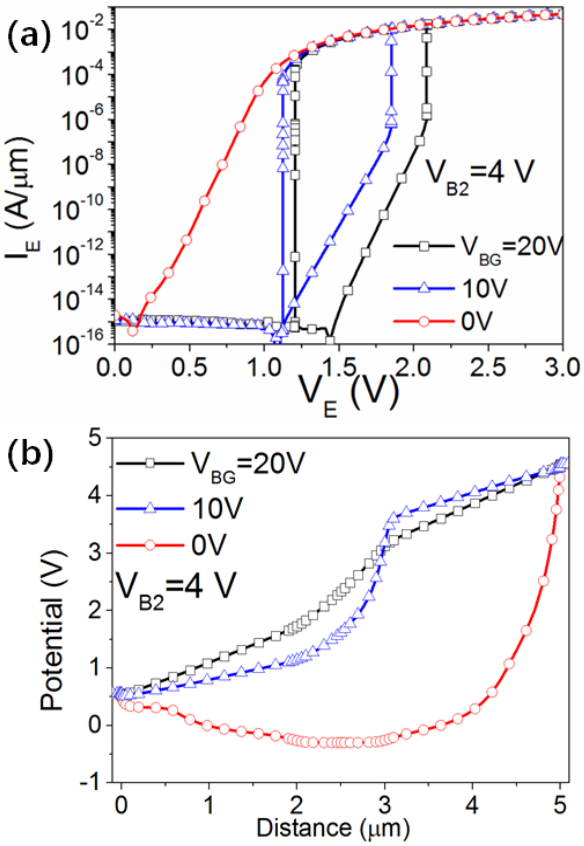

Figure 3. (a) Impact of backgate voltage on the I_E-V_E characteristics at fixed V_{B2} = 4V; (b) Potential profile along the channel for V_{BG} = 0, 10, and 20V.

4. Conclusions

In this work, we have discussed UJT devices built on FD-SOI substrates. The device structure is similar to a JFET, except for the forward-biased emitter-channel PN junction. With appropriate biasing, the device exhibits sharp switching and a large voltage-controlled hysteresis window, similar to a bulk Si UJT. The turn-on voltage is linearly modulated by the voltage applied to the second base. The backgate voltage, which emulates an N-type body, controls device operation and performance, as explained by the potential distribution in the channel.

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Acknowledgments

This work was supported by the National Key R&D Program of China (2018YFB2202800) and the Shanghai Rising Star Program (19QA1401100).

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